

# High Efficiency Li-Ion Battery Charger for Photovoltaic Sources

#### DESCRIPTION

The TS52001 is a DC/DC synchronous switching Liion Battery Charger with fully integrated power switches, internal compensation, and full fault protection. The TS52001 utilizes a temperature-independent photovoltaic Maximum Power Point Tracking (MPPT-Lite<sup>TM</sup>) calculator to optimize power output from the source during Full Charge Constant-Current (CC) mode. The switching frequency of 1MHz enables the use of small filter components, resulting in smaller board space and reduced BOM costs.

In Full Charge Constant-Current mode the duty cycle is controlled by the MPPT-Lite<sup>TM</sup> regulator. Once termination voltage is reached, the regulator operates in voltage mode. When the regulator is disabled (EN is low), the device draws 10uA quiescent current.

The TS52001 includes supervisory reporting through the nFLT (Inverted Fault) open drain output to interface other components in the system. Device programming is achieved by an I<sup>2</sup>C interface through SCL and SDA pins.

### **APPLICATIONS**

- Portable solar chargers
- Off-grid systems
- Wireless sensor networks
- Smoke detectors
- HVAC controls

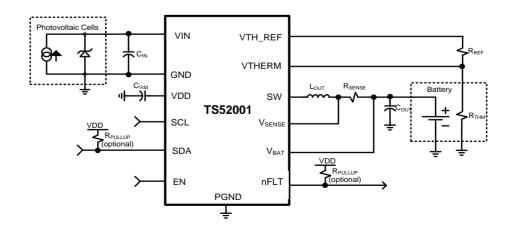
#### **FEATURES**

- Utilizes a temperature-independent PV MPPT-Lite<sup>TM</sup> regulation scheme
- V<sub>BAT</sub> reverse current blocking
- Programmable temperature-compensated termination voltage with +/- 1% tolerance
- Up to 1.5A of continuous output current in Full Charge Constant-Current (CC) mode
- User programmable charging current
- High efficiency up to 92% at typical load
- Current mode PWM control in constant voltage
- Supervisor for V<sub>BAT</sub> reported at the nFLT pin
- Input supply under-voltage lockout
- Full protection for V<sub>BAT</sub> over-current, over-temp, over-voltage, and charging timeout
- Charge status indication
- I2C program interface with EEPROM registers

### **SUMMARY SPECIFICATIONS**

- Wide input voltage range: 4.0V to 8.1V
- Packaged in a 16pin QFN (4x4)

## TYPICAL APPLICATION



# **PINOUT**

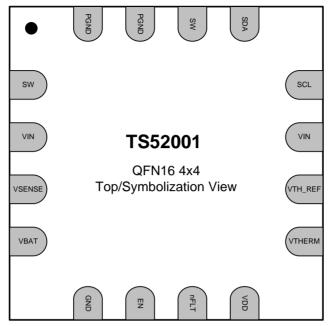


Figure 1b: Package Pinout Diagram

# PIN DESCRIPTION

Pin Symbol	Pin#	Function	Description				
SW	1	Switching Voltage Node	Connected to 4.7uH (typical) inductor				
VIN	2	Photovoltaic Input Voltage	Input voltage				
VSENSE	3	Current Sense Positive Input	Positive input for the MPP current loop.				
VBAT	4	Battery Input	Regulator Feedback Input				
GND	5	GND	Primary ground for the majority of the device except the low-side power FET.				
EN	6	Enable Input	Above 2.2V the device is enabled. GND the pin to disable the device. Includes internal pull-up.				
nFLT	7	Inverted Fault	Open-drain output.				
VDD	8	Internal 3.3V Supply Output	Connected to 100nF capacitor to GND				
VTHERM	9	Battery Temperature Sensor Minus Node	Minus node for the thermistor which is located in close proximity to the battery.				
VTH_REF	10	Battery Temperature Sensor Positive Node	Positive node for the thermistor which is located in close proximity to the battery				
VIN	11	Photovoltaic Input Voltage	Input voltage				
SCL	12	Clock Input	I <sup>2</sup> C clock input.				
SDA	13	Data Input/Output	I <sup>2</sup> C data open-drain output.				
SW	14	Switching Voltage Node	Connected to 4.7uH (typical) inductor				
PGND	15	Power GND	GND supply for internal low-side FET/integrated diode				
PGND	16	Power GND	GND supply for internal low-side FET/integrated diode				

## **FUNCTIONAL BLOCK DIAGRAM**

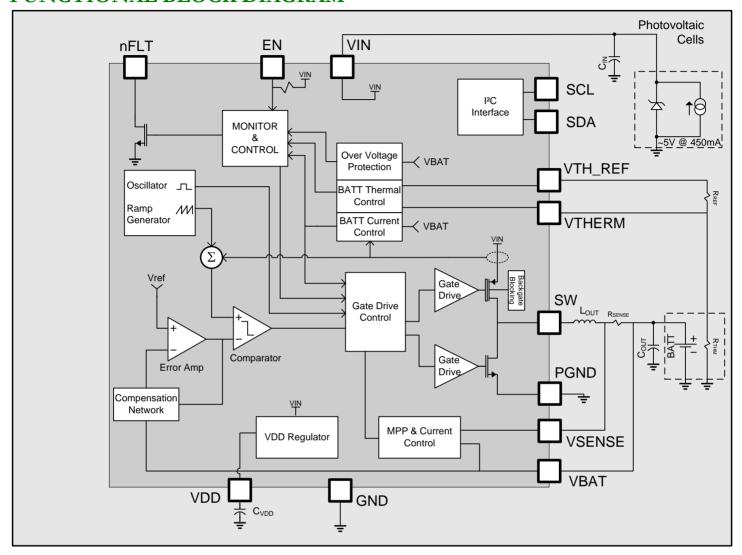


Figure 2: TS52001 Block Diagram



### ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted<sup>(1,2,3)</sup>

Parameter	Range	Unit
VIN, EN, nFLT, SCL, SDA, VTHERM, VTH_REF, VBAT, VSENSE	-0.3 to 8.8	V
SW	-1 to 8.8	V
VDD	-0.3 to 3.6	V
Operating Junction Temperature Range, T <sub>J</sub>	-40 to 125	°C
Storage Temperature Range, T <sub>STG</sub>	-65 to 150	°C
Electrostatic Discharge – Human Body Model	±2k	V
Electrostatic Discharge – Machine Model	+/-200	V
Lead Temperature (soldering, 10 seconds)	260	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$\theta_{JA}$	Thermal Resistance Junction to Air (Note 1)	50	°C/W

Note 1: Assumes 4x4 QFN-16 in 1 in<sup>2</sup> area of 2 oz copper and 25°C ambient temperature.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Тур	Max	Unit
VIN	Photovoltaic Input Operating Voltage	4		8.1	V
R <sub>SENSE</sub>	Sense Resistor		50		mΩ
L <sub>OUT</sub>	Output Filter Inductor Typical Value (Note 1)		4.7		uН
Соит	Output Filter Capacitor Typical Value (Note 2)		4.7		uF
C <sub>OUT-ESR</sub>	Output Filter Capacitor ESR			100	mΩ
$C_{IN}$	Input Supply Bypass Capacitor Value (Note 3)	3.3	10		uF
$C_{\mathrm{VDD}}$	VDD Supply Bypass Capacitor Value (Note 2)	70	100	130	nF
TA	Operating Free Air Temperature	-40		85	°C
$T_{J}$	Operating Junction Temperature	-40		125	°C

Note 1: For best performance, an inductor with a saturation current rating higher than the maximum V<sub>BAT</sub> load requirement plus the inductor current ripple.

<sup>(2)</sup> All voltage values are with respect to network ground terminal.

<sup>(3)</sup> ESD testing is performed according to the respective JESD22 JEDEC standard.

Note 2: For best performance, a low ESR ceramic capacitor should be used.

Note 3: For best performance, a low ESR ceramic capacitor should be used. If C<sub>IN</sub> is not a low ESR ceramic capacitor, a 0.1uF ceramic capacitor should be added in parallel to C<sub>IN</sub>.



## **CHARACTERISTICS**

Electrical Characteristics,  $T_J = -40C$  to 125C, VIN = 5.3V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Тур	Max	Unit
VIN Supply V	Voltage					
VIN	Photovoltaic Voltage Input		4		8.1	V
I <sub>CC-NORM</sub>	Quiescent current Normal Mode	I <sub>LOAD</sub> = 0A, no switching		3		mA
I <sub>CC-DISABLE</sub>	Quiescent current Disable Mode	EN = 0V		10	50	uA
VBAT Leaka	ge		•		•	•
I <sub>BAT-LEAK</sub>	Leakage Current From Batt	$EN = 0V, V_{BAT} = 4.1V$			10	uA
I <sub>BAT-BACK</sub>	Reverse Current	$V_{BAT} > VIN, V_{BAT} = 4.1V, Tj < 85C$			10	uA
	oltage Lockout					•
VIN <sub>-UV</sub>	Input Supply Under-Voltage Threshold	VIN Increasing		3.15		V
VIN <sub>-UV_HYST</sub>	Input Supply Under-Voltage Threshold Hysteresis		100	200		mV
OSC			· ·	L	ı	
Fosc	Oscillator Frequency		0.9	1	1.1	MHz
	Orain Output			11		
I <sub>OH-nFLT</sub>	High-Level Output Leakage	$V_{nFLT} = 5.3V$		0.1		uA
V <sub>OL-nFLT</sub>	Low-Level Output Voltage	$I_{nFLT} = -1mA$			0.4	V
	Input Voltage Thresholds	2.		II.		
V <sub>IH</sub>	High Level Input Voltage		2.2			V
V <sub>IL</sub>	Low Level Input Voltage				0.8	V
V <sub>HYST</sub>	Input Hysteresis			200		mV
I <sub>IN-EN</sub>	Input Leakage	V <sub>EN</sub> =VIN		0.1		uA
IIV EIV	L	$V_{EN}=0V$		-2.0		uA
$I_{\text{IN-SCL}}$	Input Leakage	V <sub>SCL</sub> =VIN		55		uA
-114-361		V <sub>SCL</sub> =0V		-0.1		uA
$I_{IN-SDA}$	Input Leakage	V <sub>SDA</sub> =VIN		0.1		uA
		$V_{SDA}$ = $0V$		-0.1		uA
V <sub>OL-SDA</sub>	Low-Level Output Voltage	$I_{SDA} = -1mA$			0.4	V
Thermal Shu				Т	1	
TSD	Thermal Shutdown Junction		150	170		°C
	Temperature					
$TSD_{HYST}$	TSD Hysteresis			10		°C
Pre-Charge				Т	1	
$V_{PreChg}$	Pre-Charge Voltage Threshold		2.9	3.0	3.1	V
VPC <sub>HYST</sub>	Pre-Charge Voltage Hysteresis			70		mV
Charge Rest						
$V_{ReStart}$	Voltage below termination for charging restart			100		mV
	charging restart			I	l	I



### **CHARGER CHARACTERISTICS**

Electrical Characteristics,  $T_1 = -40C$  to 125C, VIN = 5.3V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Тур	Max	Unit
Charging Regulat	tor: L=4.7uH and C=4.7uF					
I <sub>BAT-FC</sub>	Output Current Limit in Full-Charge Mode	I <sub>BAT</sub> = 1.5A	I <sub>BAT</sub> - 10%	$I_{BAT}$	I <sub>BAT</sub> + 10%	A
$V_{\mathrm{BAT-TO}}$	Termination Voltage in Top-Off Mode	$I_{BAT} = 0.1C, 0C < Tj < 85C$	V <sub>BAT</sub> - 1%	$V_{BAT}$	V <sub>BAT</sub> + 1%	V
$t_{TO}$	Top-Off Mode Time Out		0		120	min
$t_{ t FC}$	Full-Charge Timer		200		1400	min
$t_{acc}$	Timer Accuracy		-10%		+10%	
D	High Side Switch On Resistance	$I_{SW} = -1A$ , $T_J = 25C$		200		mΩ
$R_{DSON}$	Low Side Switch On Resistance	$I_{SW} = 1A, T_J = 25C$		250		mΩ
$I_{BAT}$	Max Output Current			1.5		Α
I <sub>OCD</sub>	Over-Current Detect	HS switch current		2.5		A
$V_{BAT-OV}$	V <sub>BAT</sub> Over-Voltage Threshold		101% V <sub>BAT</sub>	102% V <sub>BAT</sub>	103% V <sub>BAT</sub>	
DUTY <sub>MAX</sub>	Max Duty Cycle			98		%

# I<sup>2</sup>C INTERFACE TIMING REQUIREMENTS

Electrical Characteristics,  $T_1 = -40C$  to 125C, VIN = 5.3V (unless otherwise noted)

Crowled	Downwator	Standa	rd Mode	Fast N	lode <sup>(1)</sup>	II-a-!4
Symbol	Parameter	Min	Max	Min	Max	Unit
$f_{scl}$	I <sup>2</sup> C clock frequency	0	100	0	400	kHz
$t_{sch}$	I <sup>2</sup> C clock high time	4		0.6		μs
$t_{scl}$	I <sup>2</sup> C clock low time	4.7		1.3		μs
$t_{\rm sp}^{(2)}$	I <sup>2</sup> C tolerable spike time	0	50	0	50	ns
$t_{sds}$	I <sup>2</sup> C serial data setup time	250		250		ns
$t_{sdh}$	I <sup>2</sup> C serial data hold time	0		0		μs
$t_{icr}^{(2)}$	I <sup>2</sup> C input rise time		1000		300	ns
$t_{\mathrm{icf}}^{(2)}$	I <sup>2</sup> C input fall time		300		300	ns
$t_{ocf}^{(2)}$	I <sup>2</sup> C output fall time; 10 pF to 400 pF bus		300		300	ns
$t_{buf}$	I <sup>2</sup> C bus free time between Stop and Start	4.7		1.3		μs
$t_{sts}$	I <sup>2</sup> C Start or repeated Start condition setup time	4.7		0.6		μs
$t_{sth}$	I <sup>2</sup> C Start or repeated Start condition hold time	4		0.6		μs
$t_{sps}^{(2)}$	I <sup>2</sup> C Stop condition setup time	4		0.6		μs

<sup>(1)</sup> The I<sup>2</sup>C interface will operate in either standard or fast mode.

<sup>(2)</sup> Parameters not tested in production.



# THERMISTOR CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{ m VTH\_REF}$	VTH_REF output voltage	$I_{VT\_REF} = 2uA-100uA$		1.22		V
10KΩ Temperatu	re Thresholds - β=3434K			_		
0°C	0°C Vtherm Threshold (0°C)	Decreasing Temperature		75.6		%VTH _REF
0°C <sub>HYST</sub>	0°C Vtherm Threshold with Hysteresis (10°C)	Increasing Temperature		66.5		%VTH _REF
10°C	10°C Vtherm Threshold (10°C)	Decreasing Temperature		66.2		%VTH _REF
10°C <sub>HYST</sub>	10°C Vtherm Threshold with Hysteresis (11°C)	Increasing Temperature		65.4		%VTH _REF
45°C	45°C Vtherm Threshold (45°C)	Increasing Temperature		34.5		%VTH _REF
45°C <sub>HYST</sub>	45°C Vtherm Threshold with Hysteresis (44°C)	Decreasing Temperature		35.3		%VTH _REF
50°C	50°C Vtherm Threshold (50°C)	Increasing Temperature		30.8		%VTH _REF
50°C <sub>HYST</sub>	50°C Vtherm Threshold with Hysteresis (49°C)	Decreasing Temperature		31.5		%VTH _REF
60°C	60°C Vtherm Threshold (60°C)	Increasing Temperature		24.9		%VTH _REF
60°C <sub>HYST</sub>	60°C Vtherm Threshold with Hysteresis (50°C)	Decreasing Temperature		30.8		%VTH _REF
100KΩ Temperat	ure Thresholds - β=4311K					
0°C	0°C Vtherm Threshold (0°C)	Decreasing Temperature		80.5		%VTH _REF
0°C <sub>HYST</sub>	0°C Vtherm Threshold with Hysteresis (10°C)	Increasing Temperature		69.8		%VTH _REF
10°C	10°C Vtherm Threshold (10°C)	Decreasing Temperature		69.8		%VTH _REF
10°C <sub>HYST</sub>	10°C Vtherm Threshold with Hysteresis (11°C)	Increasing Temperature		68.6		%VTH _REF
45°C	45°C Vtherm Threshold (45°C)	Increasing Temperature		31.3		%VTH _REF
45°C <sub>HYST</sub>	45°C Vtherm Threshold with Hysteresis (44°C)	Decreasing Temperature		32.3		%VTH _REF
50°C	50°C Vtherm Threshold (50°C)	Increasing Temperature		27.0		%VTH _REF
50°C <sub>HYST</sub>	50°C Vtherm Threshold with Hysteresis (49°C)	Decreasing Temperature		27.8		%VTH _REF
60°C	60°C Vtherm Threshold (60°C)	Increasing Temperature		19.4		%VTH _REF
60°C <sub>HYST</sub>	60°C Vtherm Threshold with Hysteresis (50°C)	Decreasing Temperature		27.0		%VTH _REF



#### **FUNCTIONAL DESCRIPTION**

The TS52001 is a fully-integrated Li-Ion battery charger IC based on a highly-efficient switching topology. It includes a Maximum Power Point Tracking (MPPT) function to optimize its input voltage to extract the maximum possible power from a photovoltaic cell. It includes configurability for termination voltage, charge current and a host of other variables to allow optimum charging conditions for a wide range of Li-Ion batteries. A 1 MHz internal switching frequency facilitates low-cost LC filter combinations.

When the battery voltage is below 3.0 volts, the device will enter a pre-charge state and apply a small, programmable charge current to safely charge the battery to a level for which full charge current can be applied. Once the full charge mode has been initiated, the device will maximize available charge current to the battery by adjusting its duty cycle to regulate its input voltage to the Maximum Power Point (MPP) voltage of the photovoltaic cell. If sufficient current is available from the PV cell to exceed the safe 1C charge rate of the battery, then the programmable 1C current limit function will take precedence over the MPP control function and the PV cell voltage will rise above the MPP value.

When the battery voltage has increased enough to go into maintenance mode, the PWM control loop will force a constant voltage across the battery. Once in constant voltage mode, current is monitored to determine when the battery is fully charged. This regulation voltage as well as the 1C charging current can be set to change based on battery temperature. There are 4 temperature ranges where these can be set independently, 0-10°C, 10-45°C, 45-50°C and 50-60°C. The 0°C and 60°C thresholds will stop charging and have 10 degrees of hysteresis. The intermediate points have 1 degree of hysteresis.

### INTERNAL PROTECTION DETAILS

#### **Internal Current Limit**

The current through the inductor is sensed on a cycle by cycle basis and if current limit is reached, it will abbreviate the cycle. Current limit is always active when the regulator is enabled.

#### **Thermal Shutdown**

If the temperature of the die exceeds 170°C (typical), the SW outputs will tri-state to protect the device from damage. The nFLT and all other protection circuitry will stay active to inform the system of the failure mode. Once the device cools to 160°C (typical), the device will attempt to start up again. If the device reaches 170°C, the shutdown/restart sequence will repeat.

### **VIN Under-Voltage Lockout**

The device is held in the off state until VIN reaches 3.15V. There is a 200mV hysteresis on this input, which requires the input to fall below 2.95V before the device will disable.

#### **Battery Over-Voltage Protection**

The TS52001 has a battery protection circuit designed to shutdown the charging profile if the battery voltage is greater than the termination voltage. The termination voltage can change based on user programming, so the protection threshold is set to 2% above the termination voltage. Shutting down the charging profile puts the TS52001 in a fault condition.

#### **FAULT HANDLING**

#### nFLT Pin Functionality

In the event of a battery over-voltage, the battery temperature being outside of the safe charging range or the full charge timer expiring, charging will stop, and the nFLT pin will be pulled low. When the fault condition is no longer present, the device will enter the INITIALIZE state, but the nFLT pin will remain low until register 0 is read. When the register 0 is read, the nFLT pin will go high until a new fault is detected.

#### **Other Faults**

When an open thermistor, thermal shut down, VIN under-voltage, or top off time-out are detected, charging will immediately stop and the corresponding bit in register 0 will be set. The device will enter the INITIALIZE state until the fault is no longer detected.



### SERIAL INTERFACE

The TS52001 features an I²C slave interface which offers advanced control and diagnostic features. I²C operation offers configuration control for termination voltages, charge currents, and charge timeouts. This configurability allows for optimum charging conditions in a wide range of Li-Ion batteries. I²C operation also offers fault and warning indicators. Whenever a fault is detected, the associated status bit in the STATUS register is set and the nFLT pin is pulled low. Whenever a warning is detected, the associated status bit in the STATUS register is set, but the nFLT pin is not pulled low. Reading of the STATUS register resets the fault and warning status bits, and the nFLT pin is released after all fault status bits have been reset.

### I<sup>2</sup>C SUBADDRESS DEFINITION

	Slave Adress + R/nW				Subaddress					Data																		
Start	G3	G2	G1	G0	A2	A1	A0	R/nW	ACK	<b>S7</b>	<b>S6</b>	<b>S</b> 5	<b>S4</b>	<b>S3</b>	<b>S2</b>	<b>S1</b>	S0	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK	Stop
									•																			
										-																		

Start - Start Condition

G(3:0) - Group ID: Address fixed at 1001b A(2:0) - Device ID: Address fixed at 000b R/nW - Read / not Write select bit ACK - Acknowledge

S(7:0) - Subaddress: Defined per the address register map

D(7:0) - Data: Data to be transmitted with the device

Stop - Stop Condition

Figure 3: Sub-address in I<sup>2</sup>C Transmission

### I<sup>2</sup>C BUS OPERATION

The TS52001 has a slave I<sup>2</sup>C interface that supports standard and fast mode data rates, auto-sequencing, and is compliant to I<sup>2</sup>C standard version 3.0.

I<sup>2</sup>C is a two-wire serial interface where the two lines are serial clock (SCL) and serial data (SDA). SDA must be connected to a positive supply through an external pull-up resistor. The devices communicating on this bus can drive the SDA line low or release it to high impedance. The device that initiates the I<sup>2</sup>C transaction becomes the master of the bus. Communication is initiated by the master sending a Start condition, a high-to-low transition on SDA, while the SCL line is high. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/nW). After receiving the valid address byte, the device responds with an acknowledge (ACK). An ACK is a low on SDA during the high of the ACK related clock pulse. On the I<sup>2</sup>C bus, during each clock pulse only one data bit is transferred. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as Start or Stop control commands. A low-to-high transition on SDA while the SCL input is high, indicates a Stop condition and is sent by the master (see Figure 4).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The SDA line must be released by the transmitter before the receiver can send an ACK bit. The receiver that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. To ensure proper operation, setup and hold times must be met. An end of data is signaled by the master receiver to the slave transmitter by not generating an acknowledge after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. The transmitter must then release the data line to enable the master to generate a Stop condition.

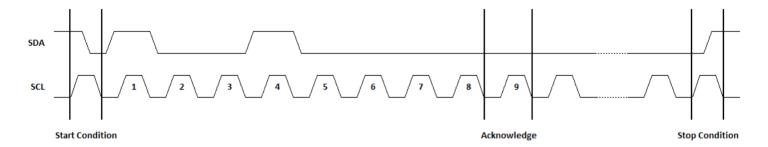


Figure 4: I<sup>2</sup>C Start / Stop Protocol

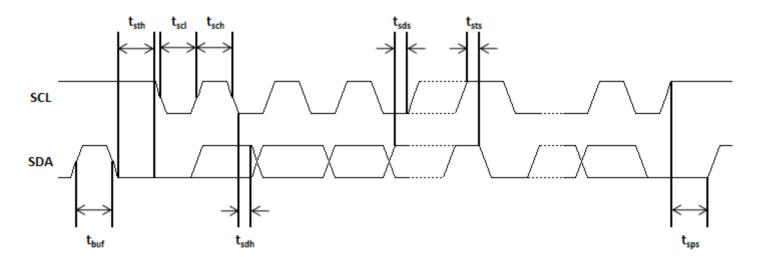
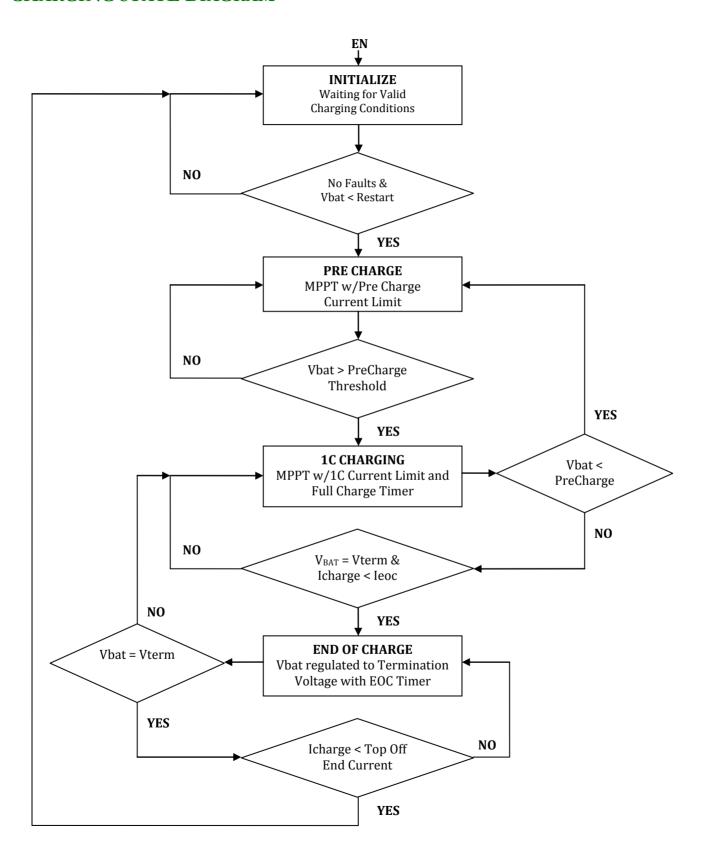


Figure 5: I<sup>2</sup>C Data Transmission Timing

### CHARGING STATE DIAGRAM





REGISTER DESCRIPTION (Device Address = 0x48)

REGISTER	ADDRESS (HEX)	NAME	DEFAULT	DESCRIPTION
0	00	STATUS	0x00	Status bit register
1	N/A	N/A	N/A	Register not implemented
2	02	CONFIG1(1)	EEPROM	Configuration register
3	03 CONFIG2 <sup>(1)</sup> EEPROM		Configuration register	
4	04	CONFIG3(1)	EEPROM	Configuration register
5	05	CONFIG4(1)	EEPROM	Configuration register
6	06	CONFIG5(1)	EEPROM	Configuration register
7-16	N/A	N/A	N/A	Registers not implemented
17	11	CONFIG_ENABLE	0x00	Enable configuration register access
18	12	EEPROM_CTRL <sup>(1)</sup>	0x00	EEprom control register

<sup>(1)</sup> CONFIG and EEPROM\_CTRL registers are only accessible when CONFIG\_ENABLE register is written.

## **STATUS REGISTER (STATUS)**

Address - 0x00h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	BATT_OV	1C_TO	TEMP_0C	TEMP_60C	TSD	TOP_TO	VIN_UV	TH_OPEN
READ/WRITE	R	R	R	R	R	R	R	R

FIELD NAME	BIT DEFINITION <sup>(2)</sup>							
BATT_OV	Battery over-voltage							
1C_T0	Full charge timer has timed out							
TEMP_0C	OC Thermistor indicates battery temperature < 0°C							
TEMP_60C	Thermistor indicates battery temperature > 60°C							
TSD	Thermal shutdown							
TOP_TO	Top Off timer has timed out							
VIN_UV	VIN under-voltage							
TH_OPEN	Thermistor Open (battery not present)							

<sup>(1)</sup> Faults are defined as BATT\_OV, 1C\_TO, TEMP\_OC, and TEMP\_60C. Warnings are defined as TSD, TOP\_TO, VIN\_UV, and TH\_OPEN. Faults cause the nFLT pin to be pulled low, Warnings do not cause the nFLT pin to be pulled low. All status bits are cleared after register read access. nFLT pin will go high impedance (open drain output) after the status register has been read and all status bits have been reset.



# **CONFIGURATION REGISTER (CONFIG1)**

Address - 0x02h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	PRE_CHRG[1:0]		V_TERM_0_10[2:0]			V_TERM_10_45[2:0]		
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FIELD NAME	BIT DEFINITION
PRE_CHRG[1:0] <sup>(1)</sup>	Pre-Charging configuration
	00 – 50 mA
	01 – 100 mA
	10 – 185 mA
	11 – 370 mA
V_TERM_0_10[2:0] <sup>(2)</sup>	Voltage Termination 0-10°C configuration
	000 – 3.94 V
	001 – 4.00 V
	010 – 4.05 V
	011 – 4.10 V
	100 – 4.12 V
	101 – 4.15 V
	110 – 4.18 V
	111 - Invalid Setting
V_TERM_10_45[2:0] <sup>(2)</sup>	Voltage Termination 10-45°C configuration
	000 – 3.94 V
	001 – 4.00 V
	010 – 4.05 V
	011 – 4.10 V
	100 – 4.12 V
	101 – 4.15 V
	110 – 4.18 V
	111 - Invalid Setting

<sup>(1)</sup> PRE\_CHRG Note: Maximum output current when  $V_{BAT} < 3.0 \text{ V}$ .

<sup>(2)</sup> V\_TERM Note: Unique settings available for battery temperatures 0-10°C, 10-45°C, 45-50°C, and 50-60°C. For <0°C and >60°C, charging is disabled and a fault is set.



# **CONFIGURATION REGISTER (CONFIG2)**

Address - 0x03h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	EOC[1:0]		V_TERM_45_50[2:0]			V_TERM_50_60[2:0]		
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FIELD NAME	BIT DEFINITION
EOC[1:0] <sup>(1)</sup>	End of charge configuration
	00 – 50 mA
	01 – 100 mA
	10 – 185 mA
	11 – 370 mA
V_TERM_45_50[2:0] <sup>(2)</sup>	Voltage Termination 45-50°C configuration
	000 – 3.94 V
	001 – 4.00 V
	010 - 4.05 V
	011 - 4.10 V
	100 – 4.12 V
	101 – 4.15 V
	110 – 4.18 V
	111 - Invalid Setting
V_TERM_50_60[2:0] <sup>(2)</sup>	Voltage Termination 50-60°C configuration
	000 – 3.94 V
	001 – 4.00 V
	010 - 4.05 V
	011 - 4.10 V
	100 – 4.12 V
	101 – 4.15 V
	110 – 4.18 V
	111 - Invalid Setting

<sup>(1)</sup> EOC Note: Maximum output current when  $V_{BAT} < 3.0 \text{ V}$ .

<sup>(2)</sup> V\_TERM Note: Unique settings available for battery temperatures 0-10°C, 10-45°C, 45-50°C, and 50-60°C. For <0°C and >60°C, charging is disabled and a fault is set.



# **CONFIGURATION REGISTER (CONFIG3)**

Address - 0x04h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	MAX_CHRG_CURR_0_10[3:0]			MAX_CHRG_CURR_10_45[3:0]				
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FIELD NAME	BIT DEFINITION
MAX_CHRG_CURR_0_10[3:0] <sup>(1)</sup>	Maximum charge current 0-10°C configuration
	0000 – 50 mA
	0001 – 100 mA
	0010 – 200 mA
	0011 – 300 mA
	0100 – 400 mA
	0101 – 500 mA
	0110 - 600 mA
	0111 – 700 mA
	1000 – 800 mA
	1001 – 900 mA
	1010 – 1000 mA
	1011 – 1100 mA
	1100 – 1200 mA
	1101 – 1300 mA
	1110 – 1400 mA
	1111 – 1500 mA
MAX_CHRG_CURR_10_45[3:0] <sup>(1)</sup>	Maximum charge current 10-45°C configuration
	0000 – 50 mA
	0001 – 100 mA
	0010 – 200 mA
	0011 - 300 mA
	0100 – 400 mA
	0101 – 500 mA
	0110 - 600 mA
	0111 - 700 mA
	1000 – 800 mA
	1001 – 900 mA
	1010 – 1000 mA 1011 – 1100 mA
	1101 – 1100 mA 1100 – 1200 mA
	1100 - 1200 mA 1101 - 1300 mA
	1101 – 1300 mA 1110 – 1400 mA
	1110 - 1400 mA 1111 - 1500 mA
	1111 – 1300 IIIA

<sup>(1)</sup> MAX\_CHRG\_CURR Note: Unique settings available for battery temperatures 0-10°C, 10-45°C, 45-50°C, and 50-60°C. For <0°C and >60°C, charging is disabled and a fault is set.



# **CONFIGURATION REGISTER (CONFIG4)**

Address - 0x05h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0	
FIELD NAME	MAX_CHRG_CURR_45_50[3:0]				MAX_CHRG_CURR_50_60[3:0]				
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

FIELD NAME	BIT DEFINITION
MAX_CHRG_CURR_45_50[3:0] <sup>(1)</sup>	Maximum charge current 45-50°C configuration
	0000 – 50 mA
	0001 – 100 mA
	0010 – 200 mA
	0011 – 300 mA
	0100 – 400 mA
	0101 – 500 mA
	0110 - 600 mA
	0111 - 700 mA
	1000 – 800 mA
	1001 – 900 mA
	1010 – 1000 mA
	1011 – 1100 mA
	1100 – 1200 mA
	1101 – 1300 mA
	1110 – 1400 mA
	1111 – 1500 mA
MAX_CHRG_CURR_50_60[3:0] <sup>(1)</sup>	Maximum charge current 50-60°C configuration
	0000 – 50 mA
	0001 – 100 mA
	0010 – 200 mA
	0011 - 300 mA
	0100 – 400 mA
	0101 - 500 mA
	0110 - 600 mA
	0111 - 700 mA
	1000 – 800 mA
	1001 – 900 mA
	1010 – 1000 mA 1011 – 1100 mA
	1100 – 1200 mA 1101 – 1300 mA
	1101 - 1300 mA 1110 - 1400 mA
	1111 – 1500 mA

<sup>(1)</sup> MAX\_CHRG\_CURR Note: Unique settings available for battery temperatures 0-10°C, 10-45°C, 45-50°C, and 50-60°C. For <0°C and >60°C, charging is disabled and a fault is set.



# **CONFIGURATION REGISTER (CONFIG5)**

Address - 0x06h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0	
FIELD NAME	TOP_END	TH	TOP_TO[2:0]			1C_TO[2:0]			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

FIELD NAME	BIT DEFINITION				
TOP_END <sup>(1)</sup>	Top Off end configuration				
	0 – 25 mA				
	1 – 92 mA				
TH <sup>(2)</sup>	Thermistor configuration				
	0 - 10k Ohms				
	1 – 100k Ohms				
TOP_TO[2:0] <sup>(3)</sup>	Top Off timer time out configuration				
	000 – 0 minutes				
	001 – 20 minutes				
	010 – 40 minutes				
	011 – 60 minutes				
	100 – 80 minutes				
	101 – 100 minutes				
	110 – 120 minutes				
	111 - Disable time out timer				
1C_TO[2:0] <sup>(4)</sup>	Full charge timer time out configuration				
	000 – Disable full charge timer				
	001 – 200 minutes				
	010 – 400 minutes				
	011 – 600 minutes				
	100 – 800 minutes				
	101 – 1000 minutes				
	110 – 1200 minutes				
	111 – 1400 minutes				

<sup>(1)</sup> TOP\_END Note: Charging stops when  $V_{BAT} = V_{termination}$  and  $I_{BAT} < Top$  Off end.

<sup>(2)</sup> TH Note: Setting for nominal thermistor and reference resistor value.

<sup>(3)</sup> TOP\_TO Note: Timer starts when  $V_{BAT} = V_{termination}$  and  $I_{BAT} < EOC$ .

<sup>(4) 1</sup>C\_TO Note: Timer starts when  $V_{BAT} > 3.0V$ .



## ENABLE CONFIGURATION REGISTER (CONFIG\_ENABLE)

Address - 0x11h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	EN_CFG						
READ/WRITE	R	R	R	R	R	R	R	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
EN_CFG	Enable access control bit for configuration registers 2-6
	0 – Disable access
	1 – Enable access

## EEPROM CONTROL REGISTER (EEPROM\_CTRL)

Address - 0x12h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	EE_PROG						
READ/WRITE	R	R	R	R	R	R	R	R/W
RESET VALUE	0	0	0	0	0	0	0	0

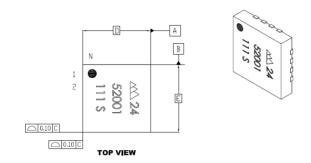
FIELD NAME	BIT DEFINITION			
EE_PROG <sup>(1)</sup>	EEprom program control bit for configuration registers 2-6			
	0 – Disable EEprom programming			
	1 – Enable EEprom programming with data from configuration registers 2-6			

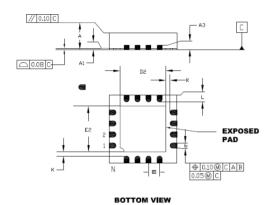
<sup>(1)</sup> EE\_PROG Note: Inputs VIN and EN must be present for 200 ms.

### EXTERNAL COMPONENT SELECTION

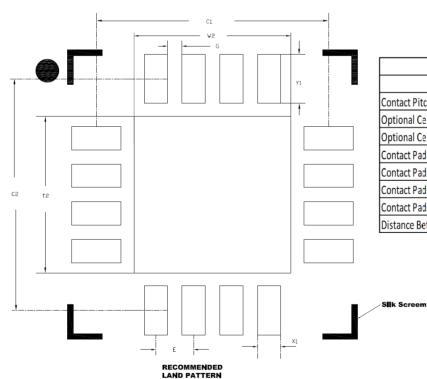
The internal compensation is optimized for a 4.7uF output capacitor and a 4.7uH inductor. To keep the output ripple low, a low ESR (less than 35mOhm) ceramic is recommended.

# PACKAGE MECHANICAL DRAWINGS





		Units	N	/ILLIMETER	S
	Dimensi	ons Limits	MIN	NOM	MAX
Number of Pins		N		16	
Pitch		е	0.65 BSC		
Overall Height		А	0.80	0.90	1.00
Standoff		A1	0.00	0.02	0.05
Contact Thickness		А3		0.20 REF	
Overall Length		D	4.00 BSC		
Exposed Pad Width		E2	2.55	2.70	2.80
Overall Width		Ε	4.00 BSC		
Exposed Pad Length		D2	2.55	2.70	2.80
Contact Width		b	0.25	0.30	0.35
Contact Length		L	0.30	0.40	0.50
Contact-to-Exposed Pad		К	0.20	-	-



Units		MILLIMETERS			
Dimension Limits		MIN	NOM	MAX	
Contact Pitch	Е	0.65 BSC			
Optional Center Pad Width	W2	-	-	2.70	
Optional Center Pad Length	T2	-	-	2.70	
Contact Pad Spacing	C1	-	4.00	-	
Contact Pad Spacing	C2	-	4.00	-	
Contact Pad Width (X16)	X1	-	-	0.40	
Contact Pad Length (X16)	Y1	-	-	0.85	
Distance Between Pads	G	0.25	-	-	

#### Notes:

Dimensions and tolerancing per ASME Y14,5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

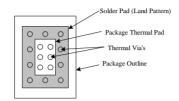
REF: Refernce Dimension, usually without tolerance, for information only.



### APPLICATION USING A MULTI-LAYER PCB

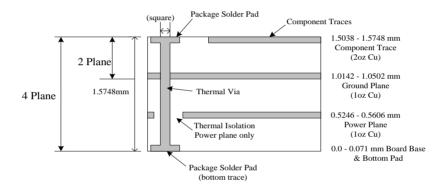
To maximize the efficiency of this package for application on a single layer or multi-layer PCB, certain guidelines must be followed when laying out this part on the PCB.

The following are guidelines for mounting the exposed pad IC on a Multi-Layer PCB with ground a plane.



Package and PCB Land Configuration For a Multi-Layer PCB

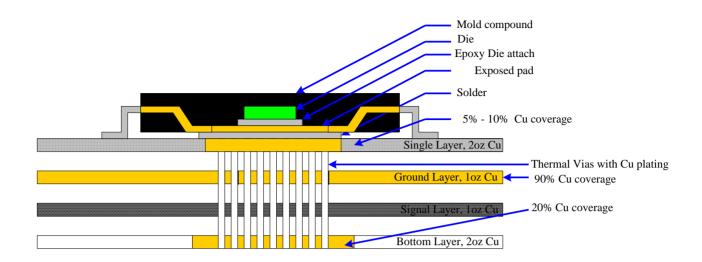
#### IEDEC standard FR4 PCB Cross-section:



Multi-Layer Board (Cross-sectional View)

In a multi-layer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors, including die area, number of thermal vias, thickness of copper, etc.

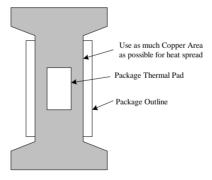




Note: NOT to Scale

The above drawing is a representation of how the heat can be conducted away from the die using an exposed pad package. Each application will have different requirements and limitations and therefore the user should use sufficient copper to dissipate the power in the system. The output current rating for the linear regulators may have to be de-rated for ambient temperatures above 85C. The de-rate value will depend on calculated worst case power dissipation and the thermal management implementation in the application.

### APPLICATION USING A SINGLE LAYER PCB



Layout recommendations for a Single Layer PCB: utilize as much Copper Area for Power Management. In a single layer board application the thermal pad is attached to a heat spreader (copper areas) by using low thermal impedance attachment method (solder paste or thermal conductive epoxy).

In both of the methods mentioned above it is advisable to use as much copper traces as possible to dissipate the heat.

### **IMPORTANT:**

If the attachment method is NOT implemented correctly, the functionality of the product is not guaranteed. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.



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