RFMD2081

45MHz TO 2700MHz IQ MODULATOR WITH SYNTHESIZER/VCO

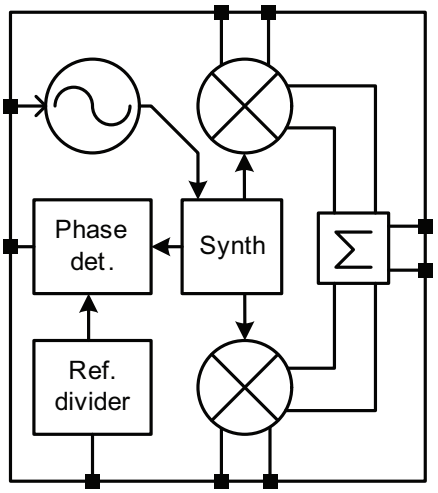
Package: QFN, 32-Pin, 5mm x 5mm

Features

- RF Output Frequency Range 45MHz to 2700MHz
- Fractional-N Synthesizer with Very Low Spurious Levels
- Typical Step Size 1.5Hz
- Fully Integrated Wideband VCOs and LO Buffers
- Integrated Phase Noise <0.2° rms at 1GHz
- -40dBc Unadjusted Carrier Suppression
- -40dBc Unadjusted Sideband Suppression
- 100MHz Baseband Input 3dB Bandwidth
- Very Low Noise Floor -162dBm/Hz Typical
- Output P1dB + 4dBm
- Output IP3 + 17dBm
- 2.7V to 3.3V Power Supply
- 135mA Typical Current Consumption
- Serial Programming Interface

Applications

- Satellite Communications
- QPSK/QAM Modulators
- Wireless Broadband
- Point-to-Point
- Software Defined Radios



Functional Block Diagram

Product Description

The RFMD2081 is a low power, wideband, IQ modulator with integrated fractional-N synthesizer and voltage controlled oscillator (VCO). The modulator features an input 3dB bandwidth of 100MHz, and can generate output frequencies of between 45MHz and 2700MHz, making it suitable for a wide range of applications.

The fractional-N synthesizer takes advantage of an advanced sigma-delta architecture that delivers ultra-fine step sizes and low spurious products. The synthesizer/VCO, combined with an external loop filter, allows the user to generate local oscillator (LO) signals from 90MHz to 5400MHz. The LO signal is buffered and routed to a high accuracy quadrature divider (/2) that drives the balanced I and Q mixers. The output of the mixers are summed and applied to a differential RF output stage. This device also features a differential input for an external VCO or LO source.

Device programming is achieved via a simple 3-wire serial interface. In addition, a unique programming mode allows up to four devices to be controlled from a common serial bus. This eliminates the need for separate chip-select control lines between each device and the host controller. Up to six general purpose outputs are provided, which can be used to access internal signals (the LOCK signal, for example) or to control front end components. The device is optimized for low power operation, consuming typically only 135mA from a 3V supply.

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{DD})	-0.5 to +3.6	V
Input Voltage (V_{IN}), any pin	-0.3 to V_{DD} +0.3	V
LO Input Power	+15	dBm
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000 ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
ESD Requirements					
Human Body Model	2000			V	DC Pins
	1500			V	All Pins
Charge Device Model	1000			V	All Pins
Operating Conditions					
Supply Voltage (V_{DD})	2.7		3.3	V	
Temperature	-40		+85	°C	
Logic Inputs/Outputs (V_{DD} = Supply to DIG_VDD pin)					
Input Low voltage	-0.3		+0.5	V	
Input High voltage	V_{DD} / 1.5		V_{DD}	V	
Input Low current	-10		+10	µA	Input = 0V
Input High current	-10		+10	µA	Input = V_{DD}
Output Low voltage	0		0.2*V_{DD}	V	
Output High voltage	0.8*V_{DD}		V_{DD}	V	
Load Resistance	10			kΩ	
Load Capacitance			20	pF	
GPO Drive Capability					
Sink Current		20		mA	At V_{OL} = +0.6V
Source Current		20		mA	At V_{OL} = +2.4V
Output Impedance		25		Ω	
Static					
Supply Current (I_{DD})		135		mA	1.3V Input DC Bias
Standby			2	mA	Reference Oscillator and Bandgap Only
Power Down Current			300	µA	ENBL = 0 and REF_STBY = 0

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Modulator (Output driving 4:1 balun)					
I & Q Input 3dB Bandwidth		100		MHz	
I & Q Input Voltage		1		V_{P-P}	Differential with 1.3V Input DC Bias
Output Power		-4		dBm	
Output Noise Floor		-162		dBm/Hz	At 10MHz Offset with 1.3V Input DC Bias
Output IP3		+17		dBm	1.3V Input DC Bias
Output P1dB		+4		dBm	1.3V Input DC Bias
Carrier Suppression		-40		dBc	Unadjusted
Carrier Suppression		-50		dBc	Input DC Bias Offset Adjusted
Sideband Suppression		-40		dBc	Unadjusted
Output Port Center Frequency Range	45		2700	MHz	
Reference Oscillator					
External Reference Frequency	10		104	MHz	
Reference Divider Ratio	1		7		
External Reference Input Level	500	800	1500	mV_{P-P}	AC-coupled
Synthesizer (PLL closed loop, 52MHz reference)					
Synthesizer Output frequency	90		5400	MHz	
Phase Detector Frequency			52	MHz	
Phase Noise, LO=1GHz		-108		dBc/Hz	10kHz Offset
		-108		dBc/Hz	100kHz Offset
		-135		dBc/Hz	1MHz Offset
		0.19		Deg	RMS Integrated from 1KHz to 40MHz
Phase Noise, LO=2GHz		-102		dBc/Hz	10kHz Offset
		-102		dBc/Hz	100kHz Offset
		-130		dBc/Hz	1MHz Offset
		0.32		Deg	RMS Integrated from 1KHz to 40MHz
Normalized phase noise floor		-214		dBc/Hz	Measured at 20kHz to 30kHz Offset
Voltage Controlled Oscillator					
Open Loop Phase Noise at 1MHz Offset					
2.5GHz LO Frequency		-134		dBc/Hz	VCO3, LO Divide by 2
2.0GHz LO Frequency		-135		dBc/Hz	VCO2, LO Divide by 2
1.5GHz LO Frequency		-136		dBc/Hz	VCO1, LO Divide by 2
Open loop phase noise at 10MHz offset					
2.5GHz LO Frequency		-149		dBc/Hz	VCO3, LO Divide by 2
2.0GHz LO Frequency		-150		dBc/Hz	VCO2, LO Divide by 2
1.5GHz LO Frequency		-151		dBc/Hz	VCO1, LO Divide by 2
External LO Input					
LO Input Frequency Range	90		5400	MHz	
External LO Input Level		0		dBm	Driven from 50Ω source via a 1:1 balun

Pin Names and Descriptions

Pin	Name	Description
1	ENBL/GPO5	Device Enable pin (see note 1 and 2).
2	EXT_LO	External local oscillator input. Use AC coupling capacitor.
3	EXT_LO_DEC	Decoupling pin for external local oscillator. Use AC coupling capacitor.
4	REXT	External bandgap bias resistor (see note 3).
5	ANA_VDD1	Analog supply. Use good RF decoupling.
6	LFILT1	Phase detector output. Low-frequency noise-sensitive node.
7	LFILT2	Loop filter op-amp output. Low-frequency noise-sensitive node.
8	LFILT3	VCO control input. Low-frequency noise-sensitive node.
9	MODE/GPO6	Mode select pin (see notes 1 and 2).
10	REF_IN	Reference input. Use AC coupling capacitor.
11	NC	
12	TM	Connect to ground.
13	RF_OUT_N	Differential output (see note 5).
14	RF_OUT_P	Differential output (see note 5).
15	GPO1/ADD1	General purpose output / MultiSlice address bit.
16	GPO2/ADD2	General purpose output / MultiSlice address bit.
17	DIG_VDD	Digital supply. Should be decoupled as close to the pin as possible.
18	MOD_Q_N	Modulator Q differential input (see note 4).
19	MOD_Q_P	Modulator Q differential input (see note 4).
20	NC	
21	NC	
22	MOD_I_N	Modulator I differential input (see note 4).
23	MOD_I_P	Modulator I differential input (see note 4).
24	ANA_VDD2	Analog supply. Use good RF decoupling.
25	GPO3	General purpose output
26	GPO4/LD/DO	General purpose output / Lock detect output / serial data out.
27	NC	
28	NC	
29	RESETX	Chip reset (active low). Connect to DIG_VDD if asynchronous reset is not required.
30	ENX	Serial interface select (active low) (See note 1).
31	SCLK	Serial interface clock (See note 1).
32	SDATA	Serial interface data (See note 1).
Exposed Paddle		Ground reference, should be connected to PCB ground through a low impedance path.

Notes:

1. An RC low pass filter may be used on this line to reduce digital noise.
2. If the device is under software control this input can be configured as a general purpose output (GPO).
3. Connect a 51KΩ resistor from this pin to ground. This pin is sensitive to low frequency noise injection.
4. DC bias voltage and modulation should be applied to this pin.
5. This pin must be connected to ANA_VDD2 using an RF choke or center tapped transformer (see application schematic).

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Theory of Operation

The RFMD2081 is a wideband IQ modulator with integrated fractional-N synthesizer and a low noise VCO core. It features a high accuracy LO quadrature divider followed by buffer circuits which drive the I and Q mixers of the modulator with the quadrature LO signals. The RFMD2081 has an integrated voltage reference and low drop out regulators supplying critical circuit blocks such as the VCOs and synthesizer. Synthesizer programming, device configuration and control are achieved through a mixture of hardware and software controls. All on-chip registers are programmed through a simple three-wire serial interface.

VCO

The VCO core in the RFMD2081 consists of three VCOs which, in conjunction with the integrated LO dividers of /1 to /32, cover the frequency range of 90MHz to 5400MHz. The modulator quadrature divider provides a further fixed divide by two to give the center frequency range at the modulator output of 45MHz to 2700MHz.

Each VCO has 128 overlapping bands which are used to achieve low VCO gain and optimal phase noise performance across the whole tuning range. The chip automatically selects the correct VCO (VCO auto-select) and the correct VCO band (VCO coarse tuning) to generate the desired LO frequency based on the values programmed into the PLL1 and PLL2 registers banks.

The VCO auto-select and VCO coarse tuning are triggered every time ENBL is taken high, or if the PLL re-lock self clearing bit is programmed high. Once the correct VCO and band have been selected the PLL will lock onto the correct frequency. During the band selection process fixed capacitance elements are progressively connected to the VCO resonant circuit until the VCO is oscillating at approximately the correct frequency. The output of this band selection, CT_CAL, is made available in the read-back register. A value of 127 or 0 in this register indicates that the coarse tuning was unsuccessful, and this should also be indicated by the CT_FAILED flag also available in the read-back register. A value between 1 and 126 indicates a successful calibration, the actual value being dependent on the desired frequency as well as process variation for a particular device.

The band select process will center the VCO tuning voltage at about 0.8V, compensating for manufacturing tolerances and process variation as well as environmental factors including temperature. In applications where the device is left enabled at the same LO frequency for some time it is recommended that automatic band selection be performed for every 30°C change in temperature. This assumes an active loop filter.

The RFMD2081 features a differential LO input to allow the mixer to be driven from an external LO source. The fractional-N PLL can be used with an external VCO driven into this LO input, which may be useful to reduce phase noise in some applications. This may also require an external op-amp, dependant on the tuning voltage required by the external VCO.

Fractional-N PLL

The RFMD2081 contains a charge-pump based fractional-N phase locked loop (PLL) for controlling the three VCOs. The PLL includes automatic calibration systems to counteract the effects of process and environmental variations, ensuring repeatable loop response and phase noise performance. As well as the VCO auto-select and coarse tuning, there is a loop filter calibration mechanism which can be enabled if required. This operates by adjusting the charge pump current to maintain loop bandwidth. This can be useful for applications where the LO is tuned over a wide frequency range.

The PLL has been designed to use a reference frequency of between 10MHz and 104MHz from an external source, which is typically a temperature controlled crystal oscillator (TCXO). A reference divider (divide by 1 to divide by 7) is supplied and should be programmed to limit the frequency at the phase detector to a maximum of 52MHz.

Two PLL programming banks are provided, the first bank is preceded by the label PLL1 and the second bank is preceded by the label PLL2. The active register bank is selected by the state of the MODE pin, low for PLL1 and high for PLL2.

The VCO outputs are first divided down in a high frequency prescalar. The output of this high frequency prescalar then enters the N divider, which is a fractional divider containing a dual-modulus prescalar and a digitally spur-compensated fractional sequence generator. This allows very fine frequency steps and minimizes fractional spurs. The fractional energy is randomized and appears as fractional noise at frequency offsets above 100kHz which will be attenuated by the loop filter. An external loop filter is used, giving flexibility in setting loop bandwidth for optimizing phase noise and lock time for example.

The synthesizer step size is typically 1.5Hz when using a 26MHz reference frequency. The exact step size for any reference and LO frequency can be calculated using the following formula:

$$(F_{REF} * P) / (R * 2^{24} * LO\_DIV*2)$$

Where F_{REF} is the reference frequency, R is the reference division ratio, P is the prescalar division ratio, and LO_DIV is the LO divider value.

Pin 26 (GPO4) can be configured as a lock detect pin. The lock status is also available in the read-back register. The lock detect function is a window detector on the VCO tuning voltage. The lock flag will be high to show PLL lock which corresponds to the VCO tuning voltage being within the specified range, typically 0.30V to 1.25V.

The lock time of the PLL will depend on a number of factors; including the loop bandwidth and the reference frequency at the phase detector. This clock frequency determines the speed at which the state machine and internal calibrations run. A 52MHz phase detector frequency will give fastest lock times, of typically <50μsecs when using the PLL re-lock bit.

Phase Detector and Charge Pump

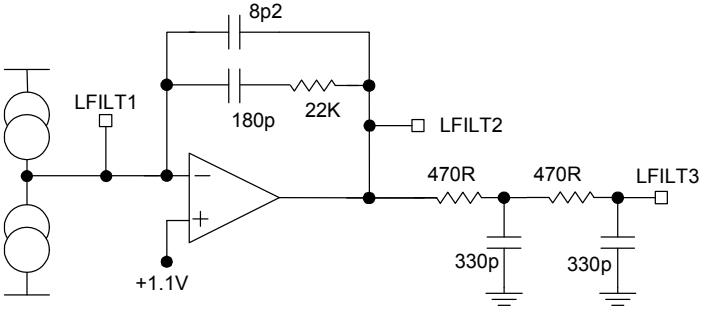
The phase detector provides a current output to drive an active loop filter. The charge pump output current is set by the value contained in the P1_CP_DEF and P2_CP_DEF fields in the loop filter configuration register. The charge pump current is given by approximately 3μA/bit, and the fields are 6 bits long. This gives default value (31) of 93μA and maximum value (63) of 189μA.

If the automatic loop bandwidth calibration is enabled the charge pump current is set by the calibration algorithm based upon the VCO gain.

The phase detector will operate with a maximum input frequency of 52MHz.

Loop Filter

The active loop filter is implemented using the on-chip low noise op-amp, with external resistors and capacitors. The op-amp gives a tuning voltage range of typically +0.1V to +2.4V. The internal configuration of the chip is shown below with the recommended active loop filter. The loop filter shown is designed to give lowest integrated phase noise, for reference frequencies of between 26MHz and 52MHz. The external loop filter components give the flexibility to optimize the loop response for any particular application and combination of reference and VCO frequencies.



External Reference

The RFMD2081 have been designed to use an external reference such as a TCXO. The typical input will be a 0.8Vp-p clipped sine wave, which should be AC-coupled into the reference input. When the PLL is not in use, it may be desirable to turn off the internal reference circuits, by setting the REFSTBY bit low, to minimize current draw while in standby mode.

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On cold start, or if REFSTBY is programmed low, the reference circuits will need a warm-up period. This is set by the SU_WAIT bits. This will allow the clock to be stable and immediately available when the ENBL bit is asserted high, allowing the PLL to assume normal operation.

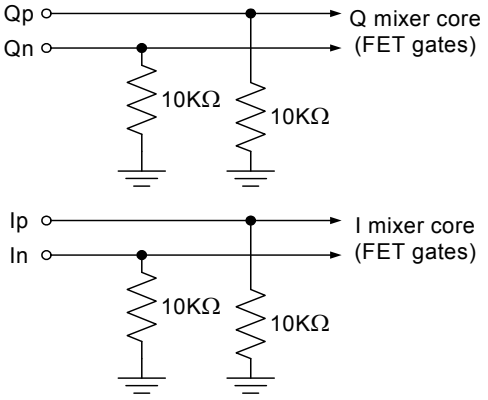
If the current consumption of the reference circuits in standby mode, typically 2mA, is not critical, then the REFSTBY bit can be set high. This allows the fastest startup and lock time after ENBL is taken high.

IQ Modulator

The IQ modulator core of the RFMD2081 is wideband covering from 45MHz to 2700MHz. It has been designed to achieve exceptional linearity for the amount of DC power consumed.

The modulator mixer cores have four coarse gain/current settings. Each setting steps the gain and linearity by 6dB and can be used to optimize performance or reduce power consumption.

The differential I and Q baseband inputs have 3dB bandwidth of 100MHz, and their input impedance is dominated by 10KΩ pull down resistors on each pin, as shown in the diagram below, so presenting a 20KΩ differential impedance. A common mode DC bias voltage of around +1.3V is required to set the current through the mixer cores for optimal performance. The offset between the common mode voltages on the differential pins can be adjusted to minimize LO leakage at the modulator output. The baseband input signals will be typically of the order of 1Vp-p differential. If required the phase and amplitude of the I and Q signals can be adjusted to reduce the level of the unwanted sideband signal at the modulator output.



The modulator output is differential and requires a balun and simple matching circuit optimized to the specific application frequencies. The modulator output pins are also used to source current for the modulator mixer circuits, about 20mA on each pin. This is usually via a center-tapped balun or by RF chokes in the external matching circuitry to the supply.

The modulator output is high impedance, consisting of approximately 2KΩ resistance in parallel with some capacitance, approximately 1pF. The modulator output does not require a conjugate matching network. It is a constant current output which will drive a real differential load of typically 200Ω. Since the mixer output is a constant current source, a higher resistance load will give higher output voltage and gain. A shunt inductor can be used to resonate with the mixer output capacitance at the frequency of interest. This inductor may not be required at lower frequencies where the impedance of the output capacitance is

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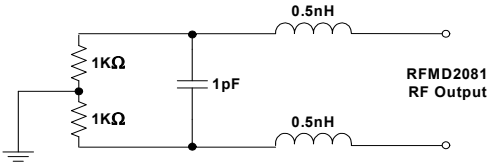
less significant. At higher output frequencies the inductance of the bond wires (about 0.5nH on each pin) becomes more significant. The following diagram is a simple model of the modulator output:



It is recommended to use a 4:1 balun on the modulator output, converting from the single ended 50Ω system to a 200Ω differential load. The RFMD2081 evaluation board has an RFXF8553 wideband transmission line transformer.

Serial Interface

All on-chip registers in the RFMD2081 are programmed using a proprietary 3-wire serial bus which supports both write and read operations. Synthesizer programming, device configuration and control are achieved through a mixture of hardware and software controls. Certain functions and operations require the use of hardware controls via the ENBL, MODE, and RESETX pins in addition to programming via the serial bus. Alternatively there is the option to control the chip completely via the serial bus.

The serial data interface can be configured for 4-wire bus operation, by setting the '4WIRE' bit in the SDI_CTRL register high. Then pin 26 is used as the data out pin, and pin 32 is the serial data in pin.

Hardware Control

Three hardware control pins are provided: ENBL, MODE, and RESETX.

The ENBL pin has two functions: to enable the analog circuits in the chip and to trigger the VCO auto-selection and coarse tuning mechanisms. The VCO auto-selection and coarse tuning are initiated when the ENBL pin is taken high. Every time the frequency of the synthesizer is reprogrammed, ENBL has to be asserted high to initiate these mechanisms and then to initiate the PLL locking. Alternatively following the programming of a new frequency the PLL re-lock self clearing bit could be used.

If the device is left in the enabled state for long periods, it is recommended that VCO auto-selection and coarse tuning (band selection) is performed for every 30°C change in temperature. The lock detect flag can be used to indicate when to perform the VCO calibration, it shows that the VCO tuning voltage has drifted significantly with changing temperature.

The RESETX pin is a hardware reset control that will reset all digital circuits to their startup state when asserted low. The device includes a power-on-reset function, so this pin should not normally be required, in which case it should be connected to the positive supply.

The MODE pin controls which PLL programming register bank is active.

Serial Data Interface Control

The normal mode of operation uses the 3-wire serial data interface to program the device registers, and three extra hardware control lines; MODE, ENBL and RESETX.

When the device is under software control, achieved by setting the SIPIN bit in the SDI_CTRL register high, then the hardware can be controlled via the SDI_CTRL register. When this is the case, the three hardware control lines are not required. If the device is under software control, pins 1 and 9 can be configured as general purpose outputs (GPO).

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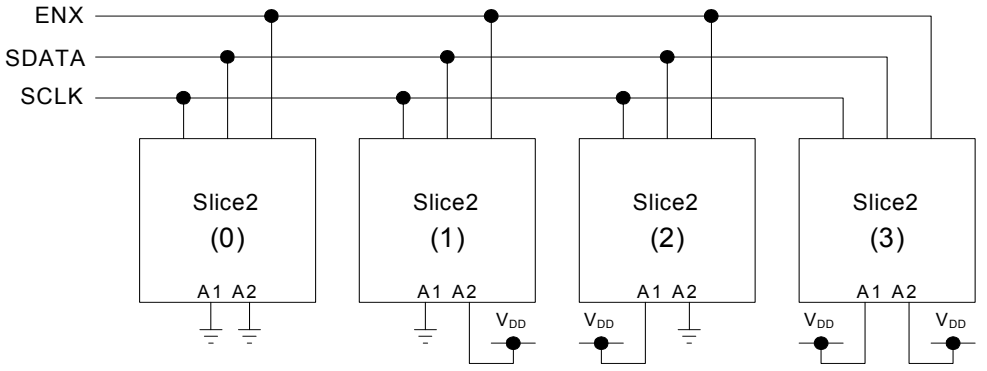
Multi-Slice Mode



The Multi-Slice mode of operation allows up to four chips to be controlled from a common serial bus. The device address pins, (15 and 16) ADD1 and ADD2, are used to set the address of each part.

On power up, and after a Reset, the devices ignore the address pins ADD1 and ADD2 and any data presented to the serial bus will be programmed into all the devices. However, once the ADDR bit in the SDI_CTRL register is set each device then adopts an address according to the state of the address pins on the device.

General Purpose Outputs

The general purpose outputs (GPOs) can be controlled via the GPO register, and will depend on the state of MODE since they can be set in different states corresponding to either path 1 or 2. The GPOs can be used for example to drive LEDs, or to control external circuitry such as switches or low power LNAs.

Each GPO pin can supply up to and above 20mA load current. The output voltage of the GPO high state will drop with increased current drive, by approximately 25mV/mA. Similarly the output voltage of the GPO low state will rise with increased current, again by approximately 25mV/mA.

Programming Information

Please refer to the register map and programming guides which are available for download from http://rfmd.com/products/IntSynthModulator/.

Evaluation Boards

The evaluation board for the RFMD2081 is provided as part of a design kit, along with the necessary cables and programming software tool to enable full evaluation of the device. The evaluation board has been configured for wideband operation; the modulator output is connected to a wideband transmission line transformer balun. Design kits can be ordered from www.rfmd.com or from local RFMD sales offices and authorized sales channels. For ordering codes please see "Ordering Information" on page 18. For further details on how to set up the design kits please refer to the user guide which can be downloaded from http://rfmd.com/products/IntSynthModulator/.

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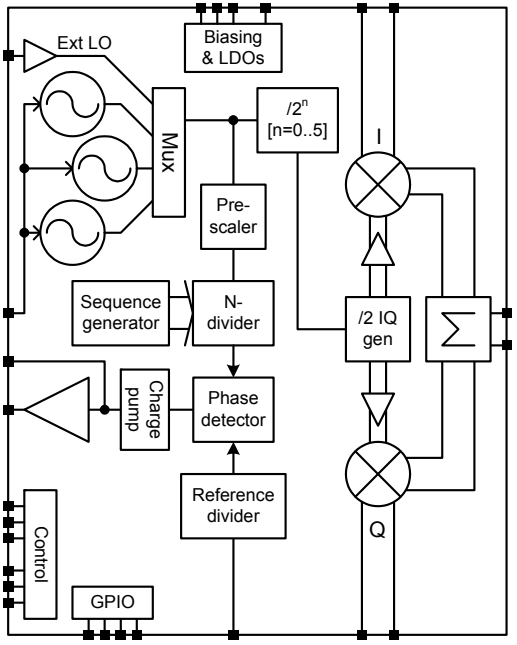
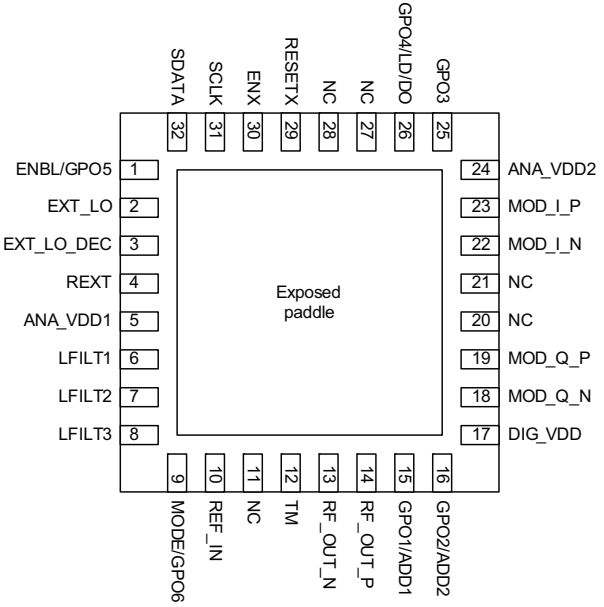
Detailed Functional Block Diagram



Pin Out



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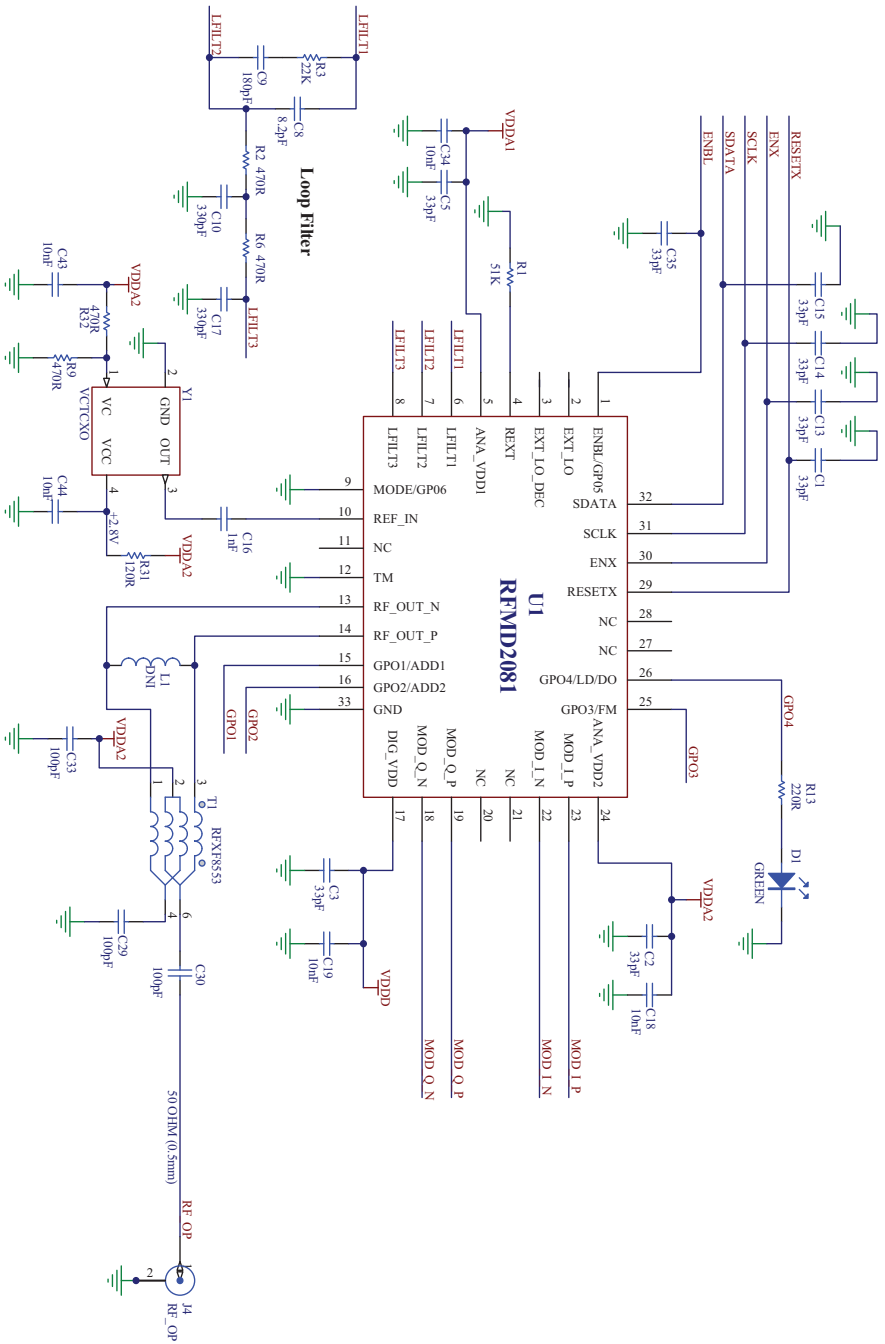
Application Schematic



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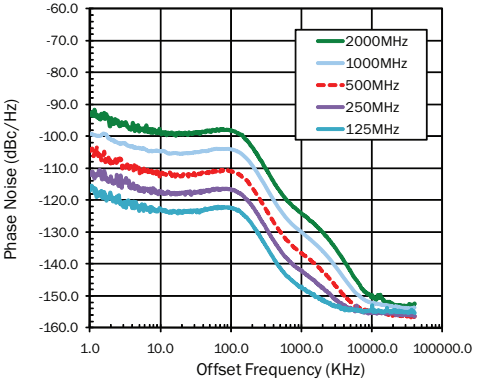
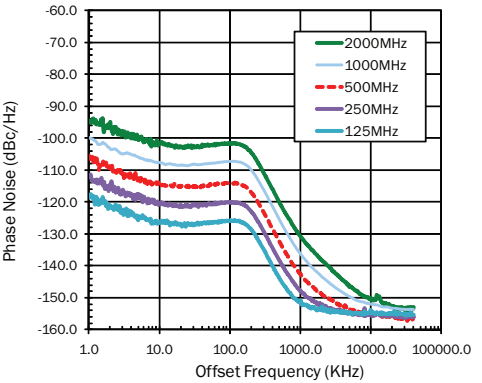
Typical Performance Characteristics: Synthesizer

V_{DD} = +3V and T_A = +27°C unless stated otherwise, as measured on RFMD2081 evaluation board.

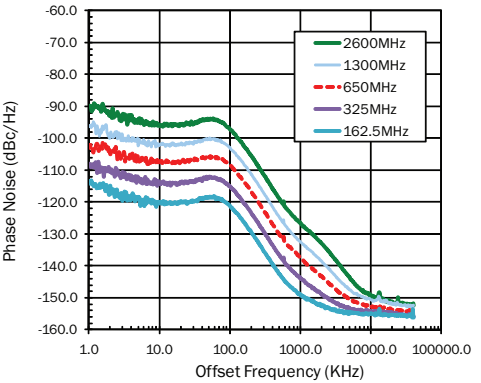
Synthesizer Phase Noise
4000MHz VCO Frequency, 26MHz Crystal Oscillator



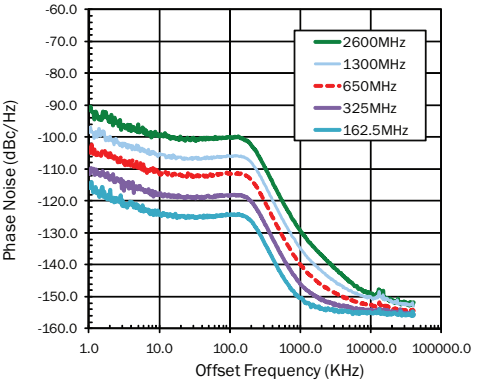
Synthesizer Phase Noise
4000MHz VCO Frequency, 52MHz Crystal Oscillator



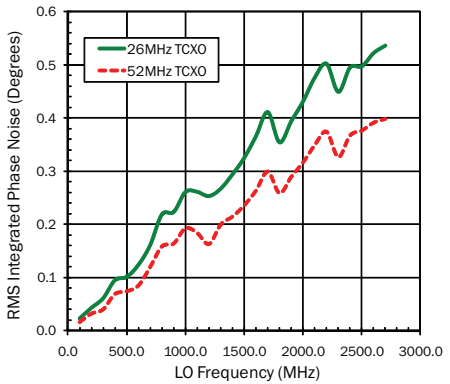
Synthesizer Phase Noise
5200MHz VCO Frequency, 26MHz Crystal Oscillator



Synthesizer Phase Noise
5200MHz VCO Frequency, 52MHz Crystal Oscillator



Synthesiser RMS Integrated Phase Noise
Integration Bandwidth 1KHz to 40MHz



Note:
- 26MHz Crystal Oscillator: NDK ENA3523A
- 52MHz Crystal Oscillator: NDK ENA3560A

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Typical Performance Characteristics: VCO

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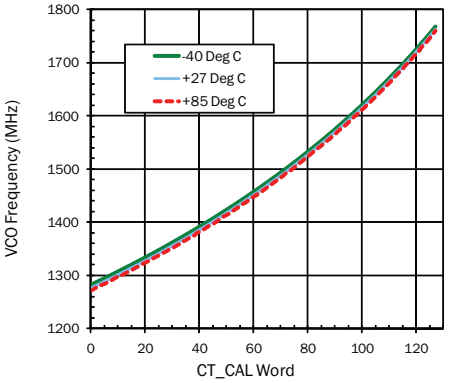
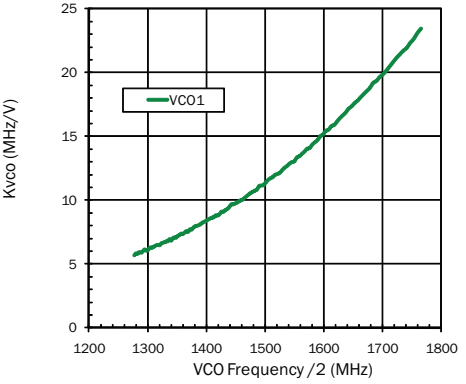
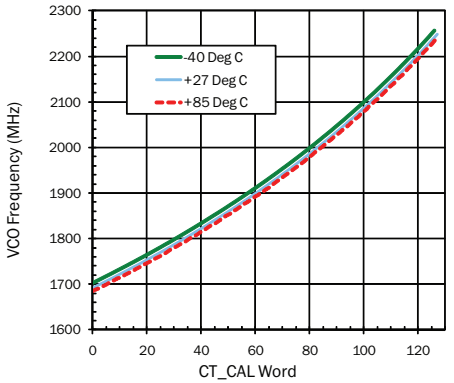
VCO1 Frequency versus CT_CAL
VCO1 with LO Divide by 2



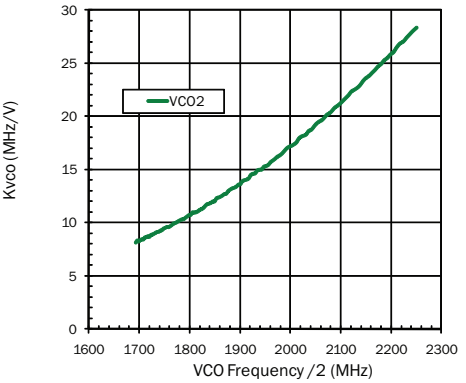
VCO1 Frequency versus Kvco
LO Divide by 2



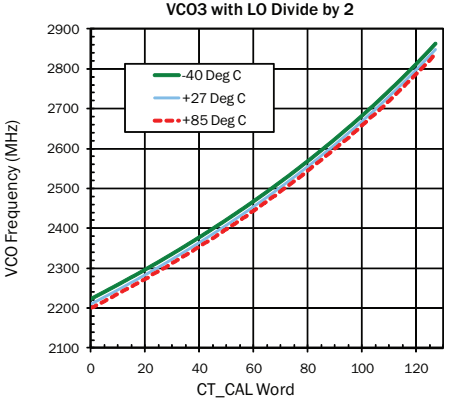
VCO2 Frequency versus CT_CAL
VCO2 with LO Divide by 2



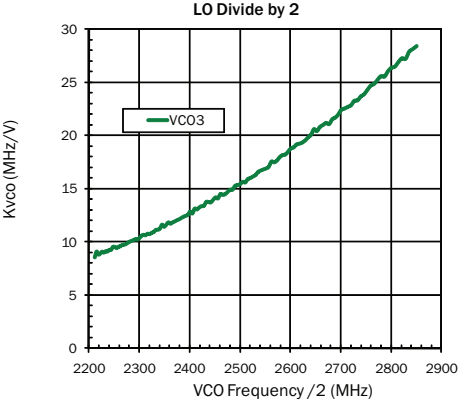
VCO2 Frequency versus Kvco
LO Divide by 2



VCO3 Frequency versus CT_CAL
VCO3 with LO Divide by 2



VCO3 Frequency versus Kvco
LO Divide by 2



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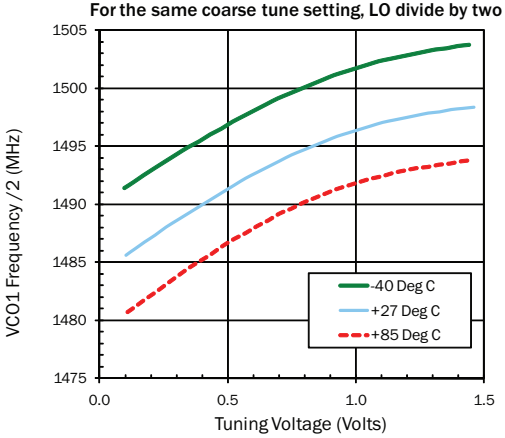
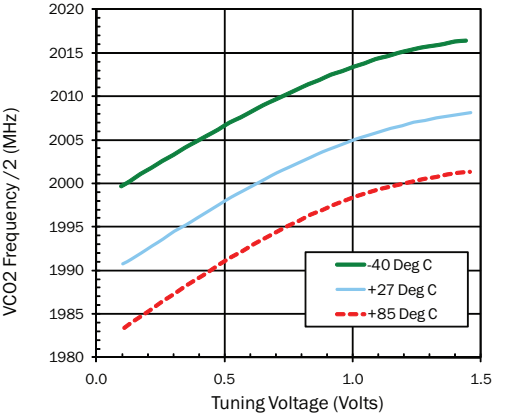
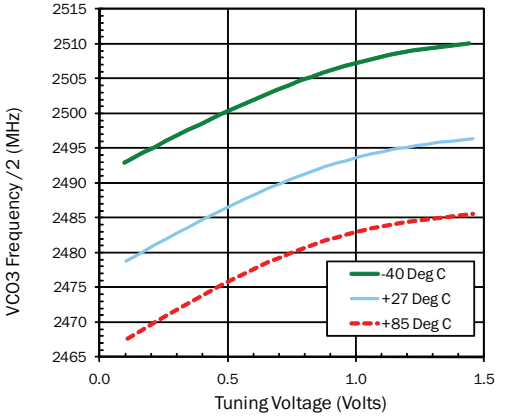
VCO1 Frequency versus Tuning Voltage
For the same coarse tune setting, LO divide by two



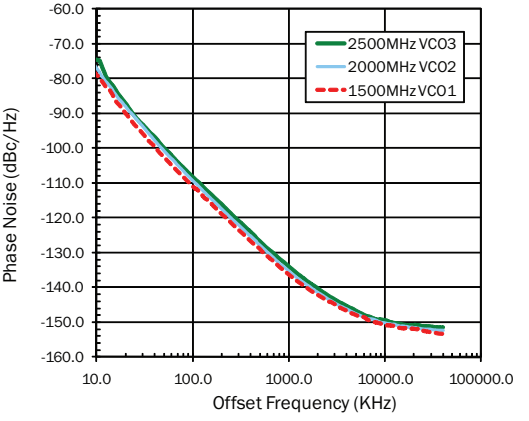
VCO2 Frequency versus Tuning Voltage
For the same coarse tune setting, LO divide by two



VCO3 Frequency versus Tuning Voltage
For the same coarse tune setting, LO divide by two



VCO Phase Noise
With LO Divide by 2



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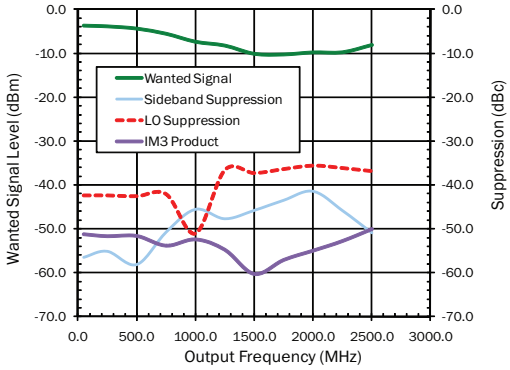
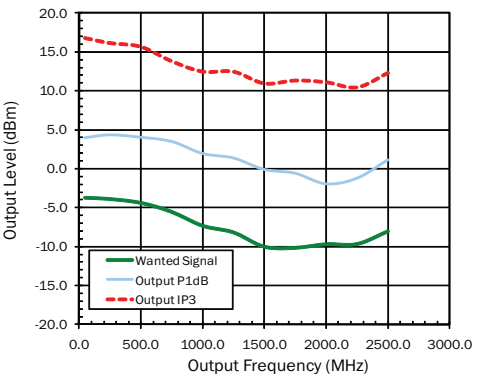
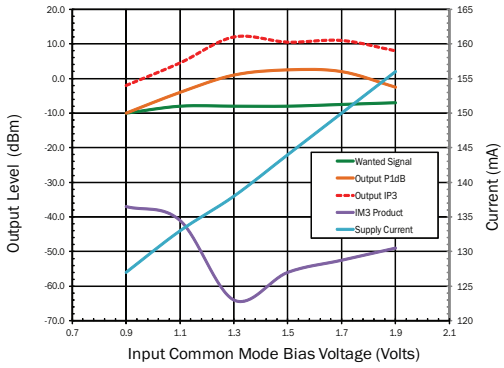
Modulator Typical Performance
I & Q Unadjusted, Output Unmatched



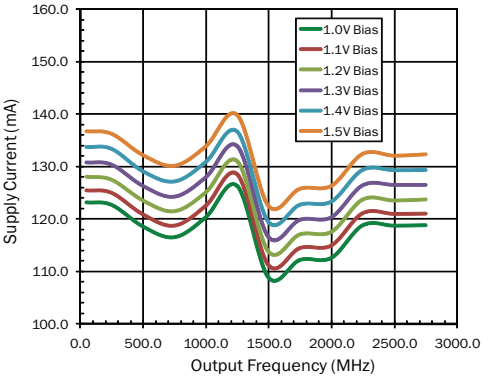
Modulator Typical Performance
Linearity, Output Unmatched



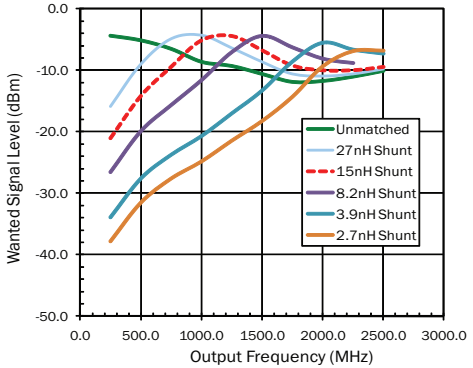
Modulator Performance Vs Common Mode Bias Voltage
Output Frequency = 1250 MHz



Typical Total Supply Current
+3.0V Supply



Modulator Output Frequency Response
Versus Shunt Matching Inductor Value



The modulator output power can be improved as output frequency increases by using a shunt inductor (L1 on Application Schematic) to resonate with the modulator output capacitance, typically 1pF.

The output transformer used for characterization is the RFXF8553 (T1) which has 3dB cut off point at 2500MHz.

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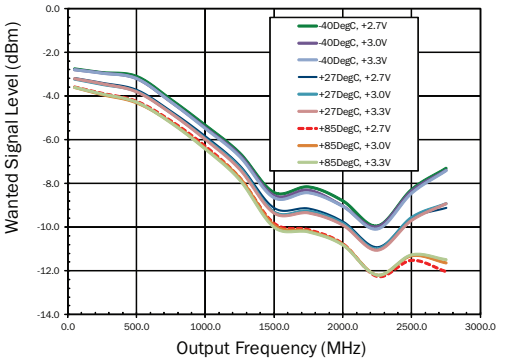
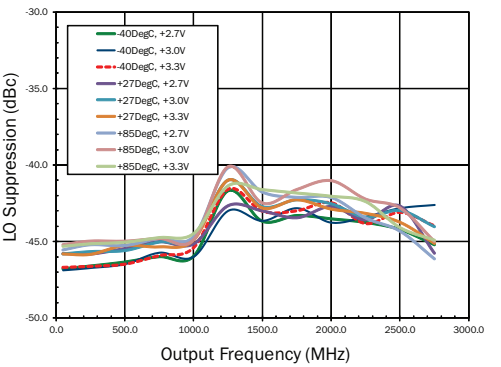
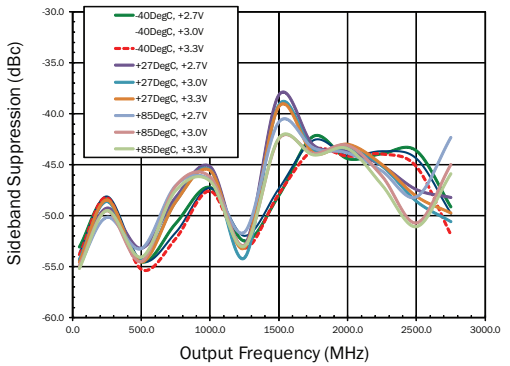
Modulator Output Power
Vs Temperature & Supply Voltage



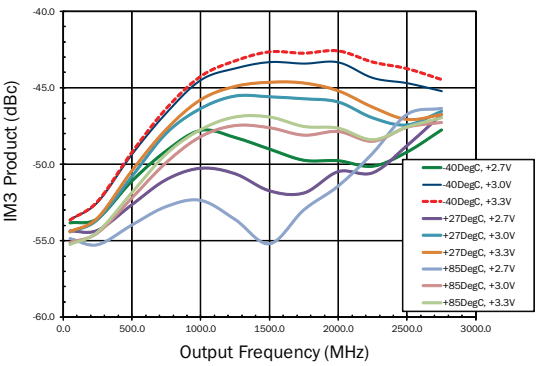
Modulator Unadjusted LO Suppression
Vs Temperature & Supply Voltage



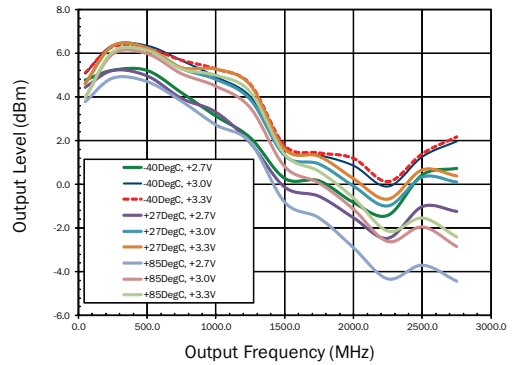
Modulator Unadjusted Sideband Suppression
Vs Temperature & Supply Voltage



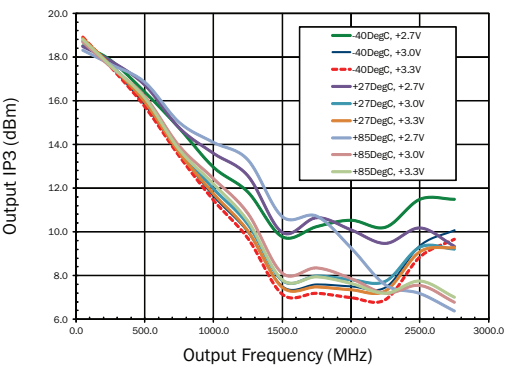
Modulator IM3 Output Tone
Vs Temperature & Supply Voltage



Modulator Output Power for 1dB Compression
Vs Temperature & Supply Voltage



Modulator Output IP3
Vs Temperature & Supply Voltage



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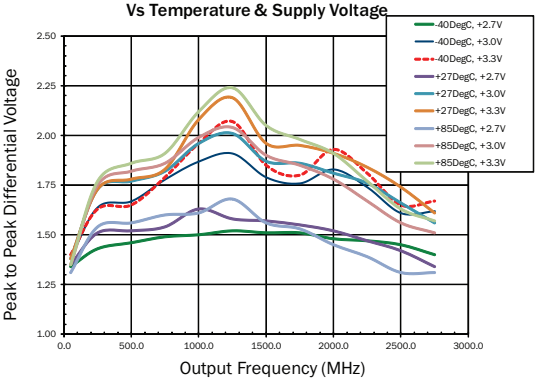
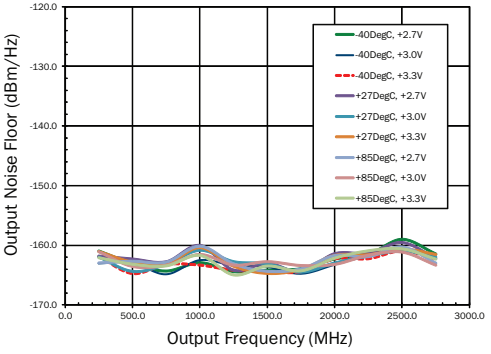
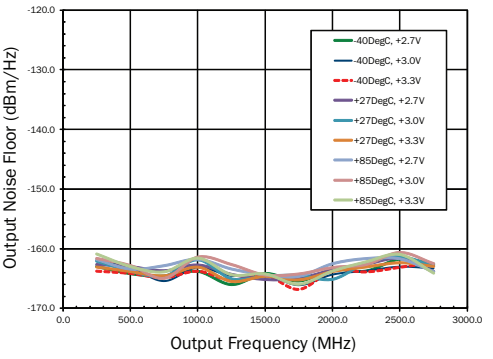
Modulator Input Voltage For 1dB Compression
Vs Temperature & Supply Voltage



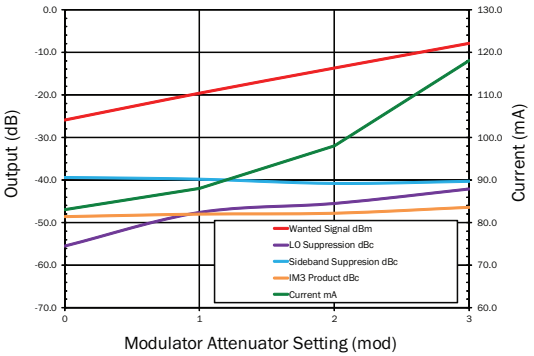
Modulator Output Noise Floor
1MHz Offset



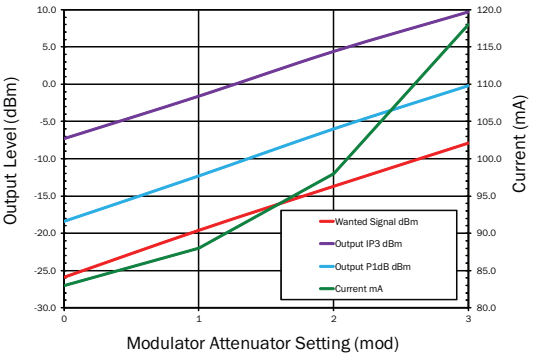
Modulator Output Noise Floor
5MHz Offset



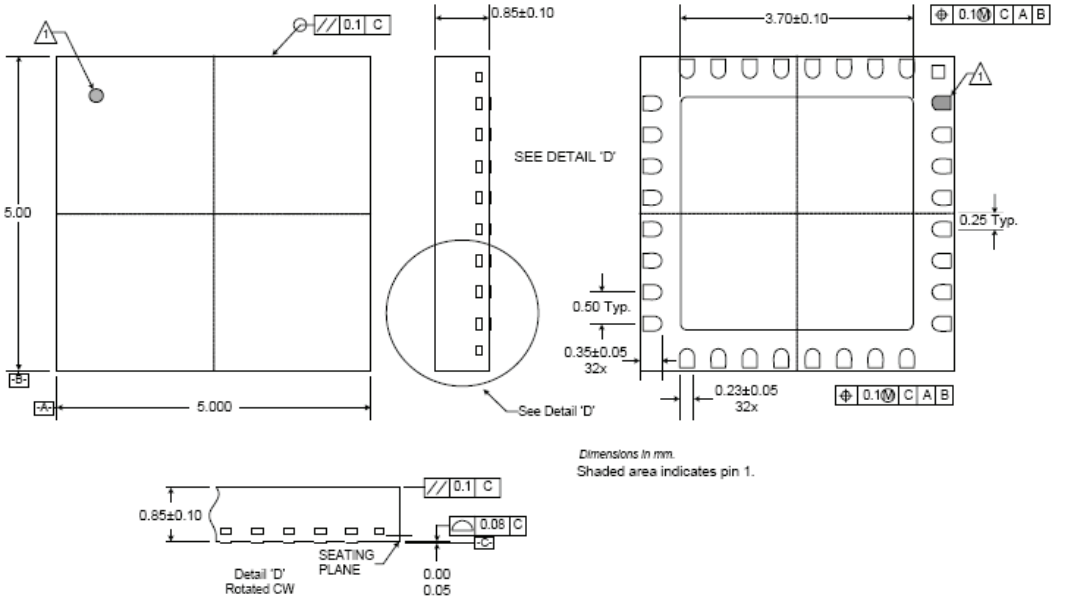
Effect of Attenuator Setting on Modulator
Unadjusted, Output Frequency = 1500MHz



Effect of Attenuator Setting on Gain & Linearity
Output Frequency = 1500MHz



.Package Drawing
QFN, 32-pin, 5mm x 5mm



Ordering Information

Ordering Code	Package	Quantity
RFMD2081SB	32-Pin QFN	5-Piece sample bag
RFMD2081SQ	32-Pin QFN	25-Piece sample bag
RFMD2081SR	32-Pin QFN	100-Piece reel
RFMD2081TR7	32-Pin QFN	750-Piece reel
RFMD2081TR13	32-Pin QFN	2500-Piece reel
DKMD2081	Complete Design Kit	1 Box

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