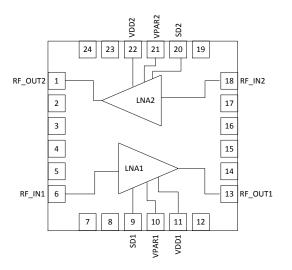


RFLA9003

Dual Low Noise Amplifier Module 1710MHz to 2180MHz

RFMD's RFLA9003 is a dual Low Noise Amplifier module with external connections to both LNAs. These LNAs feature a shutdown mode to turn off the LNA and provide up to 15dBm drive level without gain expansion and self-biasing in shutdown mode. Noise figure of 1.2dB and input P1dB of -3.5dBm make this component ideal for receiver input lineups. The RFLA9003 is packaged in a small 4.0mm x 4.0mm leadless laminate MCM. This module is internally matched to 50Ω on all RF ports making it easy to use with no external matching components required.



Functional Block Diagram

Ordering Information

| RFLA9003SQ | Sample bag with 25 pieces |
|-----------------|---|
| RFLA9003SR | 7" Reel with 100 pieces |
| RFLA9003TR13 | 13" Reel with 2500 pieces |
| RFLA9003PCK-410 | 1710MHz to 2180MHz PCBA with 5-piece sample bag |



Package: MCM, 24-pin, 4.0mm x 4.0mm

Features

- Frequency Range 1710MHz to 2180MHz
- Internally Matched to 50Ω on all RF Ports
- Shutdown Mode with +40dB Isolation
- Gain = >15dB per LNA
- Noise Figure of 1.2dB Typical
- Single +4.0V Supply
- Small 24-Pin, 4.0mm x 4.0mm, Multi-Chip Module (MCM)

Applications

- Cellular Repeaters
- General Purpose LNA

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Absolute Maximum Ratings

| Parameter | Rating | Unit |
|--|-----------------|-----------------|
| Supply Voltage | +5.5 | V _{DC} |
| Control Voltage | +5.5 | V _{DC} |
| DC Supply Current | 130 | mA |
| Power Dissipation | 770 | mW |
| Max RF Input Power | 15 | dBm |
| Operating Temperature (T _{CASE}) | -40 to +85 | °C |
| Storage Temperature Range | -40 to +150 | °C |
| Junction Temperature (T _J) | 150 | °C |
| ESD Rating - Human Body Model (HBM) | 1000 (Class 1C) | V |
| Moisture Sensitivity Level | MSL3 | |





RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000pm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Nominal Operating Parameters

| Description | Specification | | | | | |
|---------------------------------|---------------|------|------|------|---|--|
| Parameter | Min | Тур | Max | Unit | Condition | |
| Individual LNA Performance | | | | | Temp = 25°C, V _{CC} = 4V, Standard Application Circuit | |
| Frequency Range | 1710 | | 2180 | MHz | | |
| Gain (On Mode) | 15 | 18 | 21 | dB | SD = 0V | |
| Noise Figure | | 1.2 | 1.6 | dB | | |
| Input P1dB | -6.5 | -3.5 | | dBm | | |
| Input IP3 | 6.6 | 9 | | dBm | | |
| Gain (Off Mode) | | -39 | | dB | SD = 4V | |
| Gain Delta | >40 | | | dB | Gain LNA (on mode) – Gain LNA (off mode), 1950MHz | |
| Input Return Loss | | 9.7 | | dB | | |
| Output Return Loss | | 12.5 | | dB | | |
| Isolation (LNA1 OUT to LNA2 IN) | 35 | 47.5 | | dB | | |
| Gain Compression Slope | -1.1 | -1 | -0.1 | dB | Gain compresses monotonically with increased input power once saturated | |
| Overall Power Supply | | | | | Temp = 25°C, V _{CC} = 4V, Standard Application Circuit | |
| Supply Voltage | 3.5 | 4 | 5 | V | | |
| SD Voltage | 0 | | VCC | V | | |
| Logic High | 1.7 | | VCC | V | | |
| Logic Low | 0 | | 0.6 | V | | |
| Thermal Resistance | | 118 | | °C/W | 85°C at 4.5V at 35mA | |
| Current | 14 | 29 | 36 | mA | On Mode, SD = 0V | |
| | 0.5 | 3.5 | 6 | mA | Off Mode, SD = 4V | |

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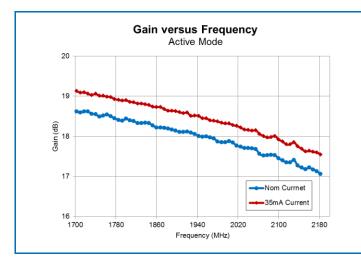
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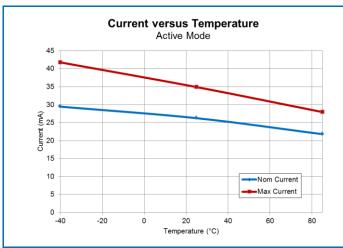
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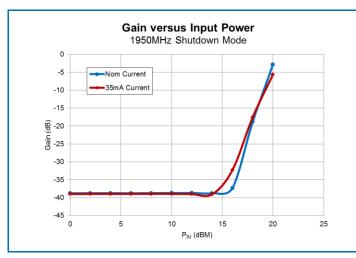
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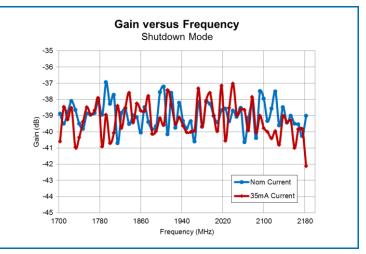


Typical Performance: T=25°C, VDD = 4V unless otherwise noted

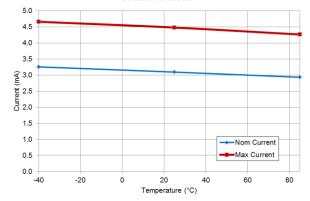


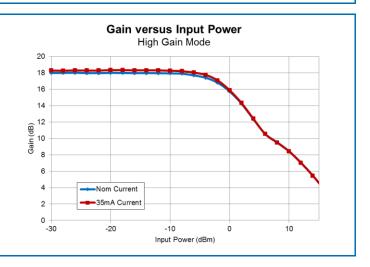






Current versus Temperature Shutdown Mode



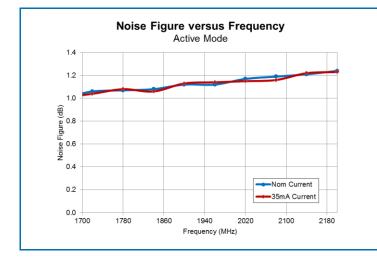


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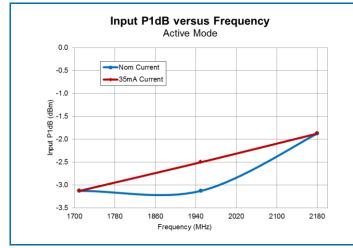
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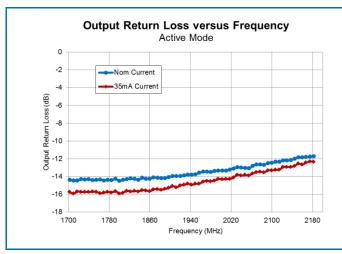
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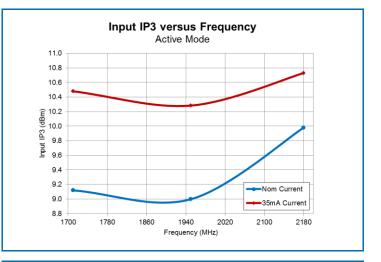




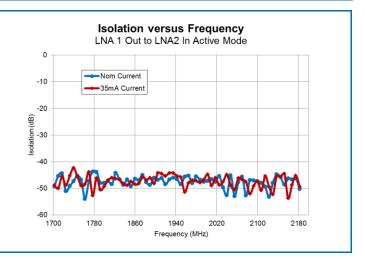








Input Return Loss versus Frequency Active Mode 0 Nom Current -2 35mA Current -4 Return Loss (dB) -6 -8 Input -10 -12 -14 1700 1780 1860 2180 1940 2020 2100 Frequency (MHz)



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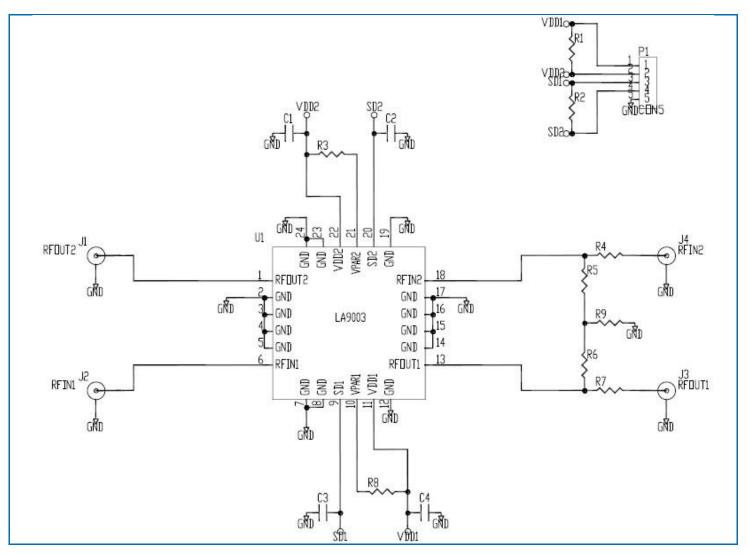
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Evaluation Board Schematic



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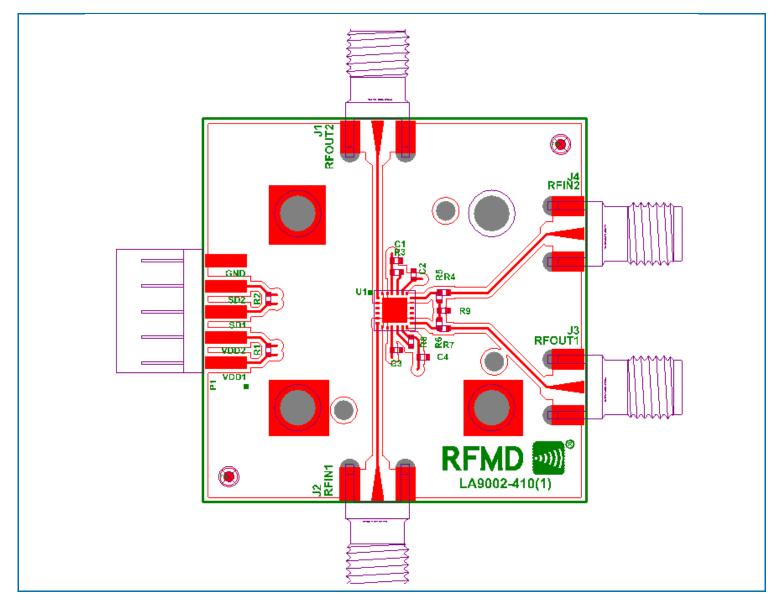
Evaluation Board Bill of Materials (BOM)

| Description | Reference Designator | Manufacturer | Manufacturer's P/N |
|--|----------------------|---------------------|--------------------|
| Evaluation Board | | DDI | LA9002-410(1) |
| RFLA9003 Module | U1 | RFMD | RFLA9003 |
| CAP, 0.1µF, 10% 16V, X7R, 0402 | C1-C4 | Murata Electronics | GRM155R71C104KA88D |
| CONN, SMA, END LNCH, UNIV, HYB MNT, FLT | J1-J4 | Heilind Electronics | PER MAT-21-9003 |
| RES, 0Ω, 0402 | R5-R6 | Kamaya, Inc. | RMC1/16SJPTH |
| CONN, HDR, ST, PLRZD, 9-PIN | P1 | ITW Pancon | MPSS100-5C |
| DNP | R1-R4*, R7-R9* | | |

Note: Parts with * following the Reference Designators should not be populated on PCBA.



Evaluation Board Assembly Drawing





Pin Names and Descriptions

| Pin | Name | Description | |
|-----|---------|---|--|
| 1 | RF_OUT2 | RF Output ; Internally 50 Ω matched and DC blocked | |
| 2 | GND | Connect to low inductance path to ground | |
| 3 | GND | Connect to low inductance path to ground | |
| 4 | GND | Connect to low inductance path to ground | |
| 5 | GND | Connect to low inductance path to ground | |
| 6 | RF_IN1 | RF Input; Internally 50Ω matched and DC blocked | |
| 7 | GND | Connect to low inductance path to ground | |
| 8 | GND | Connect to low inductance path to ground | |
| 9 | SD1 | Shut down pin for LNA1 | |
| 10 | VPAR1 | Connection for external resistor to raise current when connected from this pad to V_{DD} and to lower current when connected from this pad to ground | |
| 11 | VDD1 | VDD Supply, 10nF decoupling internal, supply for LNA1 | |
| 12 | GND | Connect to low inductance path to ground | |
| 13 | RF_OUT1 | RF Output; Internally 50Ω matched and DC blocked | |
| 14 | GND | Connect to low inductance path to ground | |
| 15 | GND | Connect to low inductance path to ground | |
| 16 | GND | Connect to low inductance path to ground | |
| 17 | GND | Connect to low inductance path to ground | |
| 18 | RF_IN1 | RF Input; Internally 50Ω matched and DC blocked | |
| 19 | GND | Connect to low inductance path to ground | |
| 20 | SD2 | Shut down pin for LNA2 | |
| 21 | VPAR2 | Connection for external resistor to raise current when connected from this pad to V_{DD} and to lower current when connected from this pad to ground | |
| 22 | VDD2 | VDD Supply, 10nF decoupling internal, supply for LNA2 | |
| 23 | GND | Connect to low inductance path to ground | |
| 24 | GND | Connect to low inductance path to ground | |

Truth Table

| | SD1 | SD2 |
|----------|-----|-----|
| LNA1 On | 0 | Х |
| LNA1 Off | 1 | Х |
| LNA2 On | х | 0 |
| LNA2 Off | Х | 1 |

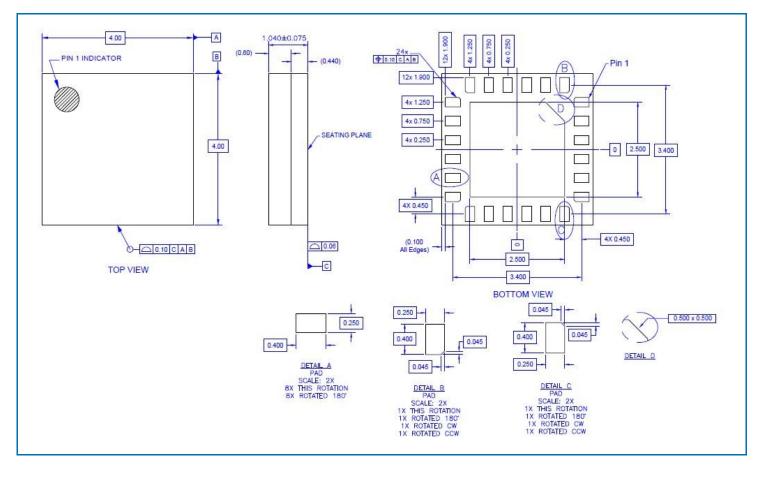
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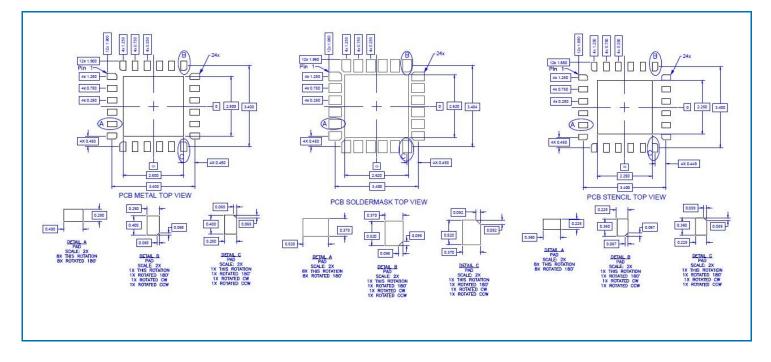


Package Outline Drawing (Dimensions in millimeters)

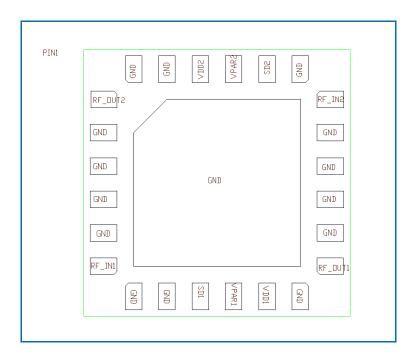




Stencil Drawing (Dimensions in millimeters)



IO Pattern Label

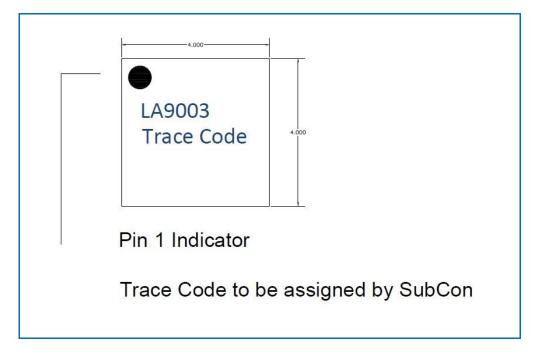


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Branding Diagram



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