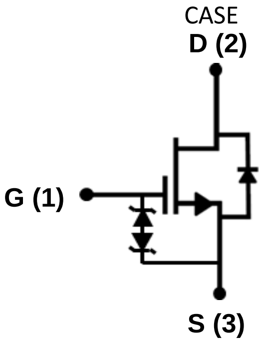
Description

United Silicon Carbide's cascode products co-package its high-performance G3 SiC JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This series exhibits ultra-low gate charge, but also the best reverse recovery characteristics of any device of similar ratings. These devices are excellent for switching inductive loads when used with recommended RC-snubbers, and any application requiring standard gate drive.



Part Number	Package	Marking
UF3C065040K3S	TO-247-3L	UF3C065040K3S

Features

- Typical on-resistance $R_{DS(on),typ}$ of 42mΩ
- Maximum operating temperature of 175°C
- Excellent reverse recovery
- Low gate charge
- Low intrinsic capacitance
- ESD protected, HBM class 2
- Very low switching losses (required RC-snubber loss negligible under typical operating conditions)

Typical Applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		650	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current [1]	I_D	T_C=25°C	54	A
		T_C=100°C	40	A
Pulsed drain current [2]	I_{DM}	T_C=25°C	125	A
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS}=3.19A	76	mJ
Power dissipation	P_{tot}	T_C=25°C	326	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	°C

[1] Limited by $T_{J,max}$

[2] Pulse width t_p limited by $T_{J,max}$

[3] Starting T_J = 25°C

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=1mA	650			V
Total drain leakage current	I_{DSS}	V_{DS}=650V, V_{GS}=0V, T_J=25°C		0.7	150	μA
		V_{DS}=650V, V_{GS}=0V, T_J=175°C		10		
Total gate leakage current	I_{GSS}	V_{DS}=0V, T_J=25°C, V_{GS}=-20V / +20V		6	±20	μA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V, I_D=40A, T_J=25°C		42	52	mΩ
		V_{GS}=12V, I_D=40A, T_J=175°C		78		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=10mA	4	5	6	V
Gate resistance	R_G	f=1MHz, open drain		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C=25°C			54	A
Diode pulse current [2]	$I_{S,pulse}$	T_C=25°C			125	A
Forward voltage	V_{FSD}	V_{GS}=0V, I_F=20A, T_J=25°C		1.5	1.75	V
		V_{GS}=0V, I_F=20A, T_J=175°C		1.8		
Reverse recovery charge	Q_{rr}	V_R=400V, I_F=40A, V_{GS}=-5V, R_{G_EXT}=20Ω di/dt=1100A/μs, T_J=25°C		138		nC
Reverse recovery time	t_{rr}			38		ns
Reverse recovery charge	Q_{rr}	V_R=400V, I_F=40A, V_{GS}=-5V, R_{G_EXT}=20Ω di/dt=1100A/μs, T_J=150°C		137		nC
Reverse recovery time	t_{rr}			38		ns

Typical Performance - Dynamic

Parameter	symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS}=100V, V_{GS}=0V, f=100kHz		1500		pF
Output capacitance	C_{oss}			200		
Reverse transfer capacitance	C_{rss}			2.2		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 400V, V_{GS}=0V		146		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS}=0V to 400V, V_{GS}=0V		325		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=400V, V_{GS}=0V		11.7		μJ
Total gate charge	Q_G	V_{DS}=400V, I_D=40A, V_{GS}=-5V to 15V		51		nC
Gate-drain charge	Q_{GD}			11		
Gate-source charge	Q_{GS}			19		
Turn-on delay time	$t_{d(on)}$	V_{DS}=400V, I_D=40A, Gate Driver=-5V to +15V, Turn-on $R_{G,EXT}$=1.8Ω, Turn-off $R_{G,EXT}$=22Ω Inductive Load, FWD: same device with V_{GS} = -5V and R_G = 22Ω RC snubber: R_S=5Ω and C_S=150pF T_J=25°C		35		ns
Rise time	t_r			24		
Turn-off delay time	$t_{d(off)}$			57		
Fall time	t_f			14		
Turn-on energy including R_S energy [4]	E_{ON}			500		μJ
Turn-off energy including R_S energy [4]	E_{OFF}			118		
Total switching energy including R_S energy [4]	E_{TOTAL}			618		
Snubber R_S energy during turn-on	E_{RS_ON}			1.7		
Snubber R_S energy during turn-off	E_{RS_OFF}			4.5		
Turn-on delay time	$t_{d(on)}$	V_{DS}=400V, I_D=40A, Gate Driver=-5V to +15V, Turn-on $R_{G,EXT}$=1.8Ω, Turn-off $R_{G,EXT}$=22Ω Inductive Load, FWD: same device with V_{GS} = -5V and R_G = 22Ω RC snubber: R_S=5Ω and C_S=150pF T_J=150°C		35		ns
Rise time	t_r			22		
Turn-off delay time	$t_{d(off)}$			60		
Fall time	t_f			13		
Turn-on energy including R_S energy [4]	E_{ON}			479		μJ
Turn-off energy including RS energy [4]	E_{OFF}			124		
Total switching energy including RS energy [4]	E_{TOTAL}			603		
Snubber R_S energy during turn-on	E_{RS_ON}			1.8		
Snubber R_S energy during turn-off	E_{RS_OFF}			5.3		

[4] The switching performance are evaluated with a RC snubber circuit as shown in Figure 24.

Thermal Characteristics

Parameter	symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.35	0.46	°C/W

Typical Performance Diagrams

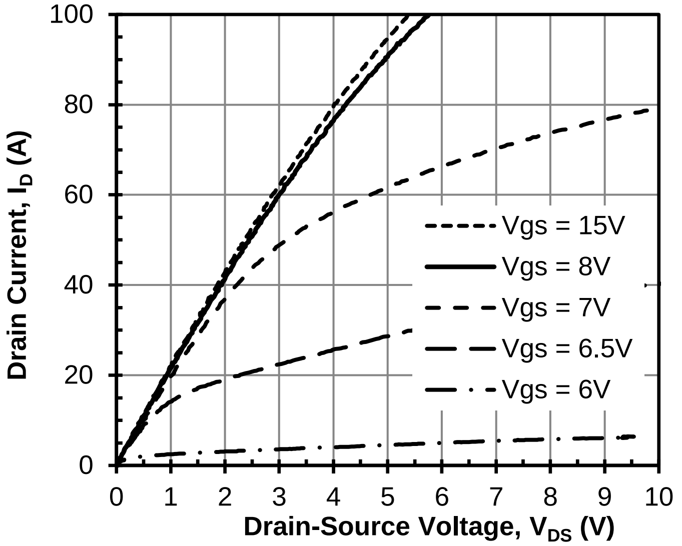


Figure 1 Typical output characteristics at T_J = - 55°C, tp < 250 µs

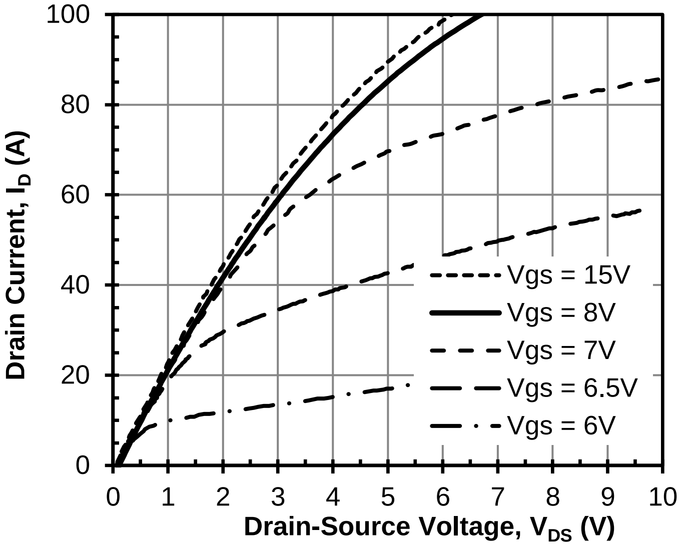


Figure 2 Typical output characteristics at T_J = 25°C, tp < 250 µs

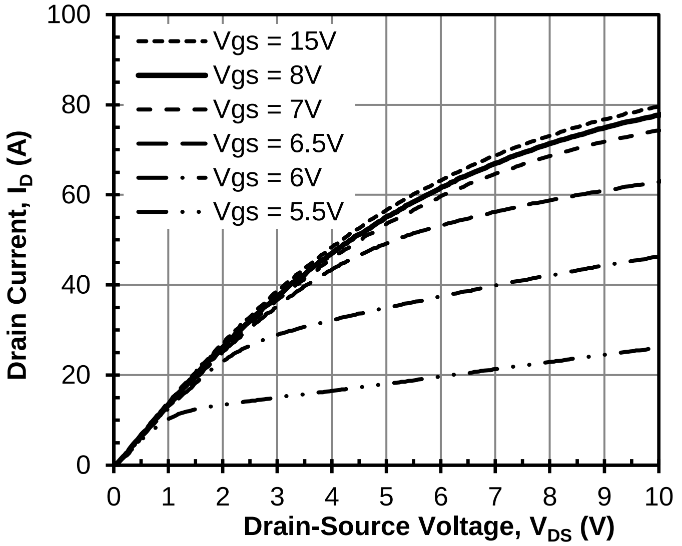


Figure 3 Typical output characteristics at T_J = 175°C, tp < 250 µs

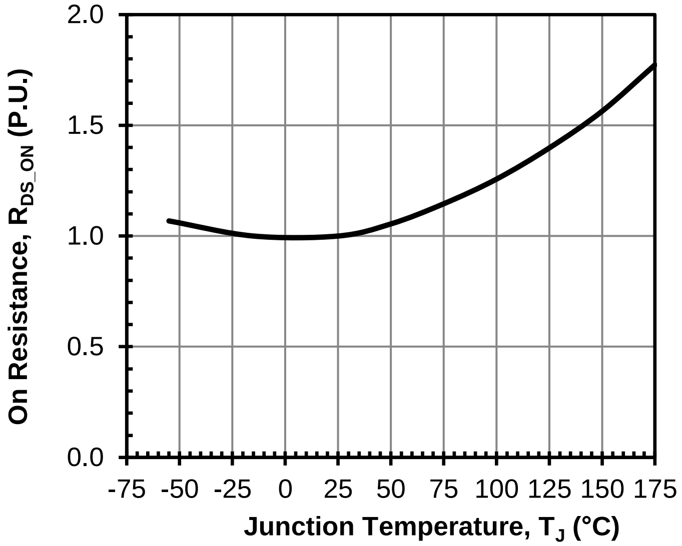


Figure 4 Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 40A

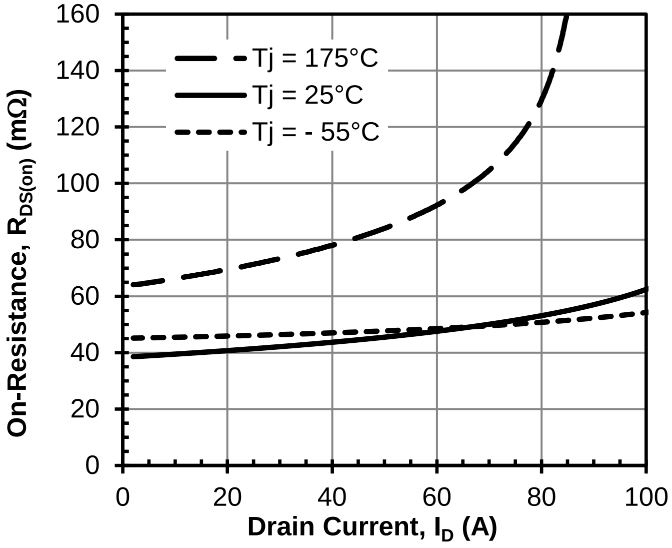


Figure 5 Typical drain-source on-resistance at V_{GS} = 12V

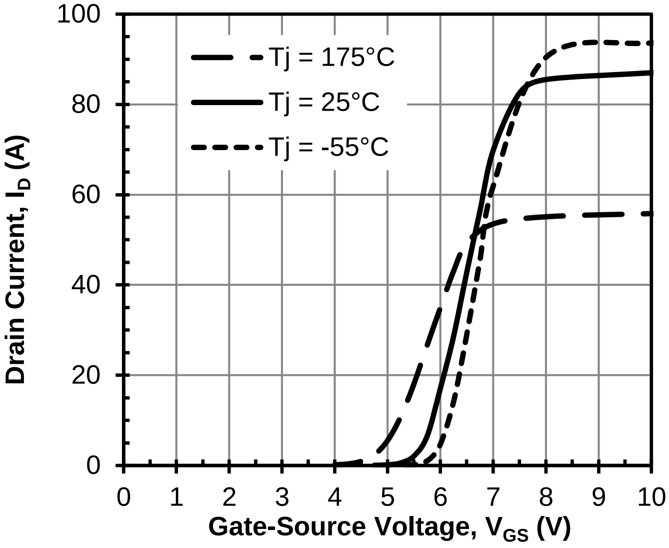


Figure 6 Typical transfer characteristics at V_{DS} = 5V

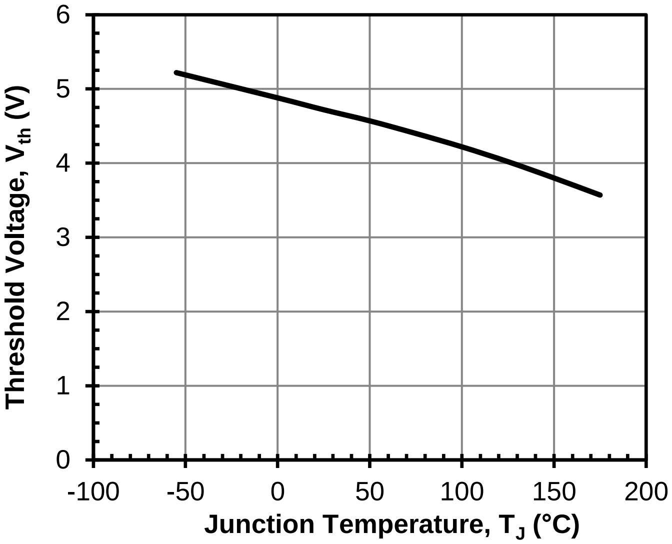


Figure 7 Threshold voltage vs. T_J at V_{DS} = 5V and I_D = 10mA

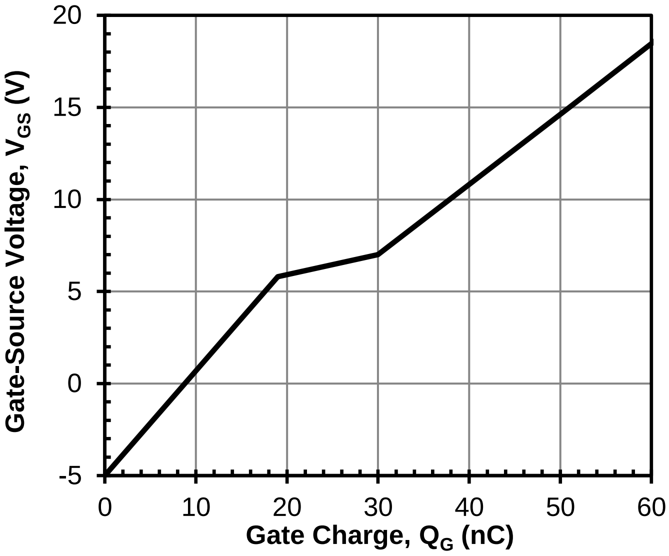


Figure 8 Typical gate charge at V_{DS} = 400V and I_D = 40A

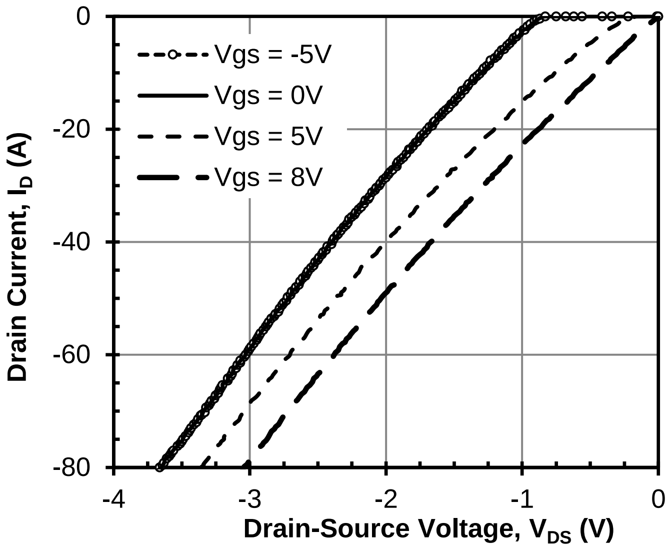


Figure 9 3rd quadrant characteristics at T_J = - 55°C

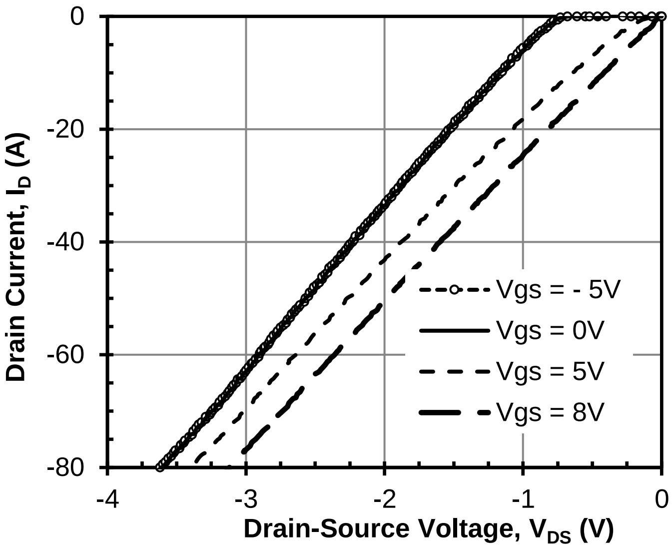


Figure 10 3rd quadrant characteristics at T_J = 25°C

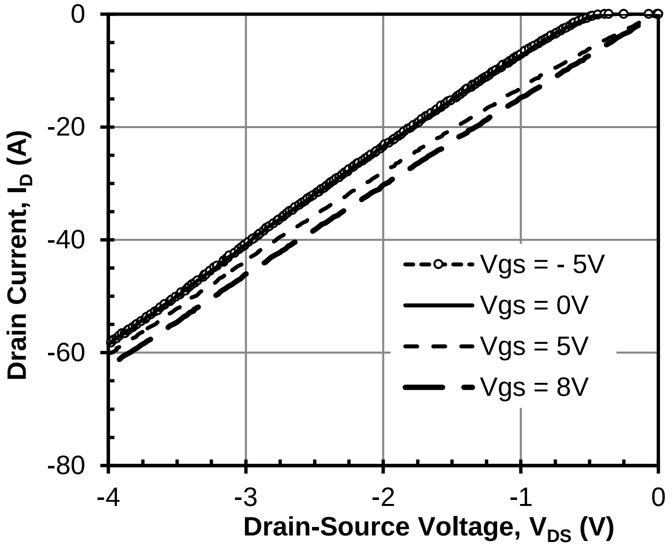


Figure 11 3rd quadrant characteristics at T_J = 175°C

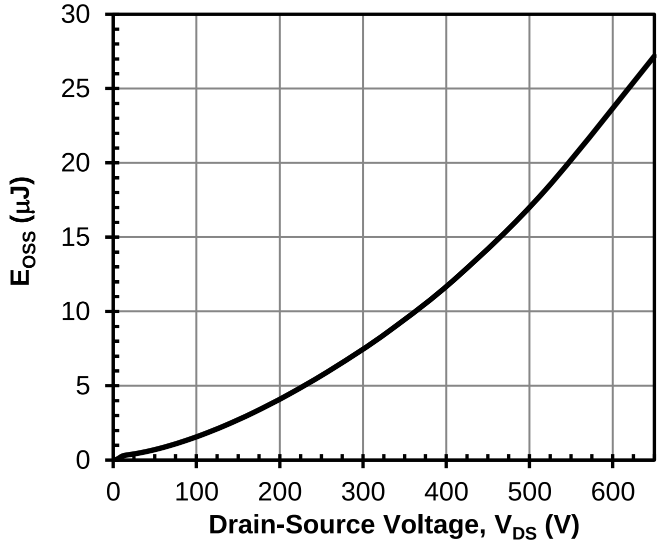


Figure 12 Typical stored energy in C_{OSS} at V_{GS} = 0V

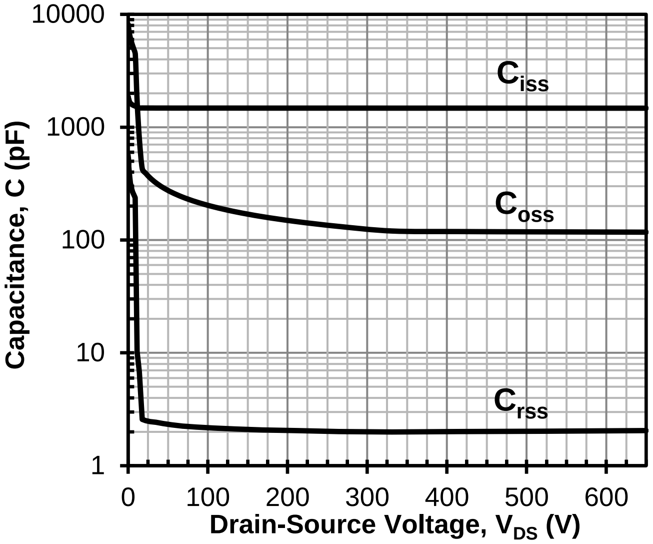


Figure 13 Typical capacitances at 100kHz and V_{GS} = 0V

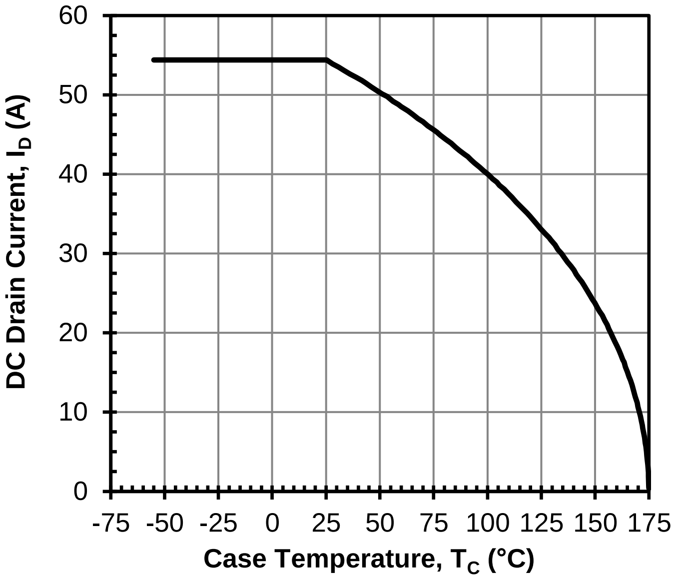


Figure 14 DC drain current derating

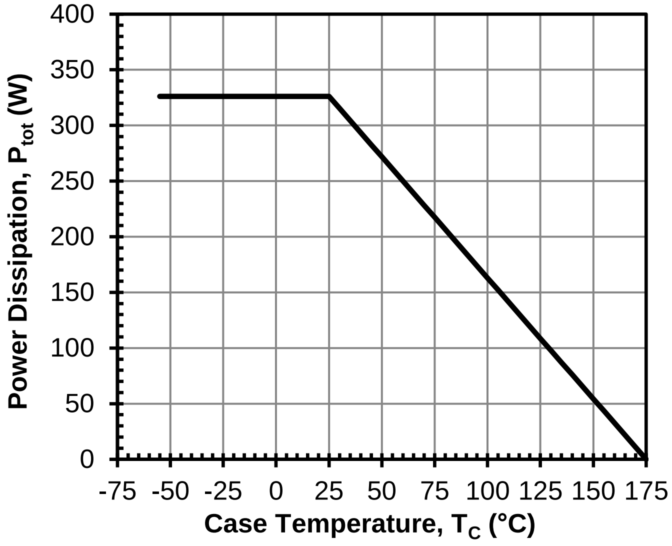


Figure 15 Total power dissipation

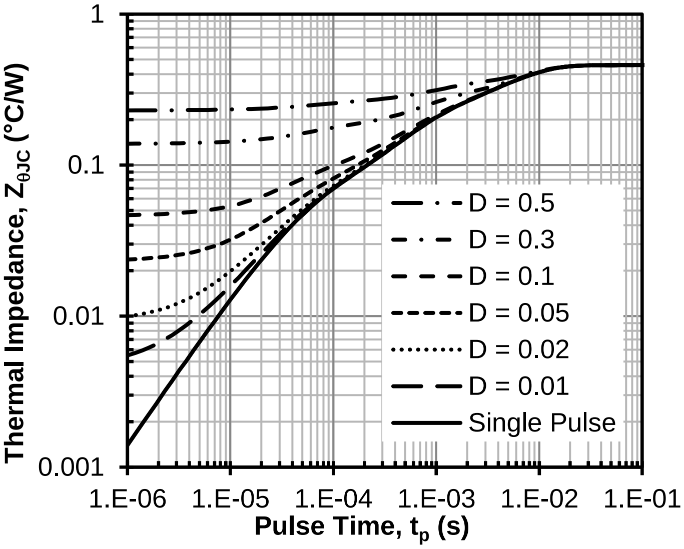


Figure 16 Maximum transient thermal impedance

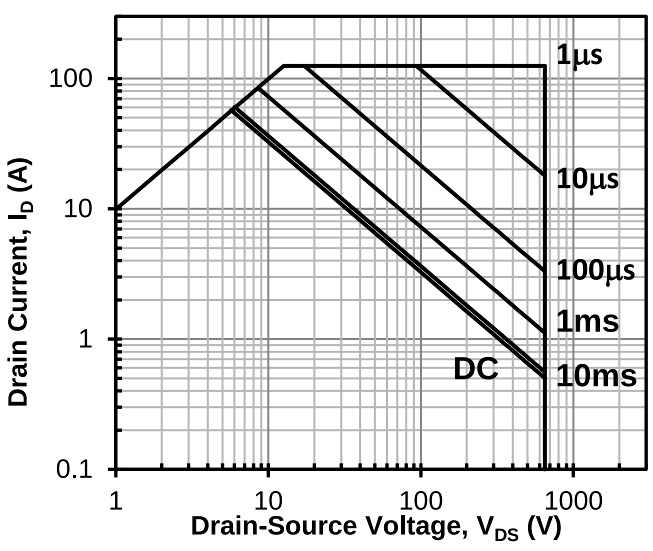


Figure 17 Safe operation area

T_c = 25°C, D = 0, Parameter t_p

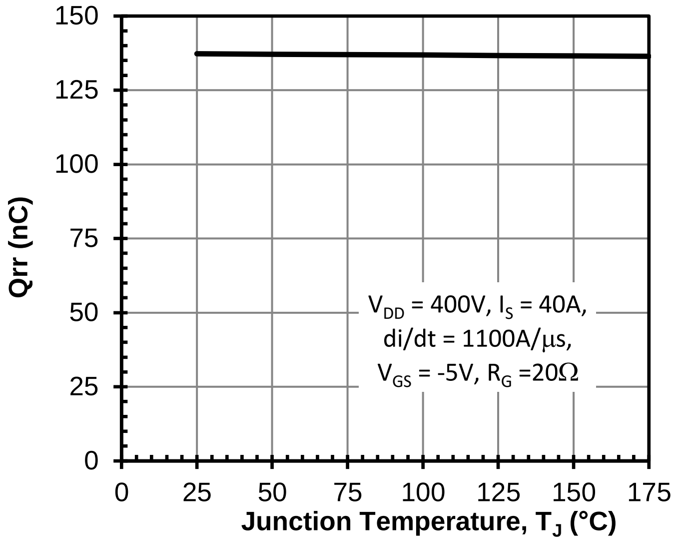
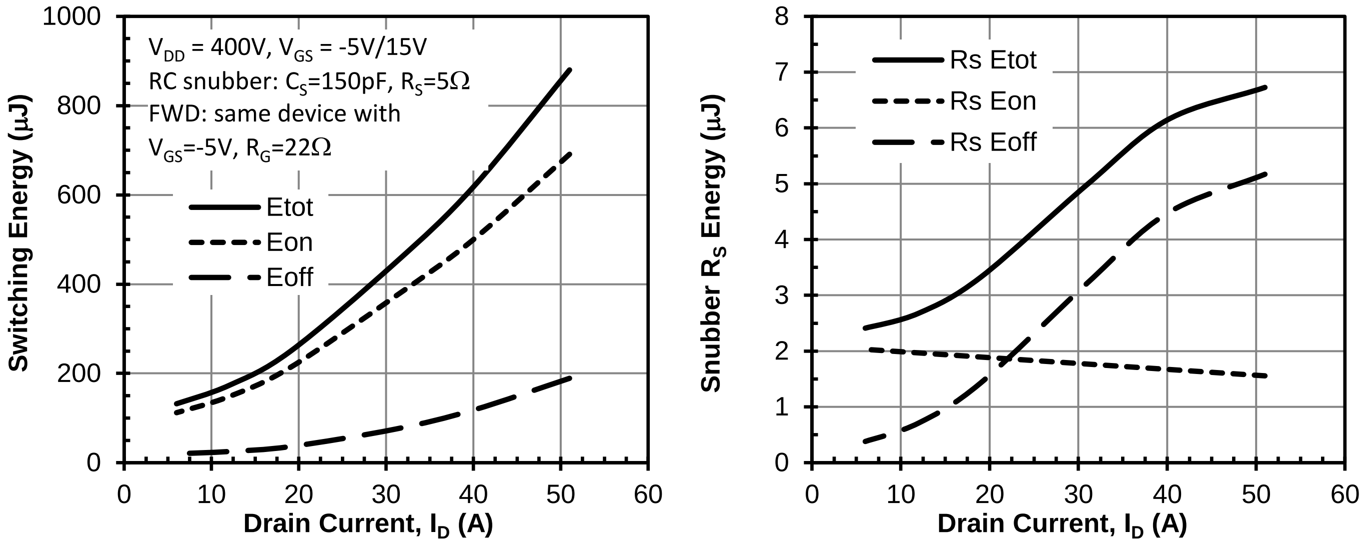
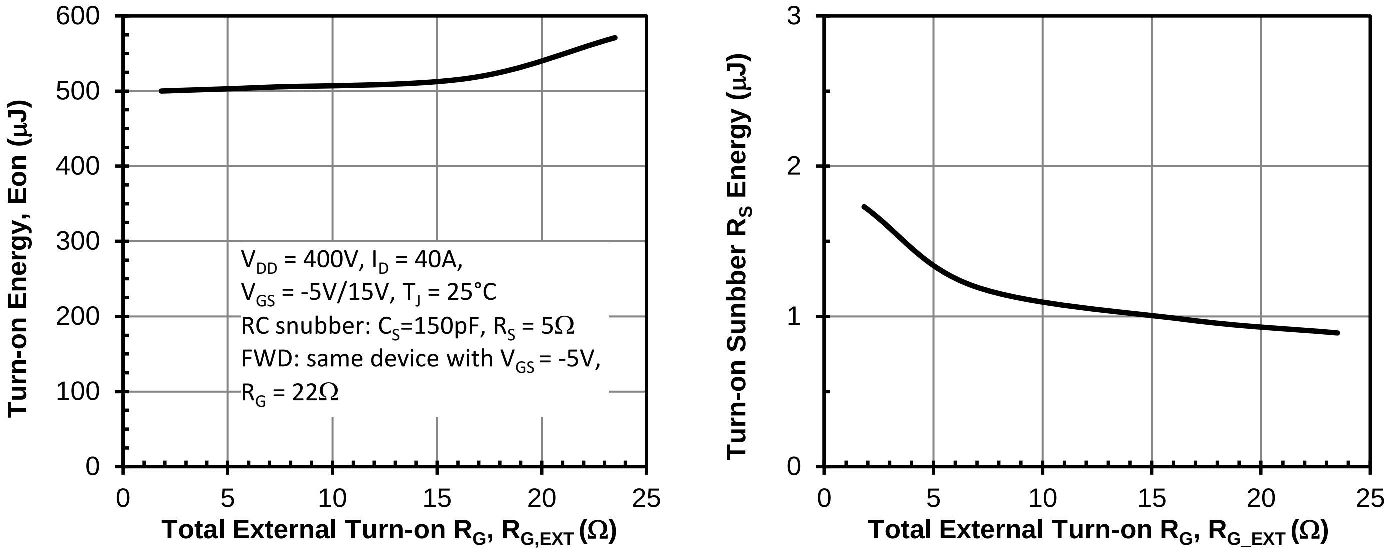


Figure 18 Reverse recovery charge Qrr vs. junction temperture



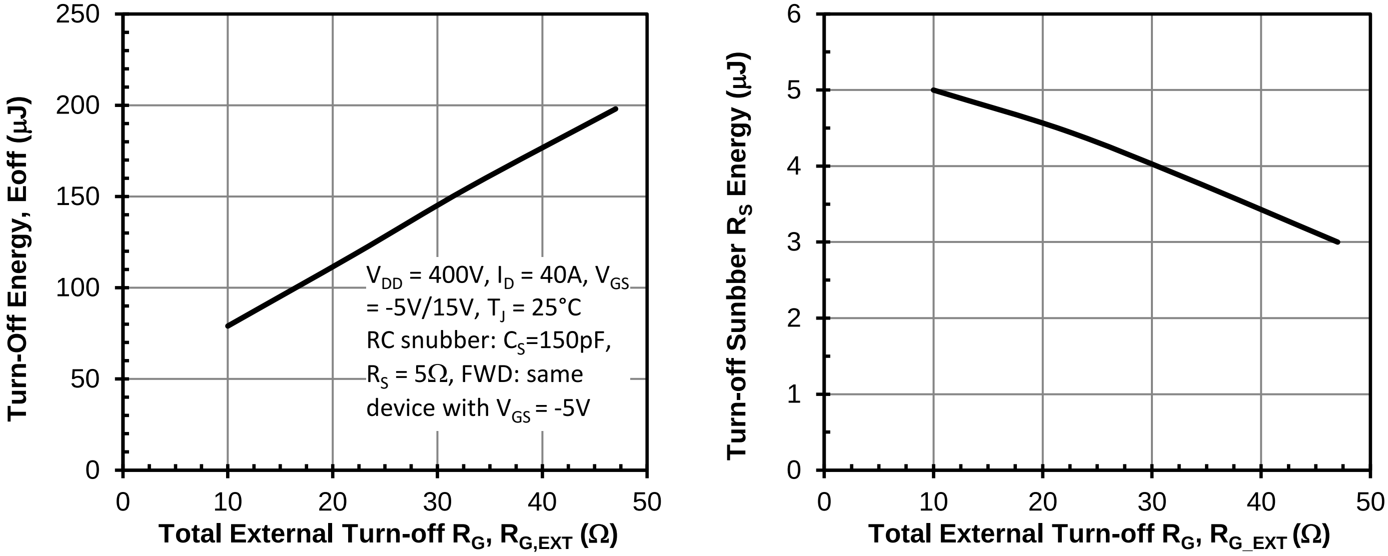
(a) *(b)*

Figure 19 Clamped inductive switching energy (a) and RC snubber energy loss (b) vs. drain current at T_J = 25°C, turn-on R_{G_EXT}=1.8 Ω and turn-off R_{G_EXT} = 22 Ω



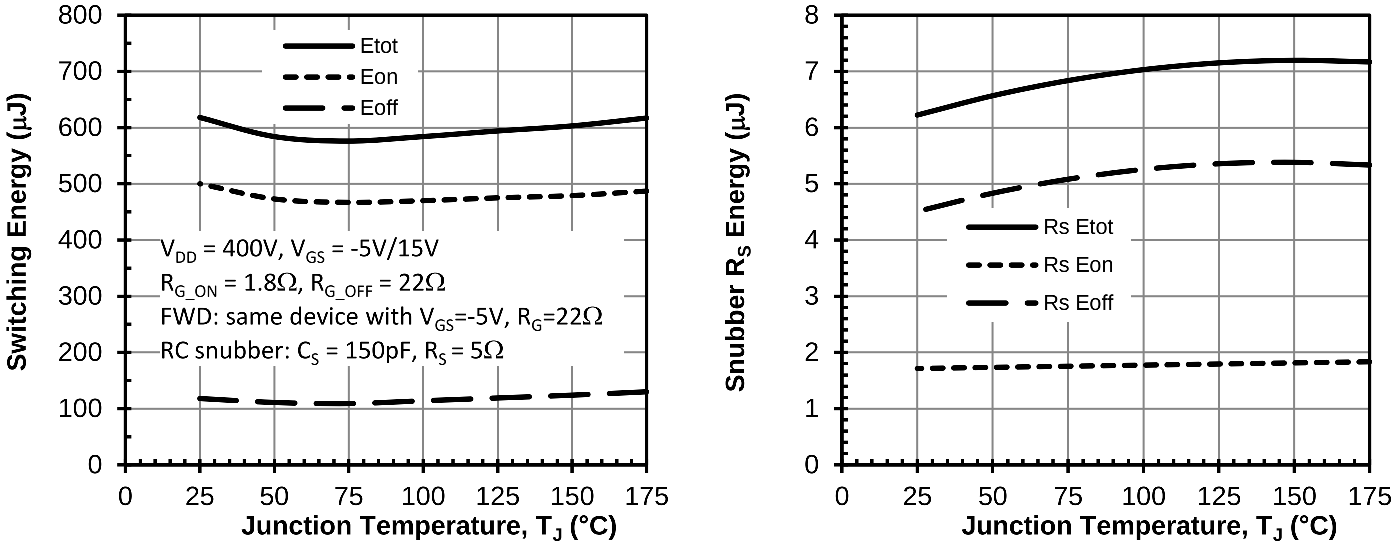
(a) *(b)*

Figure 20 Clamped inductive switching turn-on energy including RC snubber energy loss (a) and RC snubber energy loss (b) as a function of total external turn-off gate resistor R_{G_EXT}.



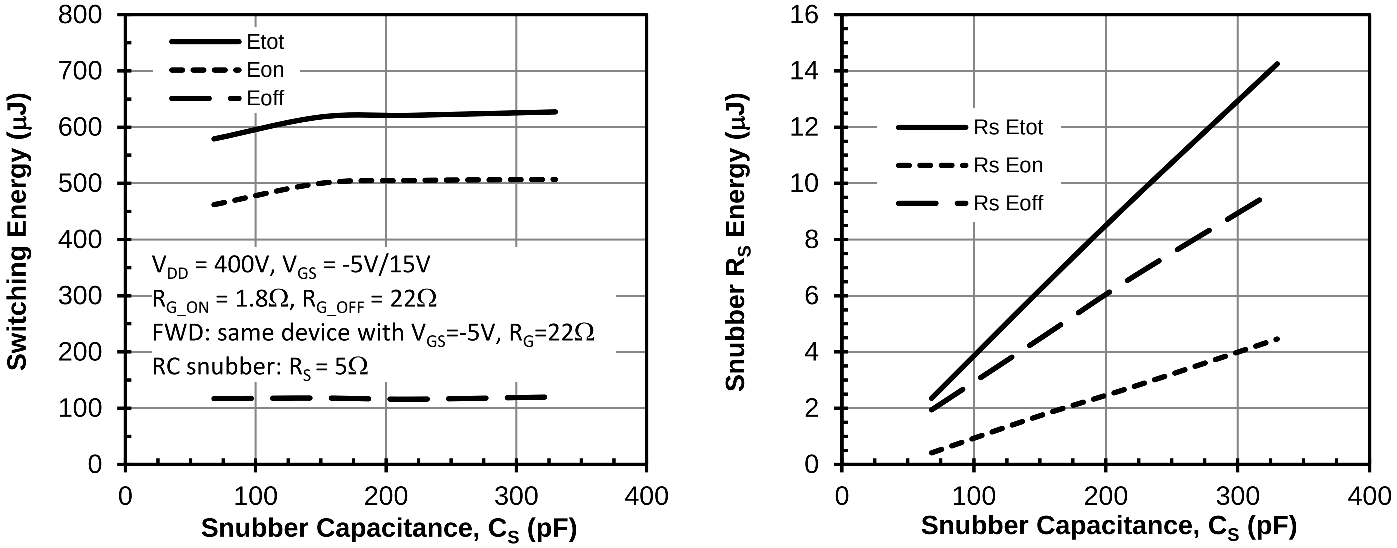
(a) *(b)*

Figure 21 Clamped inductive switching turn-off energy including RC snubber energy loss (a) and RC snubber energy loss (b) as a function of total external turn-off gate resistor R_{G_EXT}.



(a) *(b)*

Figure 22 Clamped inductive switching energy including RC snubber energy loss (a) and RC snubber energy loss (b) as a function of junction temperature at I_D = 40A



(a) *(b)*

Figure 23 Clamped inductive switching energy including RC snubber energy loss (a) and RC snubber energy loss (b) as a function of the snubber capacitance Cs at I_D = 40A and T_J = 25°C

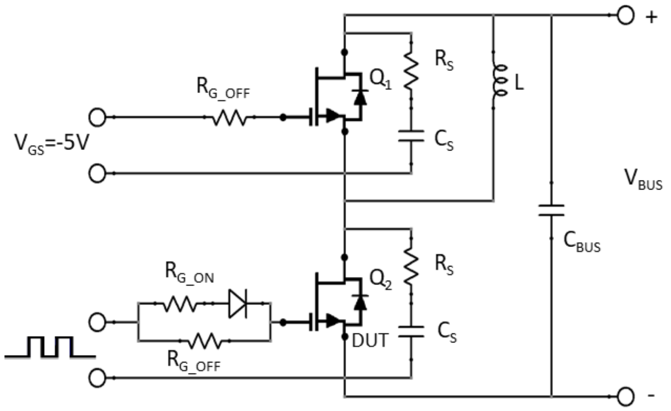


Figure 24 Inductive load switching test circuit

An RC snubber ($R_S = 5\,\Omega$, C_S = 150pF) is required to improve the turn-off waveforms.

Applications Information

SiC cascodes are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (Coss), gate charge (Qg), and reverse recovery charge (Qrr) leading to low conduction and switching losses. The SiC cascodes also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the cascode is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on cascode operation, see www.unitedsic.com.

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