TQP3M9039

50 – 1500 MHz Dual LNA

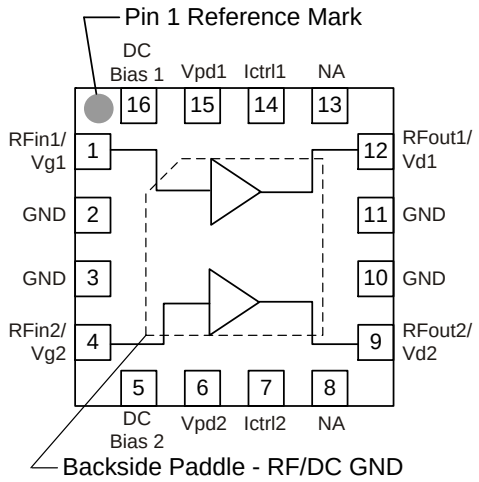
Product Description

The TQP3M9039 is a high linearity, ultra low noise figure dual device amplifier in a 4x4 mm package. At 830 MHz in a balanced configuration, the LNA provides 18 dB gain, 20.7 dBm IIP3 and 0.6 dB noise figure. The part does not require a negative supply for operation and is bias adjustable for both drain current and voltage. The device is housed in a green/RoHS-compliant industry standard QFN package.

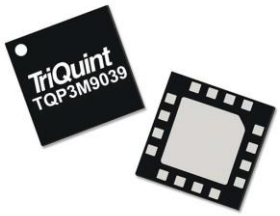
The TQP3M9039 consists of a single monolithic GaAs E-pHEMT die and integrates bias circuitry as well as shut-down capability allowing the LNA to be useful for both FDD and TDD applications.

The TQP3M9039 is optimized for the 700−1000 MHz band, but can be used outside of the band. Qorvo offers pin-compatible dual LNAs for the 1.5−2.3 GHz band (TQP3M9040) and 2.3−4.0 GHz (TQP3M9041). The balanced amplifier is optimized for high performance receivers in wireless infrastructure and can be used for base-station transceivers or tower-mounted amplifiers.

Functional Block Diagram



Top View



16-pin 4 mm x 4 mm QFN Package

Key Features

- 0.17 dB NFmin (Single Channel) at 830 MHz
- 50−1500 MHz Operational bandwidth
- 18 dB Gain at 830 MHz
- +20.7 dBm Input IP3
- Integrated shut-down biasing feature
- Bias adjustable
- Does not require negative voltage supply
- 4x4 mm 16-pin QFN plastic package

Applications

- Base Station Receivers
- Tower Mount Amplifiers
- Balanced Amplifiers
- FDD-LTE, TDD-LTE, WCDMA, CDMA, GSM
- General Purpose Wireless

Ordering Information

Part No.	Description
TQP3M9039	50−1500 MHz Dual LNA
TQP3M9039-PCB	700−1000 MHz Evaluation Board

Standard T/R size = 2500 pieces on a 13” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150°C
Drain Voltage (V_d)	+7 V
I_{dd} (V_d = 5V), single channel	300 mA
Input Power (CW)	+22 dBm
Input Power (DC off condition)	+22 dBm
Input Power (DC off condition & 10% Duty Cycle)	+30 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{pd}	0		+5	V
V_g	0	+0.5	+1	V
V_d	+2		+5	V
I_d, single channel		57	85	mA
Operating Temp. Range	−40		+105	°C
T_{ch} (for>10^6 hrs MTTF)			190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions (1)	Min	Typ	Max	Units
Operational Frequency Range		50		1500	MHz
Test Frequency			830		MHz
Gain		16.9	18.1	19.3	dB
Output P1dB			+21.5		dBm
Input IP3	Pin=−13 dBm/tone, Δf=1 MHz	+17	+20.7		dBm
Output IP3	Pout=+5 dBm/tone, Δf=1 MHz		+38.8		dBm
Noise Figure (2)	Balanced configuration		0.60	0.93	dB
Drain Voltage, V_d			+4.35		V
Drain Current, I_d	Single Channel	40	57	85	mA
Power Down Control Voltage, V_{pd}	On-State	0		+0.3	V
Switching time	Off-State	+2.1		V_d	V
Thermal Resistance, θ_{jc}	Channel to case - per channel		61		°C/W

Notes:
1. Test conditions unless otherwise noted: V_d = +4.35V, Temp.=+25°C, tuned balanced configuration.
2. The Noise Figure is de-embedded to the input pin of the input hybrid coupler.

De-embedded S-parameters Data

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
10	-0.03	-1.68	30.21	176.23	-60.44	97.03	-5.71	-0.38
50	-0.27	-7.74	29.70	162.29	-47.53	88.14	-5.42	3.49
100	-0.86	-13.71	28.71	147.86	-42.05	91.69	-4.96	4.58
200	-2.19	-19.43	26.35	127.40	-35.66	89.29	-4.23	2.40
300	-3.19	-21.05	24.10	114.93	-31.84	86.87	-3.92	-1.10
400	-3.87	-21.42	22.20	106.47	-29.16	84.94	-3.81	-4.32
500	-4.37	-21.79	20.61	100.16	-27.18	82.90	-3.79	-7.35
600	-4.73	-21.95	19.25	95.02	-25.52	80.76	-3.80	-10.12
700	-5.04	-22.43	18.07	90.61	-24.12	78.60	-3.85	-12.81
800	-5.31	-23.22	17.05	86.68	-22.92	76.46	-3.93	-15.40
900	-5.53	-24.42	16.15	83.07	-21.83	74.41	-4.01	-17.80
1000	-5.74	-25.32	15.33	79.69	-20.86	72.19	-4.09	-20.29
1100	-5.96	-26.36	14.61	76.51	-19.96	70.16	-4.20	-22.88
1200	-6.22	-27.85	13.95	73.34	-19.15	67.88	-4.33	-25.41
1300	-6.42	-29.67	13.33	70.21	-18.39	65.68	-4.44	-27.80
1400	-6.61	-31.21	12.77	67.18	-17.69	63.38	-4.56	-30.22
1500	-6.85	-32.88	12.24	64.24	-17.03	61.24	-4.70	-32.75
1600	-7.07	-34.91	11.76	61.18	-16.36	58.71	-4.84	-35.31
1700	-7.27	-36.84	11.29	58.26	-15.78	56.46	-4.97	-37.89
1800	-7.50	-38.67	10.87	55.30	-15.20	54.05	-5.14	-40.55
1900	-7.76	-41.09	10.46	52.18	-14.67	51.50	-5.32	-43.18
2000	-7.91	-43.60	10.05	49.00	-14.15	48.83	-5.47	-46.10

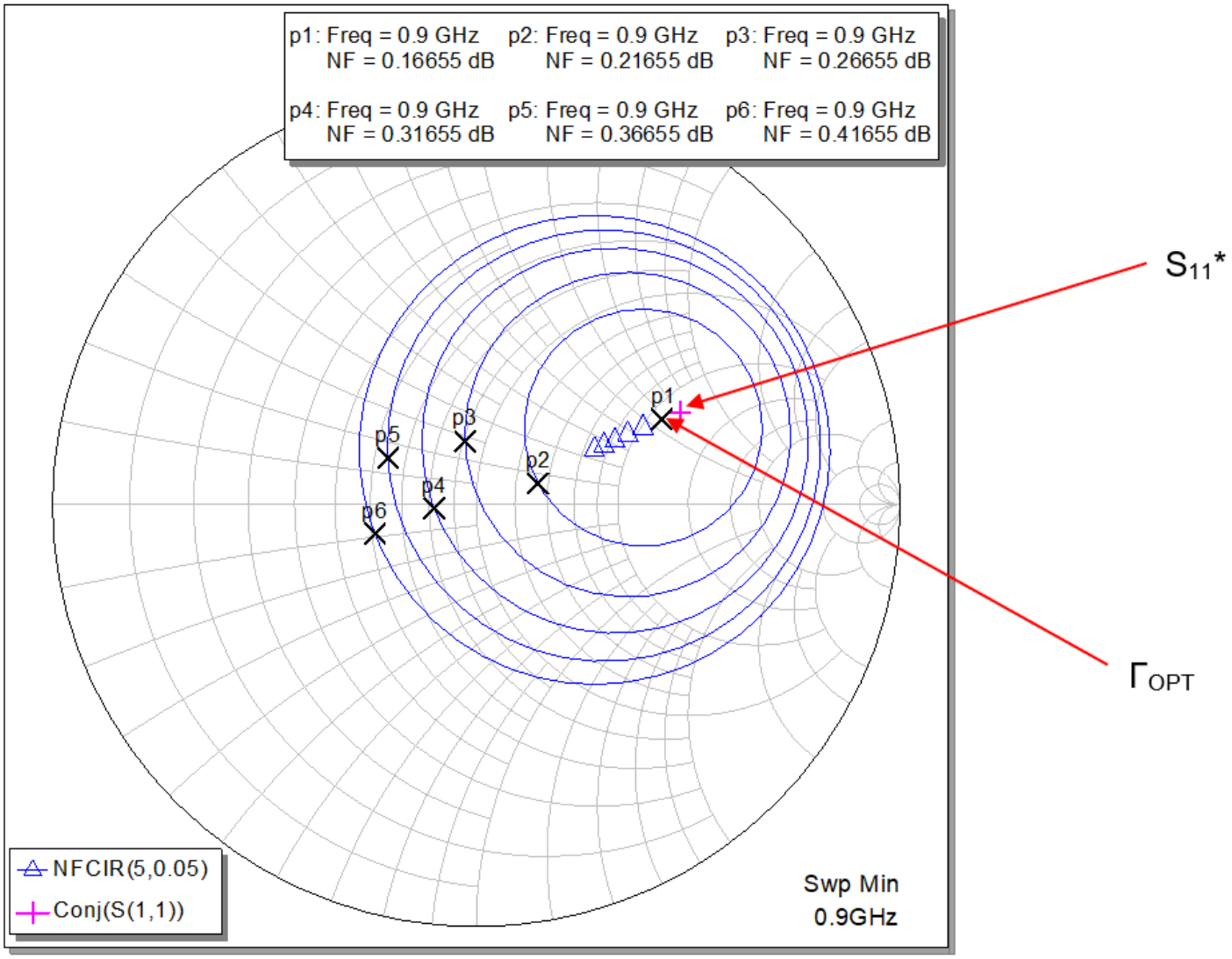
Notes:
1. Test conditions unless otherwise noted: V_{DD}=+4.35 V, I_{DD}=57 mA, Temp=+25°C, 50 Ohm system.

Noise Parameters

Freq (GHz)	NF_{min} (dB)	ΓOpt (mag)	ΓOpt (deg)	Rn (Ω)
0.6	0.13	0.55	15.58	0.06
0.7	0.13	0.54	18.71	0.06
0.75	0.01	0.87	18.77	0.06
0.8	0.14	0.55	21.87	0.06
0.85	0.19	0.47	24.59	0.06
0.9	0.17	0.48	24.86	0.06
0.95	0.15	0.49	25.27	0.06
1.0	0.14	0.58	25.29	0.06
1.1	0.14	0.53	26.97	0.06
1.2	0.18	0.46	27.47	0.06
1.3	0.16	0.40	28.40	0.06
1.4	0.15	0.37	25.37	0.05
1.5	0.33	0.43	-10.36	0.13
1.6	0.32	0.25	3.49	0.06
1.7	0.15	0.31	35.52	0.05
1.8	0.13	0.27	28.27	0.06

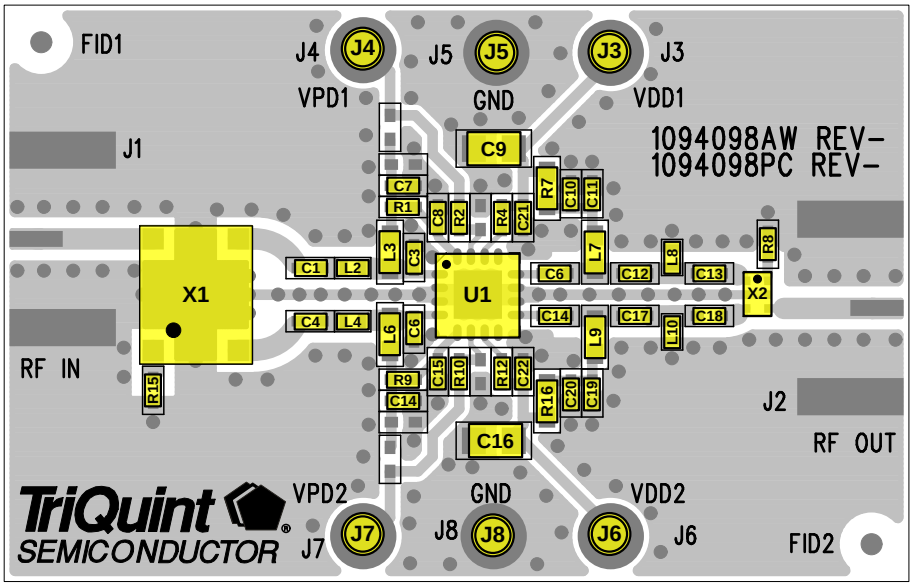
Notes:
1. Test conditions unless otherwise noted: V_{DD}=+4.35 V, I_{DD}=57 mA, Temp=+25°C, 50 Ohm system.

De-embedded S-parameters Data



Notes:
1. Noise parameter measurements taken at the package pin reference plane. The gate and drain are biased externally through bias-tees. The achievable NFmin will worsen with on board non-ideal bias circuit.

TQP3M9039-PCB Evaluation Board (700-1000 MHz)



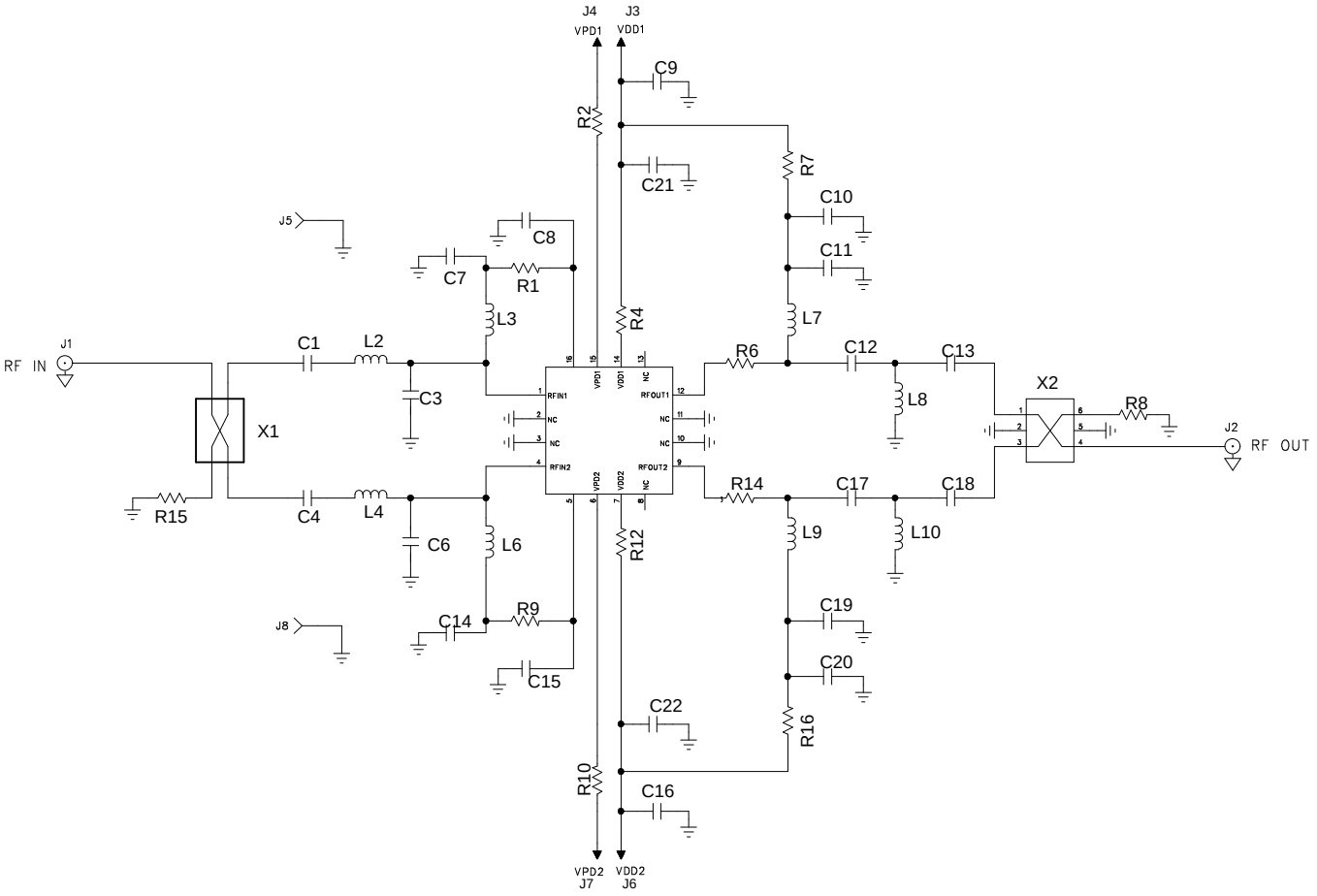
See Evaluation Board PCB Information section for PCB material and stack-up.

Bill of Material – TQP3M9039-PCB

Reference Des.	Value	Description	Manufacturer	Part Number
U1	n/a	Dual LNA	TriQuint	TQP3M9039
X1	n/a	Hybrid coupler	Anaren	X3C09P1-03S
X2	n/a	Hybrid coupler	Anaren	C0810J5003AHF
R1, R9	330 Ω	RES, 0402, +/-5%, 1/10W	Various	
R8, R15	51 Ω	RES, 0402, +/-5%, 1/10W	Various	
R6, R14	10 Ω	RES, 0402, +/-5%, 1/10W	Various	
R4, R12	3K Ω	RES, 0402, +/-5%, 1/10W	Various	
R7, R16	2.2 Ω	RES, 0603, +/-5%, 1/8W	Various	
R2, R10	0 Ω	RES, 0402, +/-5%, 1/10W	Various	
C1, C4	47 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H470J
C3, C6	1.2 pF	CAP, 0402, +/-0.1pF, 25V	Panasonic	ECD-G0E1R2B
C7, C14	1.8 pF	CAP, 0402, +/-0.1pF, 50V	AVX	04025U1R8BAT2A
C8, C15, C21, C22, C11, C19	100 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H101J
C9, C16	0.01 uF	CAP, 0805, +/-5%, 50V, X7R	Various	
C10, C20	1000 pF	CAP, 0402, +/-10%, 50V	Various	
C12, C13, C17, C18	2.2 pF	CAP, 0402, +/-0.1pF, 50V	AVX	04025U2R2BAT2A
L2, L4	6.8 nH	IND, 0402, +/-5%	Coilcraft	0402CS-6N8XJL
L3, L6	220 nH	IND, 0603, +/-5%	Coilcraft	0603CS-R22XJL
L7, L9	47 nH	IND, 0603, +/-5%, 600mA	Coilcraft	0603CS-47NXJL
L8, L10	10 nH	IND, 0402, +/-5%	Coilcraft	0402CS-10NXJL

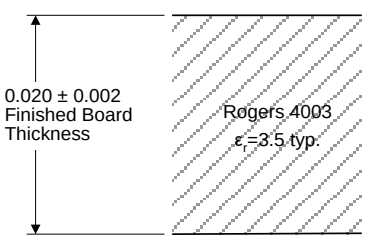
Notes:
1. R2 and R10 may be replaced with metal trace in target applications.

Application Circuit – TQP3M9039-PCB

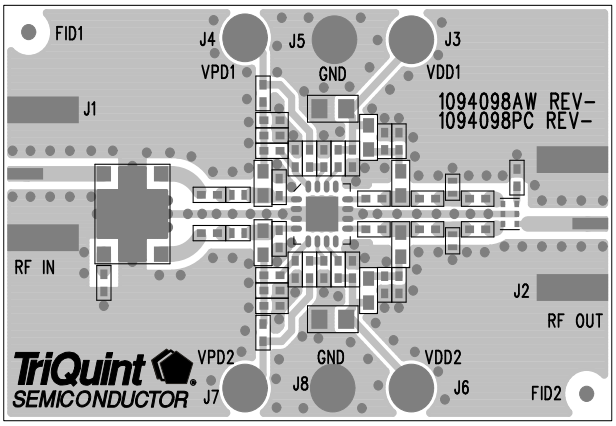


Evaluation Board PCB Information

TriQuint PCB 1094098 Material and Stack-up



50 ohm line dimensions: width = .040”, spacing = .020”

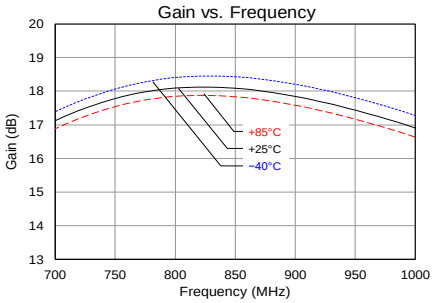


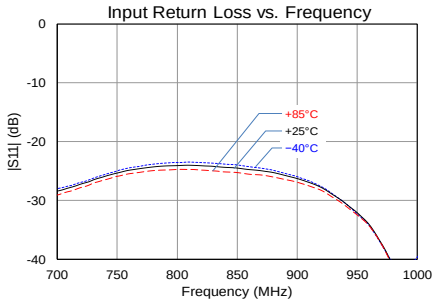
Typical Performance (Balanced Configuration)

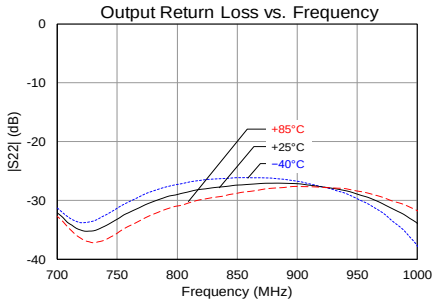
Parameter	Typical Value (1)				Units
Frequency	700	830	900	1000	MHz
Gain	17.1	18.1	17.8	16.8	dB
Noise Figure (Balanced Configuration)	0.62	0.57	0.58	0.66	dB
Input Return Loss	28	24	26	43	dB
Output Return Loss	32	27	27	34	dB
Output P1dB	+21.3	+21.5	+21.0	+20.3	dBm
IIP3 (Pin/tone=−13 dBm, Δf = 1 MHz)	+18.8	+20.7	+21.0	+21.9	dBm

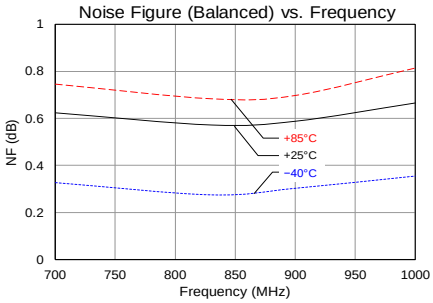
Notes:
1. Test conditions unless otherwise noted: V_{DD}=+4.35 V, I_{DD}=57 mA, Temp=+25°C, 50 Ohm system.
2. NF is de-embedded to the input of the input hybrid coupler.

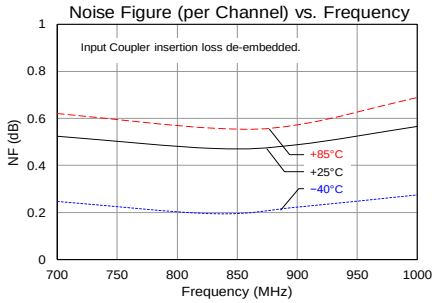
Performance Plots (Balanced Configuration)

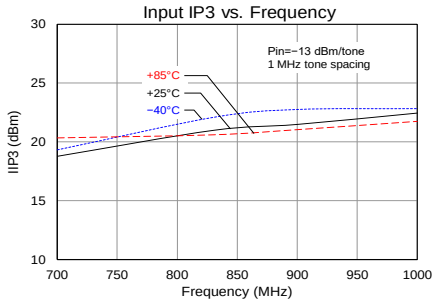


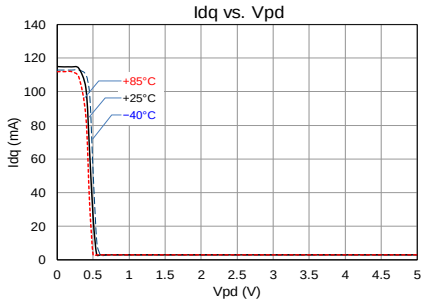






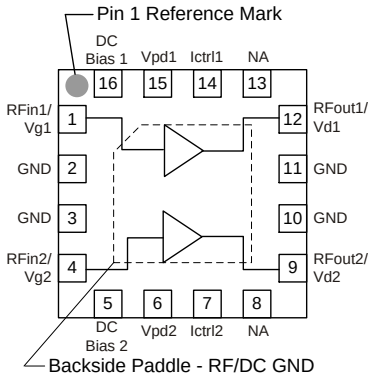






Notes:
1. Test conditions unless otherwise noted: V_{DD}=+4.35 V, I_{DD}=57 mA, Temp=+25°C, 50 Ohm system.

Pad Configuration and Description

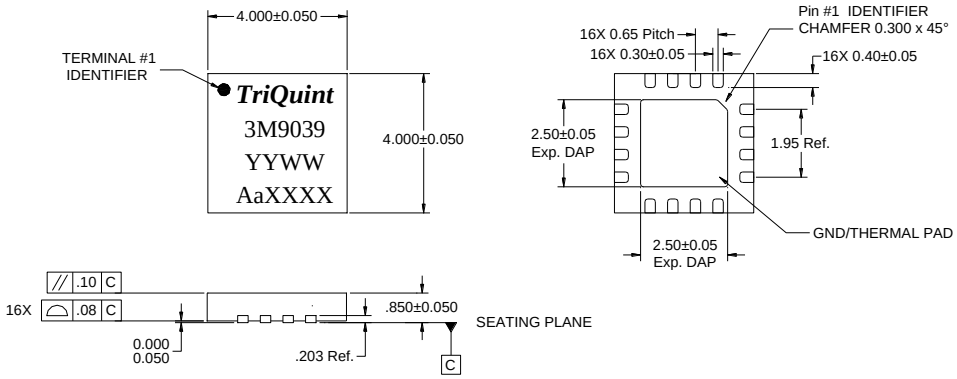


Top View

Pad No.	Label	Description
1	RFin1/Vg1	RF input pin for channel 1. Gate voltage bias pin for channel 1.
2, 3, 10, 11	GND	No internal connection but should be grounded to provide PCB mounting integrity and isolation between the two RF paths.
4	RFin2/Vg2	RF input pin for channel 2. Gate voltage bias pin for channel 2.
5	DC Bias 2	DC out bias for channel 2
6	Vpd2	Power down control voltage for channel 1
7	Ictrl2	Channel 2 drain current control
8, 13	NA	No internal connection. These pins can be grounded to provide PCB mounting integrity.
9	RFout2/Vd2	RF output pin for channel 2. Gate voltage bias pin for channel 2.
12	RFout1/Vd1	RF output pin for channel 1. Drain voltage bias pin for channel 1.
14	Ictrl1	Channel 1 drain current control
15	Vpd1	Power down control voltage for channel 1
16	DC Bias 1	DC out bias for channel 1
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

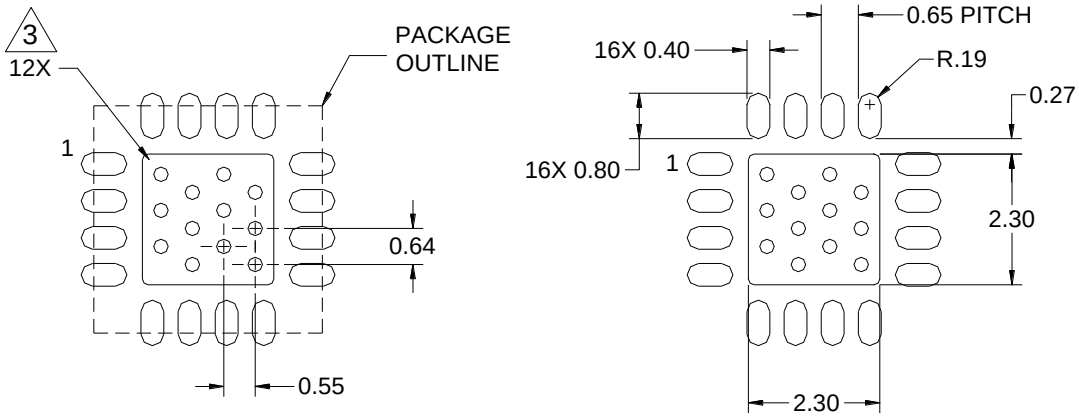
Package Marking and Dimensions

Marking: Part number – 3M9039
Year, week - YYWW
Assembly code - AaXXXX



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012

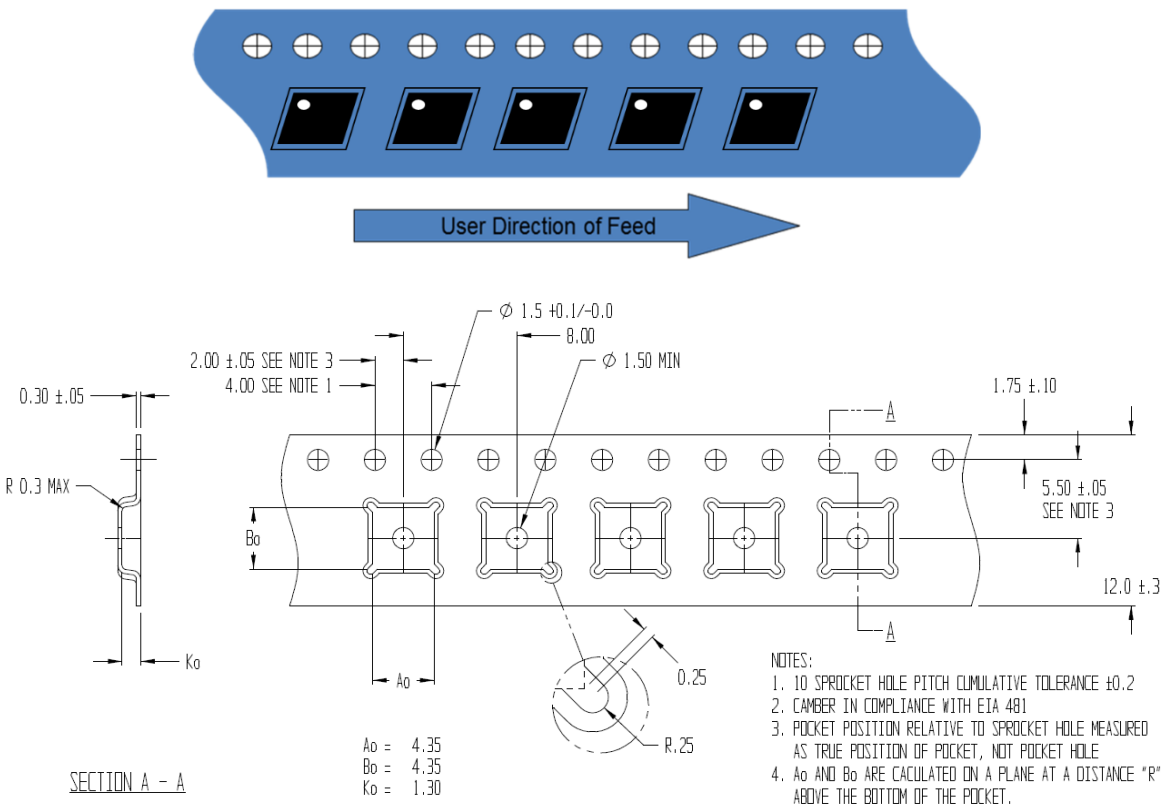
Recommended PCB Layout Pattern



COMPONENT SIDE

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

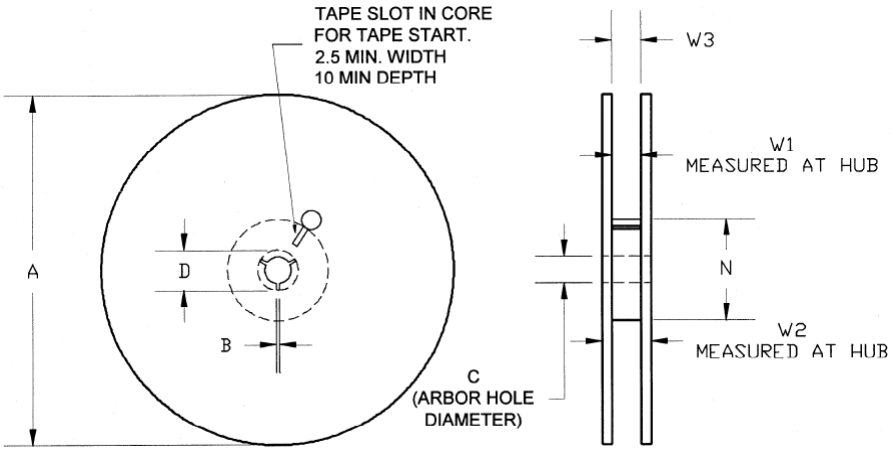
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.171	4.35
	Width	B0	0.171	4.35
	Depth	K0	0.051	1.30
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

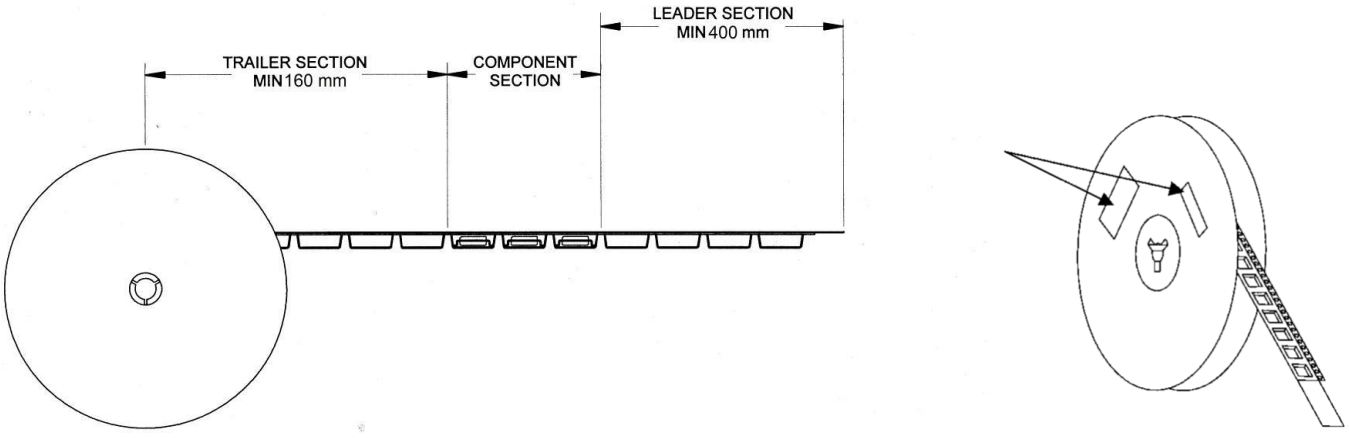
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.795	20.2

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 0B	ESDA / JEDEC JESD22-A114
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 2	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: Ni/Pd/Au *(Electroless Ni 2-5 µm, Electroless Pd 0.11-0.18 µm, Electroless (hybrid) Au 0.07 – 0.12 µm)*

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. **THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.**

Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Qorvo:

TQP3M9040 TQP3M9039 TQP3M9039-PCB