



TGS2355-SM

0.5-6 GHz 100 Watt GaN Switch

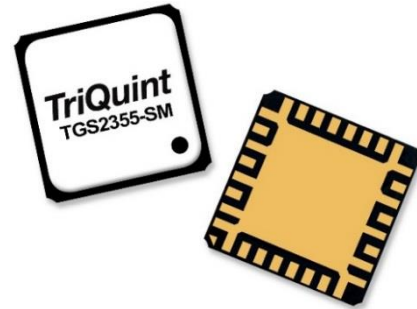
Product Overview

Qorvo's TGS2355-SM is a Single-Pole, Double-Throw (SPDT) reflective switch fabricated on Qorvo's QGaN25 0.25um GaN on SiC production process.

Operating from 0.5 to 6GHz, the TGS2355-SM typically supports up to 100W input power (pulsed) handling at control voltages of 0/-40 V. This switch maintains low insertion loss of 1.1 dB or less and greater than 40 dB isolation, making it ideal for high power switching applications across both defense and commercial platforms.

The TGS2355-SM is offered in a 5 x 5 mm air-cavity QFN package comprised of an aluminum-nitride base with a LCP epoxy-sealed lid. This, along with the minimal DC power consumption, allows for easy system integration.

Lead-free and RoHS compliant.



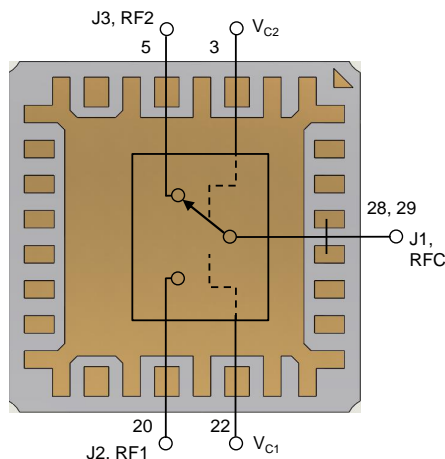
32 Pad 5 x 5 mm QFN Package

Key Features

- Frequency Range: 0.5 – 6 GHz
- Insertion Loss: < 1.1 dB
- Power Handling: 50 dBm (Pulsed)
- Isolation: 40 dB typical.
- Return Loss: > 15 dB
- Control Voltages: 0 V/-40 V
- Switching Speed: < 50 ns
- Reflective Switch
- Package Dimensions: 5.0 x 5.0 x 1.45 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Top View

Applications

- Commercial and Military Radar
- Communications
- Electronic Warfare
- Test Instruments
- General Purpose
- High Power Switching

Ordering Information

Part No.	Description
TGS2355-SM	0.5-6 GHz 100 W GaN Switch
1097066	TGS2355-SM Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Control Voltage (V _c)	-50 V
Control Current (I _c)	-3.5 / +3.5 mA
Power Dissipation	35 W
RF Input Power (pulsed, 10% Duty Cycle, 20us pulse width)	50.5 dBm
RF Input Power, CW, 50Ω, T = 85 °C	47 dBm
Mounting Temperature (30 sec)	260 °C
Storage Temperature	-55 to 150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Frequency	0.5		6	GHz
Operating Temperature Range	-40	+25	+85	°C
Input Power Handling (Pulsed)		50		dBm
Control Voltage		-40		V

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

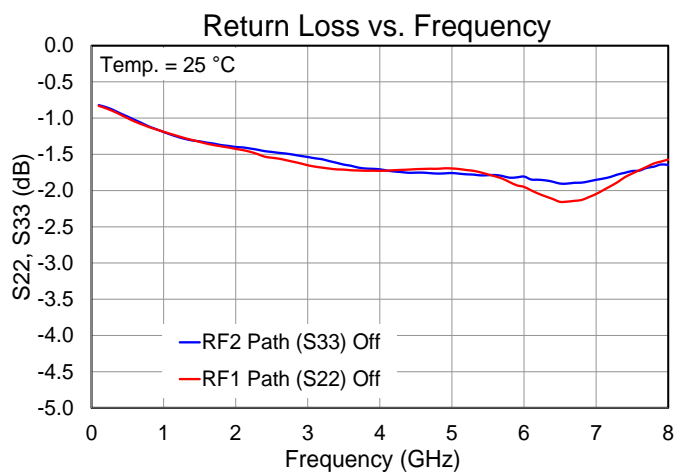
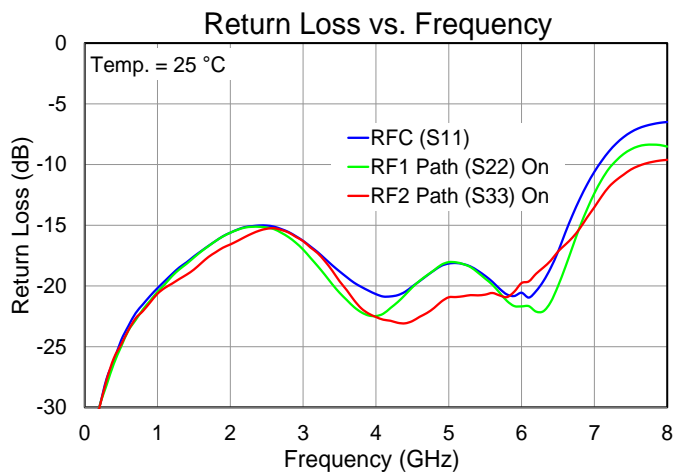
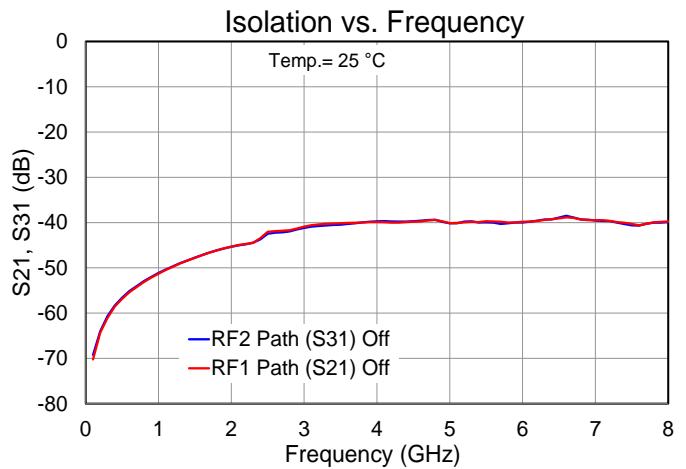
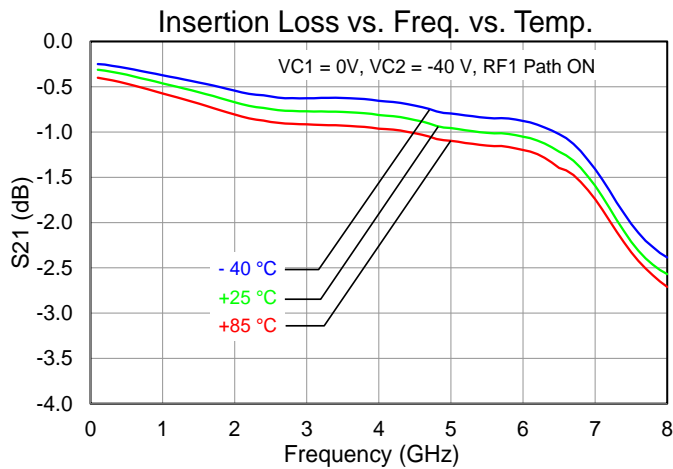
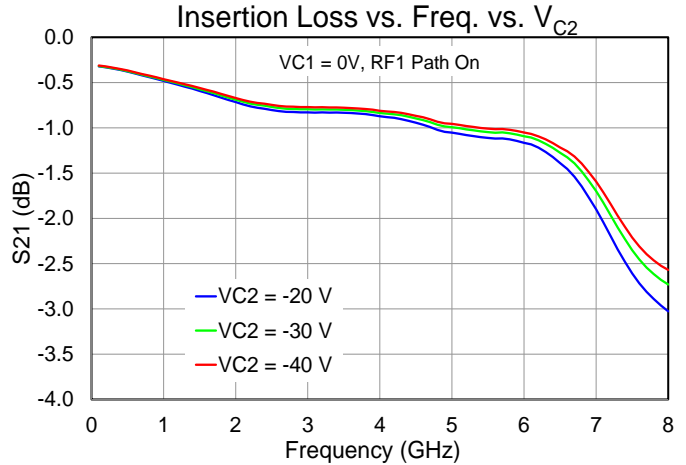
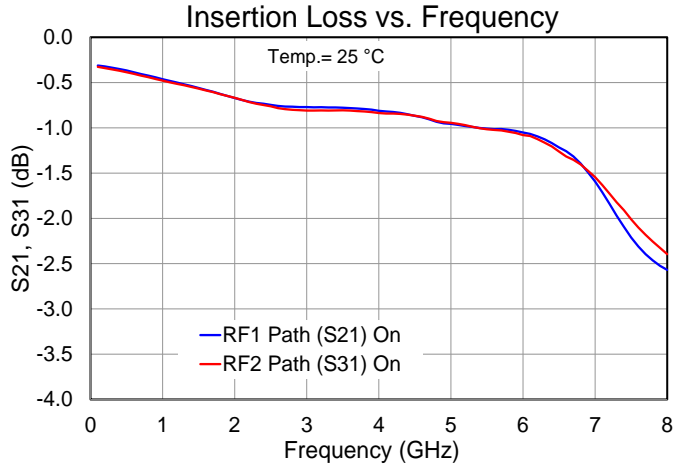
Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Units
Operational Frequency Range		0.5		6	GHz
P _{0.1dB}	Pulsed Input Power		50		dBm
Control Current (I _c)			1.0		mA
Insertion Loss	On-State, 0.5 – 4 GHz		0.7		dB
	On-State, 4 – 6 GHz		1.1		
Input Return Loss – On-State	Common Port Return Loss		15		dB
Output Return Loss – On-State	Switched Port Return Loss		15		dB
Isolation	Off-State		40		dB
Output Return Loss – Off-State (Isolated Port RL)			2.0		dB
Switching Speed (10-90%, 90-10%, V _C =-20V)			50		ns
Third Order Intermodulation Distortion (F _C =4 GHz)			-46		dBc
Second Harmonic Level (F ₀ =4 GHz)			-40		dBc
Control Voltage			-40	-48	V
Insertion Loss Temperature Coefficient			0.004		dB/ °C

Notes:

1. Test conditions unless otherwise noted: Temp= +25°C. Z₀ = 50 Ω, V_c = -40 V, parts mounted to EVB (page 6)

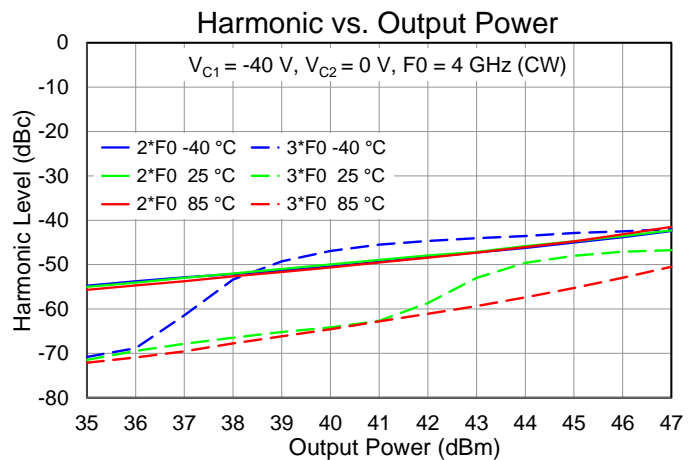
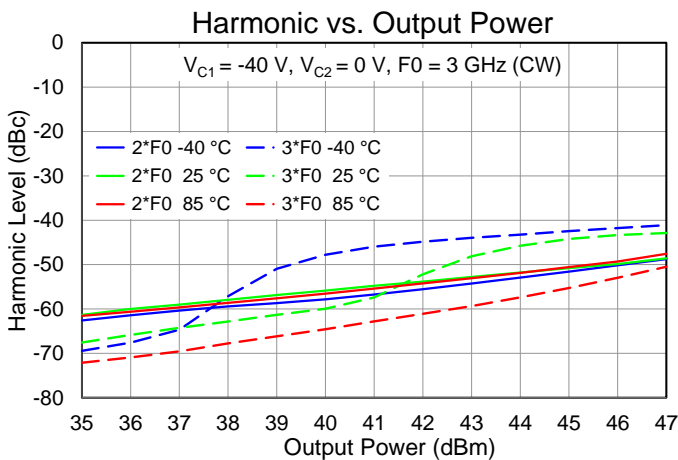
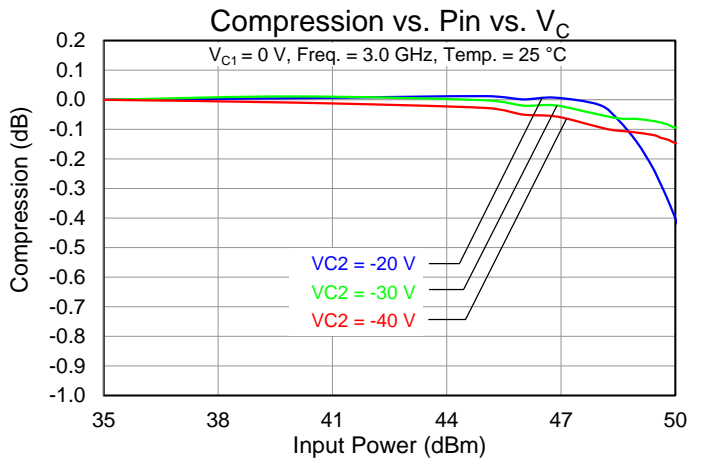
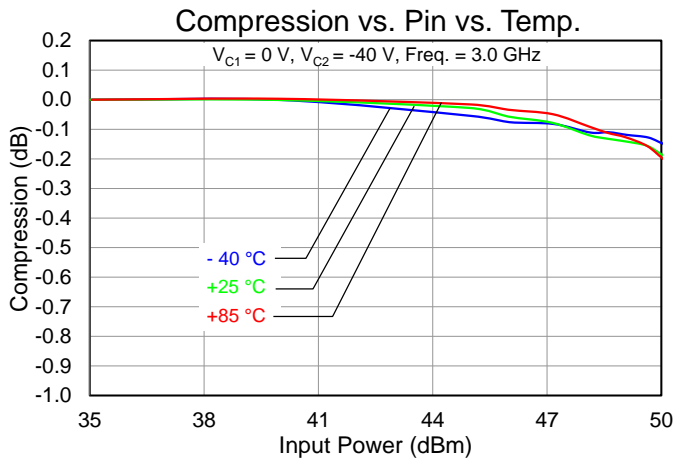
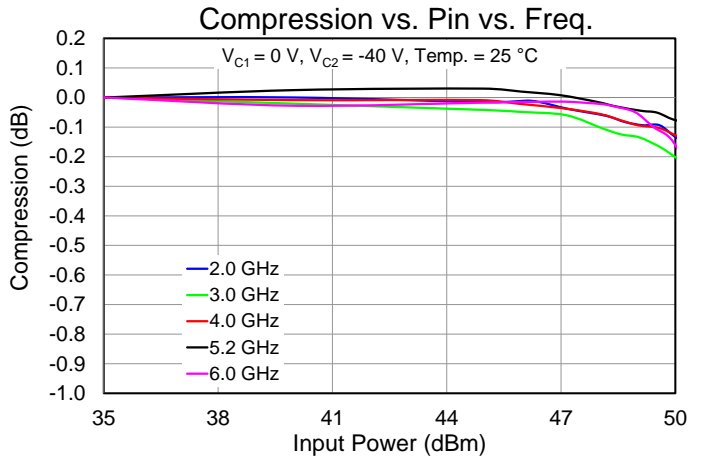
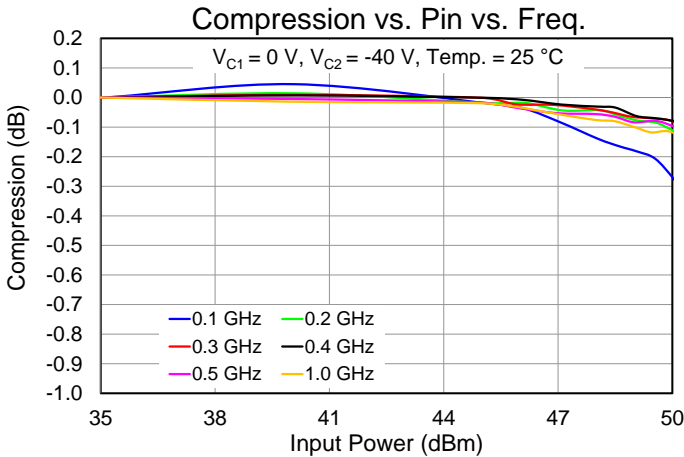
Performance Plots – Small Signal

Test conditions unless otherwise noted: CW RF Input, Temp= +25 °C, parts mounted to EVB (page 6)



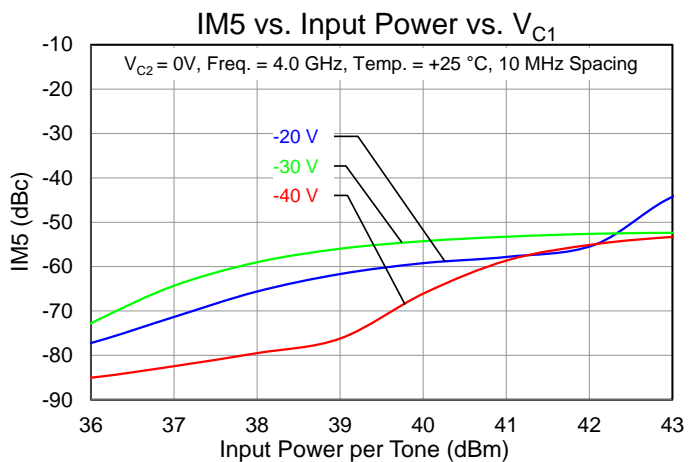
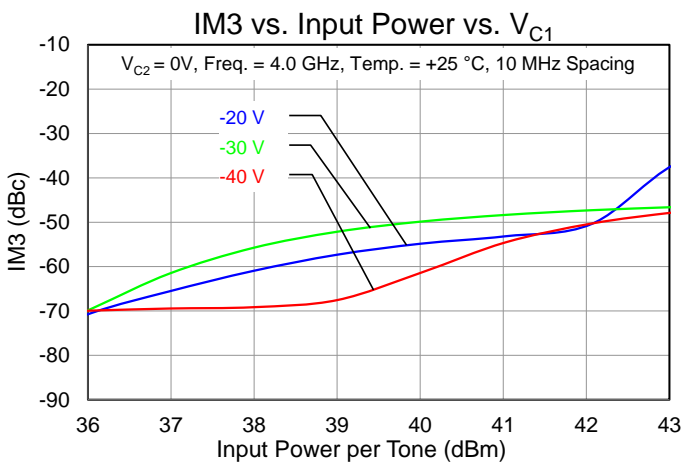
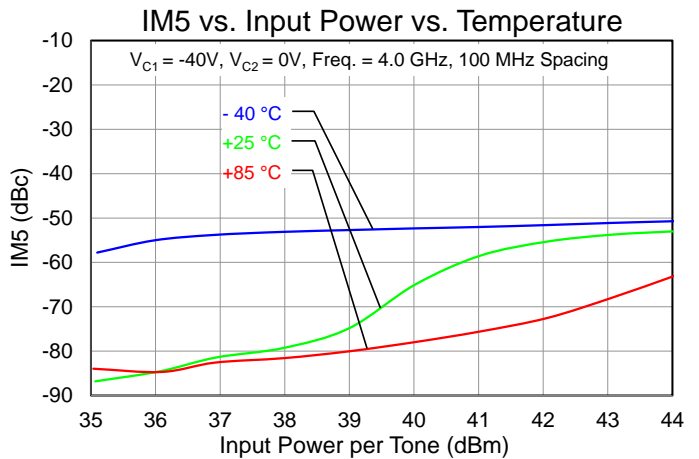
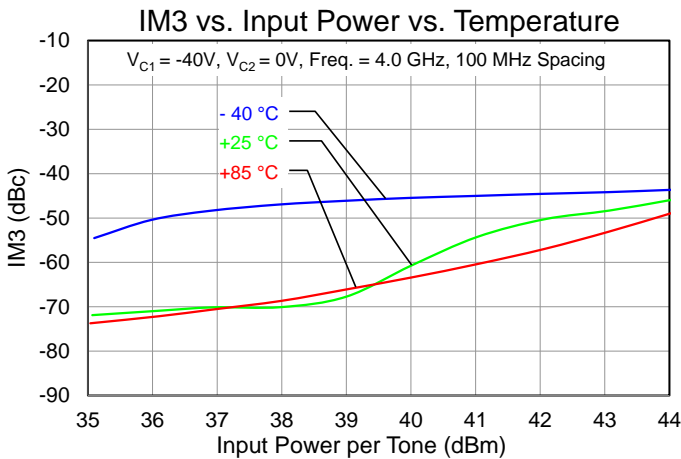
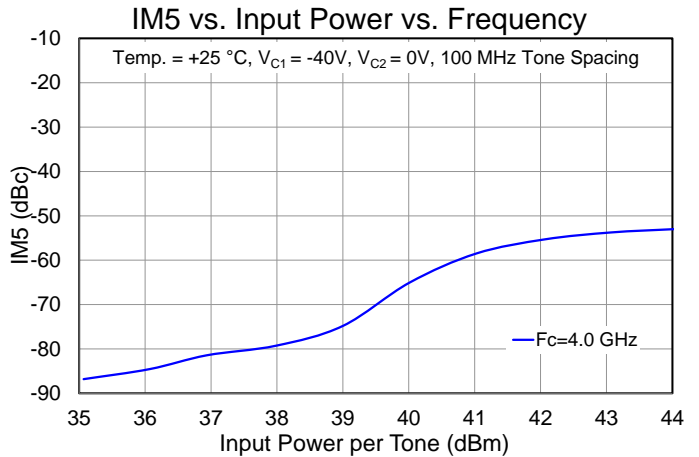
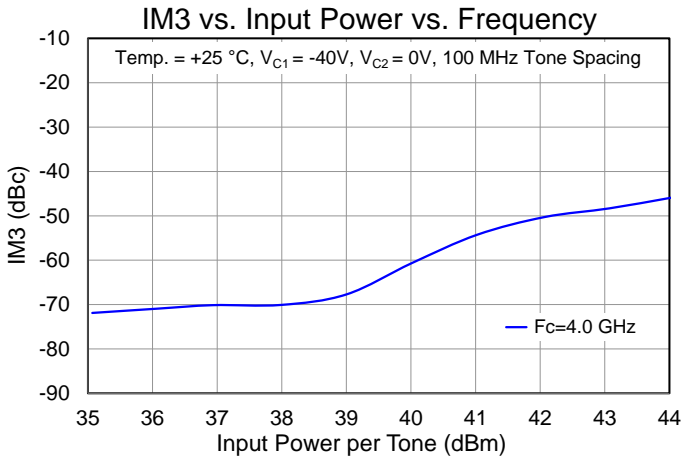
Performance Plots – Compression and Harmonics

Test conditions unless otherwise noted: parts mounted to EVB (page 9), Pulsed Input Power PW=100 us, DC=10%, T=+25 °C



Performance Plots – Linearity

Test conditions unless otherwise noted: CW RF Input, Temp= +25 °C, parts mounted to EVB (page 6)



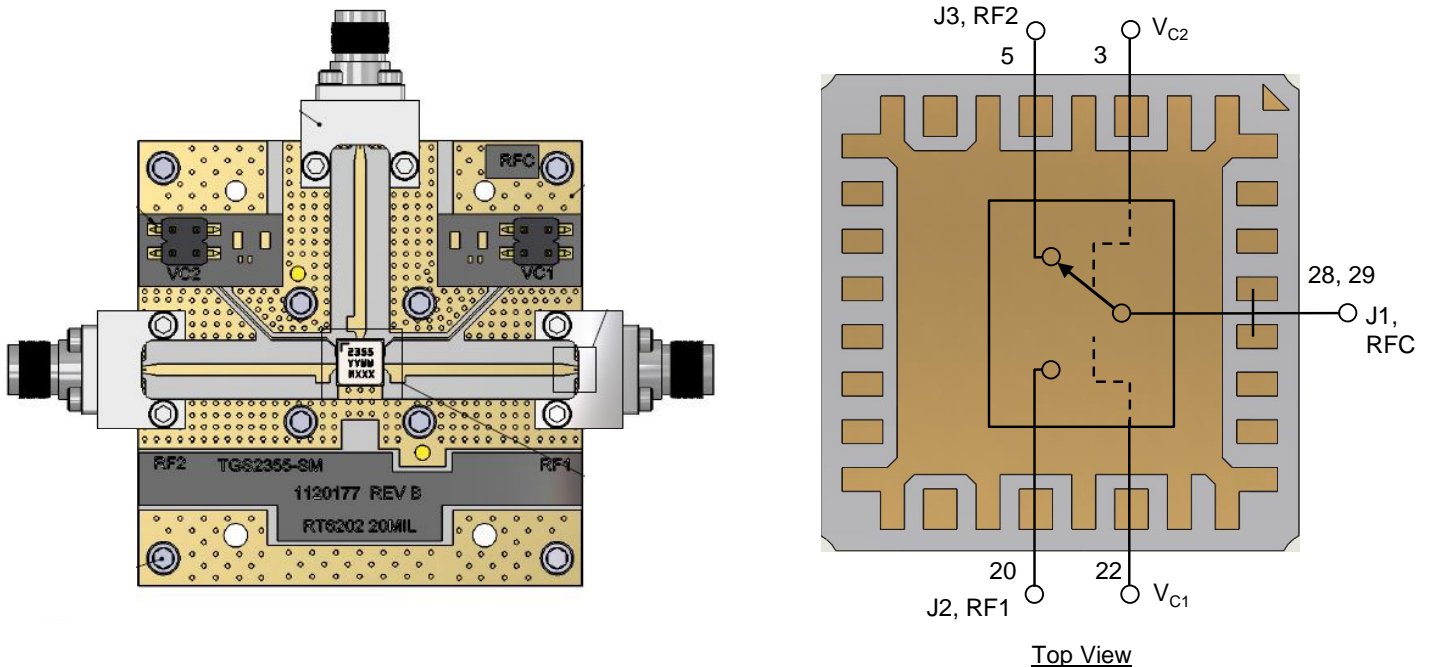
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) ^(1,2)	$T_{BASE} = 85\text{ }^{\circ}\text{C}$, $V_{C1} = 0\text{ V}$, $V_{C2} = -40\text{ V}$, $P_{IN} = 50\text{ W}$, $P_{DISS} = 15\text{ W}$, CW	2.27	$^{\circ}\text{C/W}$
Channel Temperature (T_{CH}) ^(1,2)		119	$^{\circ}\text{C}$
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85\text{ }^{\circ}\text{C}$, $V_{C1} = 0\text{ V}$, $V_{C2} = -40\text{ V}$, $P_{IN} = 100\text{ W}$, $P_{DISS} = 25\text{ W}$, Pulsed Power: PW = 100 us, DC = 10 %	1.52	$^{\circ}\text{C/W}$
Channel Temperature (T_{CH}) ^(1,2)		123	$^{\circ}\text{C}$

Notes:

- MMIC attached to 12 mil AlN QFN base using 0.8 mil thick Diemat 6030 epoxy. Thermal resistance is determined from the channel to the back of the package (fixed 85 °C temperature).
- Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

Evaluation Board (EVB) and Application Circuit



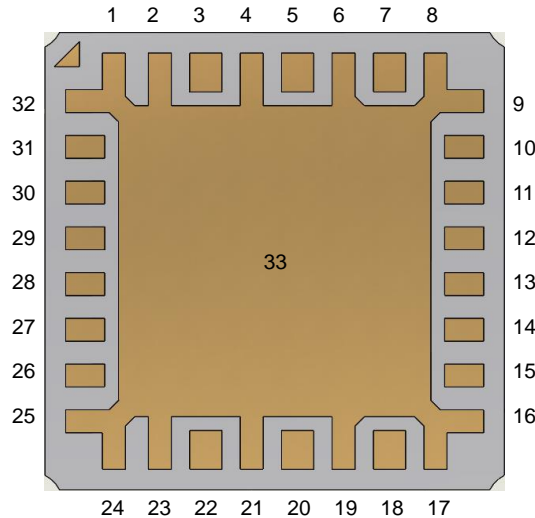
Notes:

- See Evaluation Board PCB Information for material and stack up.
- DC blocking capacitors are required on all RF ports.
- This switch can be configured as a Single Pole, Single Throw (SPST) by terminating one unused RF switched port with a 50 Ohm load.
- Tabs (as shown) on RF transmission lines are required to achieve best electrical performance.

Function Table

RF Path	State	V_{C1}	V_{C2}
RFC to RF1 (50 Ω load to RF2)	On-State (Insertion Loss)	0 V	-40 V
	Off-State (Isolation)	-40 V	0 V
RFC to RF2 (50 Ω load to RF1)	On-State (Insertion Loss)	-40 V	0 V
	Off-State (Isolation)	0 V	-40 V

Pad Configuration and Description

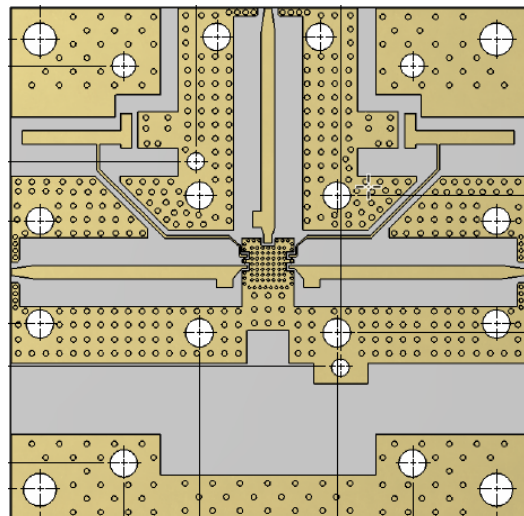
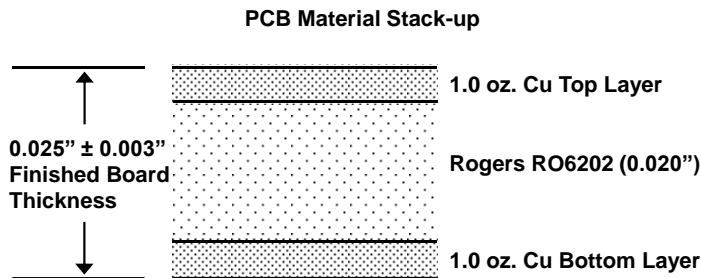


Bottom View

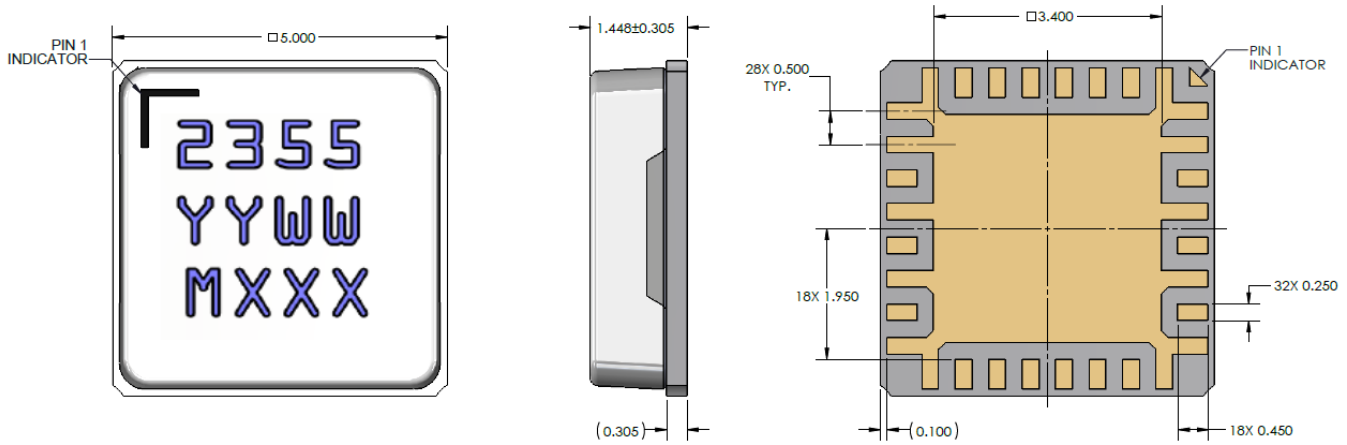
Pad No.	Label	Description
28, 29	RFC	RF common port; matched to 50 Ω; DC coupled
22	VC1	Control voltage 1
3	VC2	Control voltage 2
5	RF2	RF switched port 2; matched to 50 Ω; DC coupled
20	RF1	RF switched port 1; matched to 50 Ω; DC coupled
1-2, 4, 6-19, 21, 23-27, 30-32	GND	Connected to ground paddle (33); must be grounded to PCB to improve isolation.
33	GND	Backside paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

Evaluation Board PCB Information

PC Board Layout



Package Marking and Dimensions



Package lead finish:

Ni / Au plating

Materials:

Base: Ceramic, Lid: Plastic, Part is epoxy sealed

Part Marking:

2355 = Part Number, YY = Part Assembly Year, WW = Part Assembly Week, MXXX = Batch ID

Unless otherwise specified dimensions are in mm.

Tolerances: XX = ±.25, XXX = ± 0.127

Assembly Notes

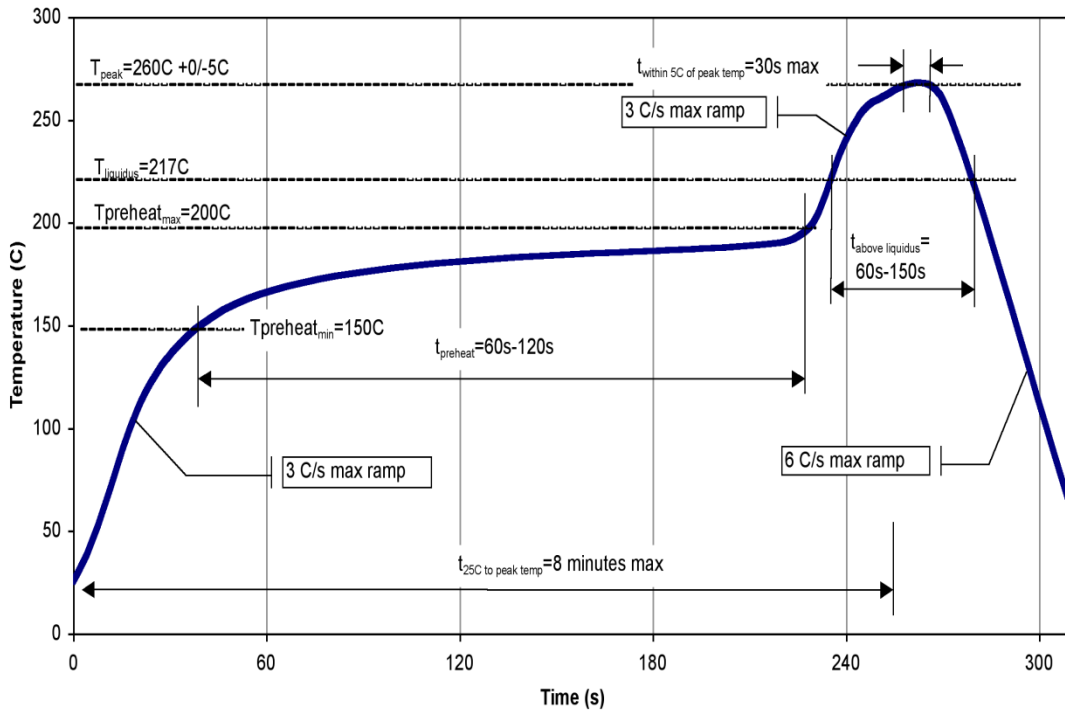
Compatible with lead-free soldering processes with 260°C peak reflow temperature.

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended.

Contact plating: Ni-Au

Solder rework not recommended

Recommended Soldering Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA / JEDEC JESD22-A114
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
 ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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