

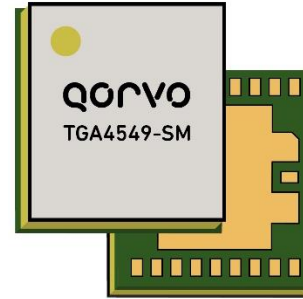
Product Overview

Qorvo's TGA4549-SM is a high frequency, high power MMIC amplifier fabricated on Qorvo's production 0.15um GaN on SiC process (QGaN15). The TGA4549-SM operates from 21.2 – 23.6 GHz and typically provides 10 W saturated output power with power-added efficiency of 20% and large-signal gain of 17 dB. This combination of high frequency performance provides the flexibility designers are looking for to improve system performance while reducing size and cost. The TGA4549-SM also has an integrated power detector to support system diagnostics and other needs.

The TGA4549-SM is offered in a small 5x5.5 mm surface mount package, matched to 50Ω with integrated DC blocking capacitors on both RF ports simplifying system integration. The frequency coverage and operational flexibility allows it support satellite communication as well as point to point data links.

The TGA4549-SM is 100% DC and RF on-wafer tested to ensure compliance to electrical specifications.

Lead-free and RoHS compliant.



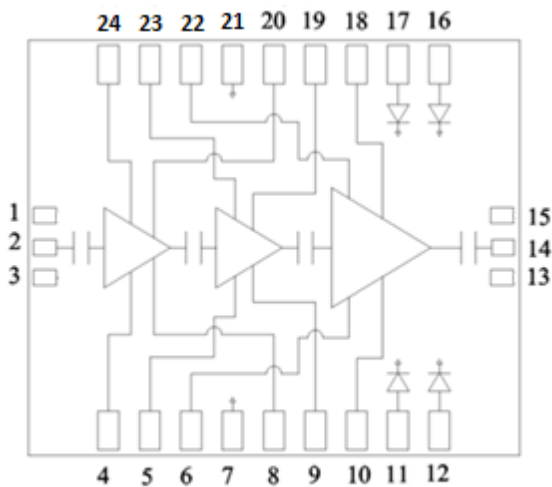
24-Lead 5.0 x 5.5 x 1.7 mm Air Cavity Laminate Package

Key Features

- Frequency Range: 21.2 – 23.6 GHz
- P_{SAT} ($P_{IN}=23$ dBm): 40 dBm
- PAE ($P_{IN}=23$ dBm): 20 %
- Small Signal Gain: 22 dB
- Large Signal Gain: 17 dB
- Integrated Power Detector
- Bias: $V_{D1} = V_{D2} = V_{D3} = +28$ V, $I_{D1} + I_{D2} + I_{D3} = 300$ mA
- Package Dimensions: 5.0 x 5.5 x 1.7 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Point-to-Point Radio
- Satellite Communications

Ordering Information

| Part No. | Description |
|-----------------|------------------------------------|
| TGA4549-SM | 21.2 – 23.6 GHz 10 W GaN PA |
| TGA4549-SMTR7X | 200 pieces on a 7" reel (standard) |
| TGA4549-SMTR7 | 500 pieces on a 7" reel |
| TGA4549-SMEVB01 | Evaluation Board |

Absolute Maximum Ratings

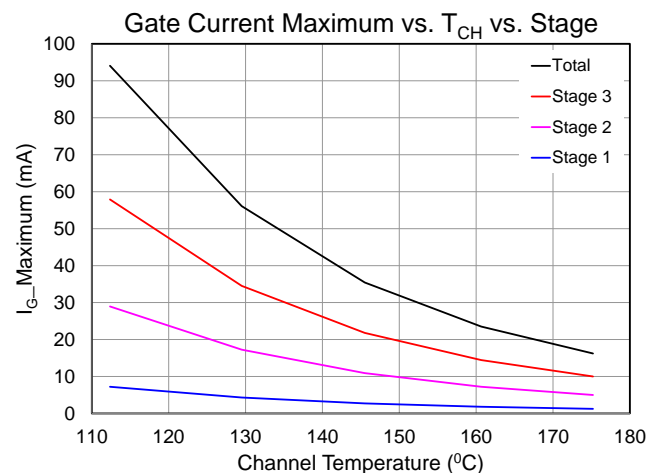
| Parameter | Rating |
|--|----------------|
| Drain Voltage (V_D) | 29.5 V |
| Gate Voltage Range (V_G) | -8 to 0 V |
| Drain Current Stage 1 (I_{D1}), Top or Bottom | 500 mA |
| Drain Current Stage 2 (I_{D2}), Top or Bottom | 500 mA |
| Drain Current Stage 3 (I_{D3}), Top and Bottom | 2 A |
| Gate Current (I_G), | See chart |
| RF Input Power, CW, 50 Ω , T=25 °C | 26 dBm |
| Dissipated Power (P_{DISS}), CW, 85 °C | 45 W |
| Reference Diode Current (I_{ref}) | 4 mA |
| Detector Diode Current (I_{det}) | 4 mA |
| Storage Temperature | -55 to +150 °C |
| Mounting Temperature (30 seconds) | 260 °C |

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|---------------------------------------|------------------|-----|-----|-------|
| Drain Voltage (V_D) | | +28 | | V |
| Drain Current, Quiescent (I_{DQ}) | | 300 | | mA |
| Drain Current, RF (I_{D_Drive}) | See chart page 5 | | | mA |
| Gate Voltage Typ. Range (V_G) | -2.1 to -2.8 | | | V |
| Gate Current, RF (I_{G_Drive}) | See chart page 5 | | | mA |
| Operating Temp. Range | -40 | +25 | +85 | °C |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.



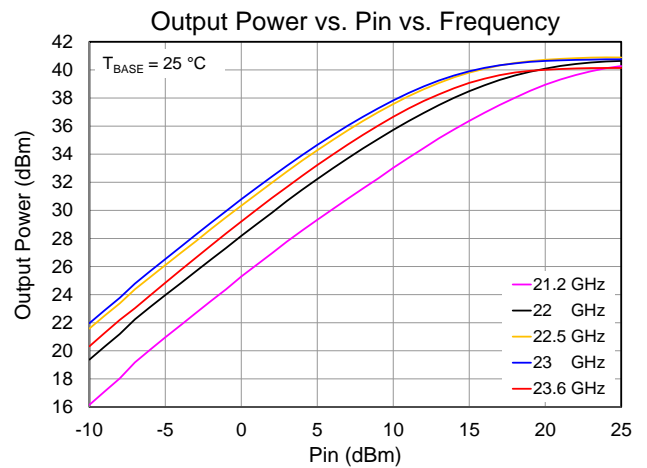
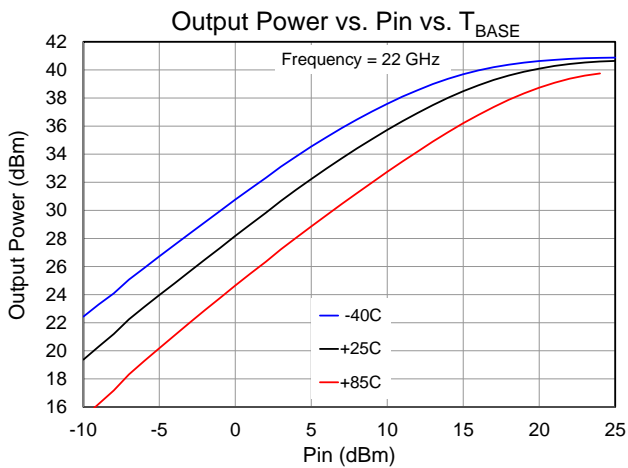
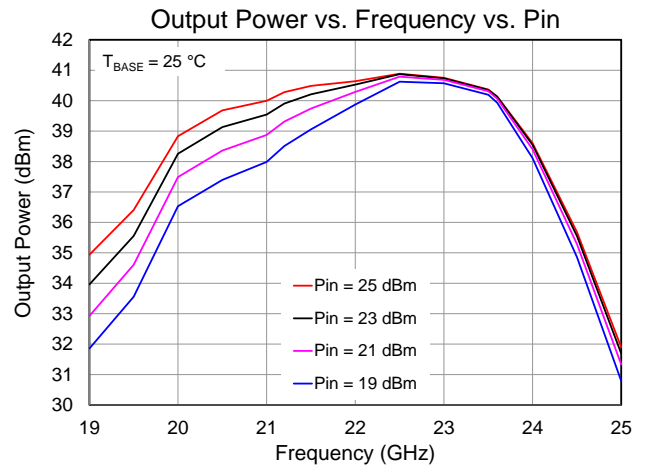
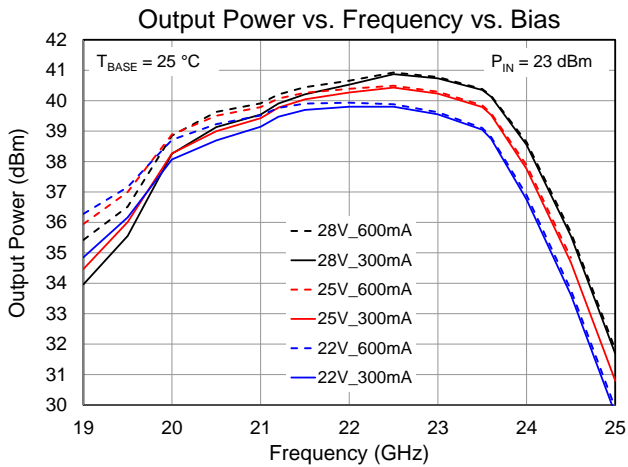
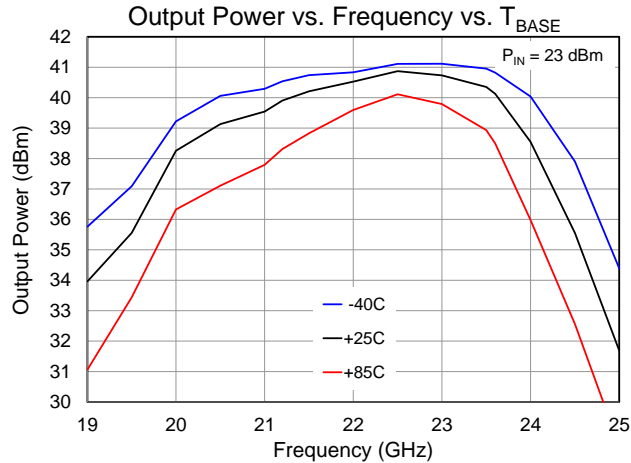
Electrical Specifications

| Parameter | Conditions ^{(1) (2)} | Min | Typ | Max | Units |
|---------------------------------------|--|------|-------|------|--------|
| Operational Frequency Range | | 21.2 | | 23.6 | GHz |
| Small Signal Gain, S21 | | | 22 | | dB |
| Input Return Loss, IRL | | | 9 | | dB |
| Output Return Loss, ORL | | | 12 | | dB |
| Output Power at Saturation, P_{SAT} | $P_{IN} = +23$ dBm | | 40 | | dBm |
| Power Added Efficiency, PAE | $P_{IN} = +23$ dBm | | 20 | | % |
| Third Order Intermodulation, IM3 | $P_{OUT} = +34$ dBm/tone | | 25 | | dBc |
| S21 Temperature Coefficient | $T_{diff} = (85 - (-40))$ °C | | -0.03 | | dB/°C |
| P_{SAT} Temperature Coefficient | $T_{diff} = (85 - (-40))$ °C, $P_{in} = +23$ dBm | | -0.02 | | dBm/°C |
| Gate Leakage | $V_D = +28$ V, $V_G = -5$ V | -8 | -1 | 0 | mA |

- Notes:
- Test conditions unless otherwise noted: CW, $V_{D1} = V_{D2} = V_{D3} = 28$ V, $I_{D1} + I_{D2} + I_{D3} = 300$ mA, adjusting $V_{G1} = V_{G2} = V_{G3}$, $T_{BASE} = +25$ °C, $Z_0 = 50$ Ω
 - T_{BASE} is back side of package

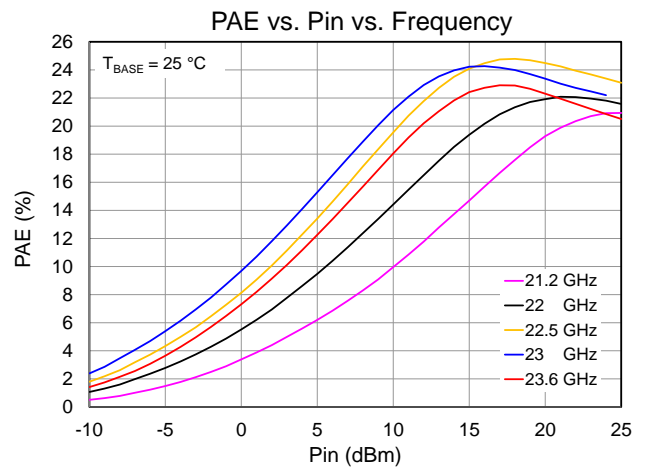
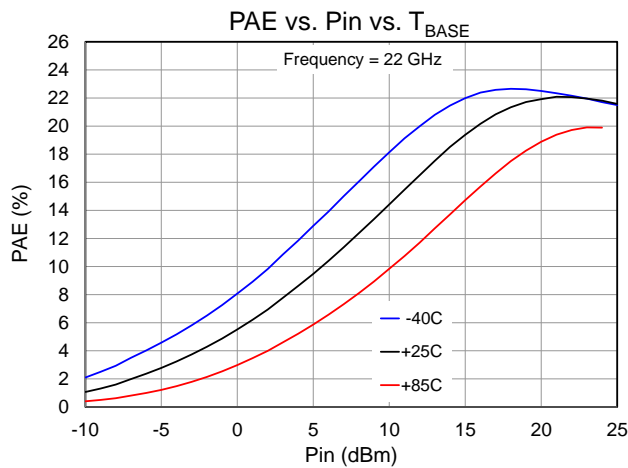
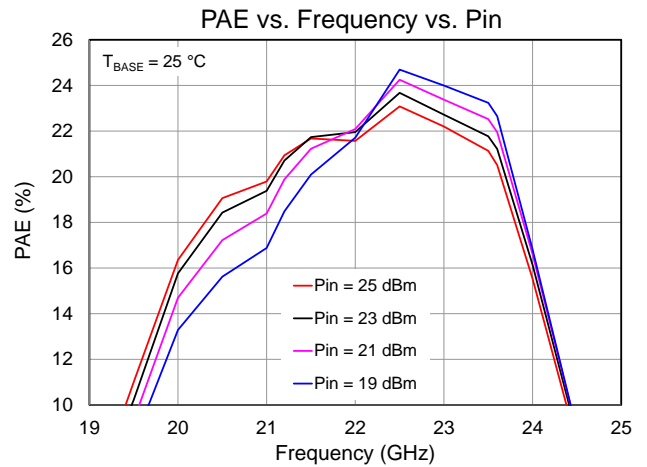
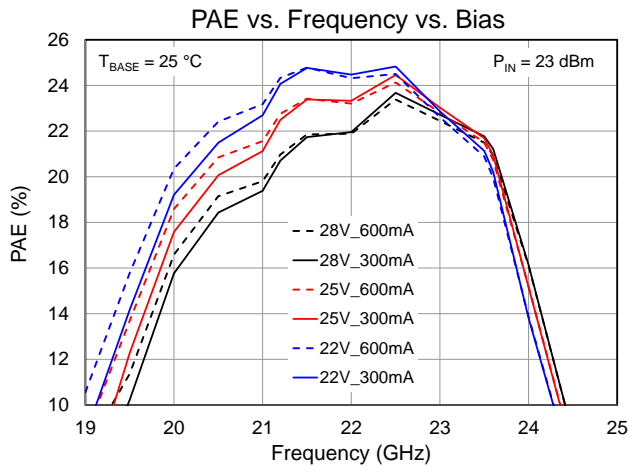
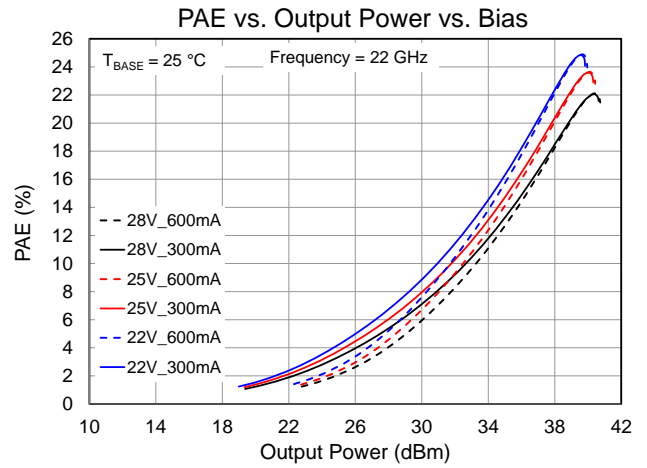
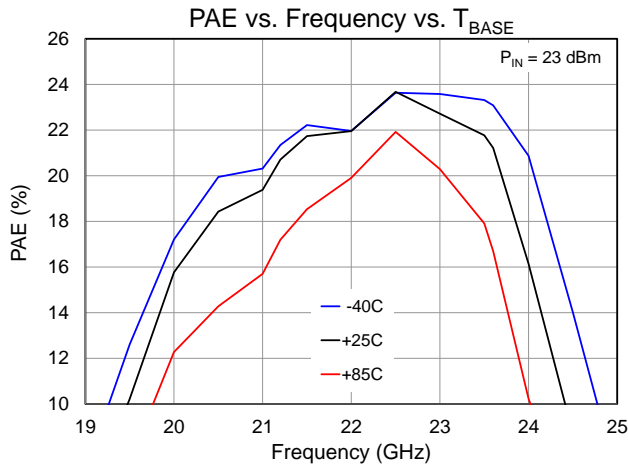
Performance Plots – Large Signal

Test conditions unless otherwise noted: CW, $V_{D1} = V_{D2} = V_{D3} = 28V$, $I_{D1} + I_{D2} + I_{D3} = 300mA$, adjusting $V_{G1} = V_{G2} = V_{G3}$, $T_{BASE} = +25\text{ }^{\circ}C$, $Z_0 = 50\ \Omega$



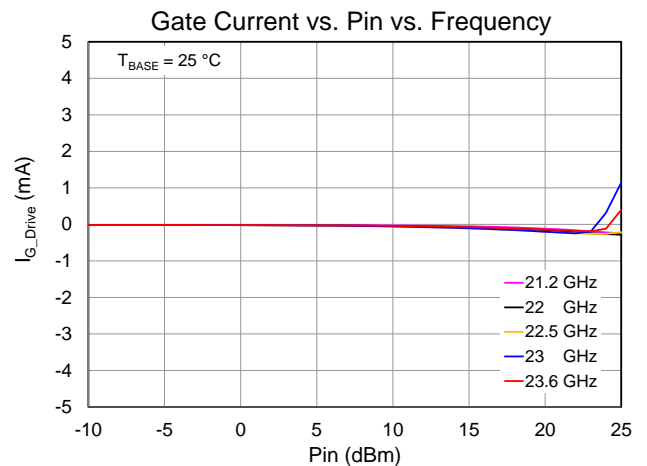
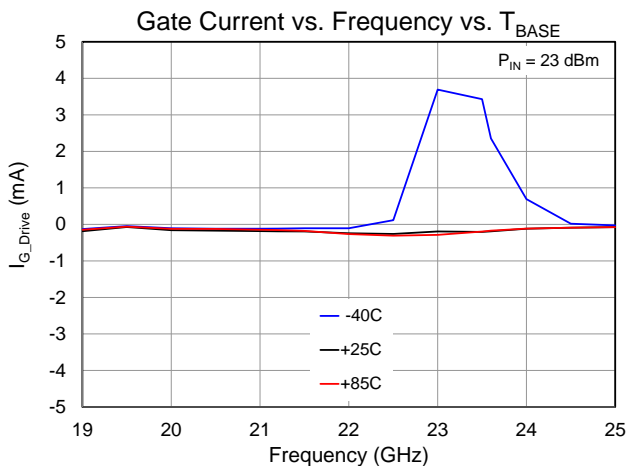
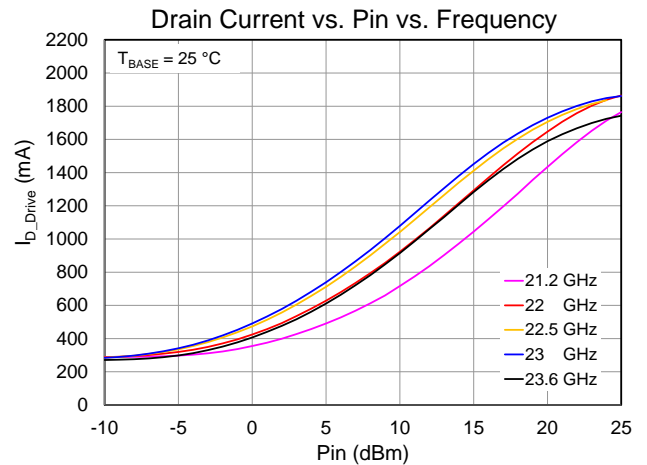
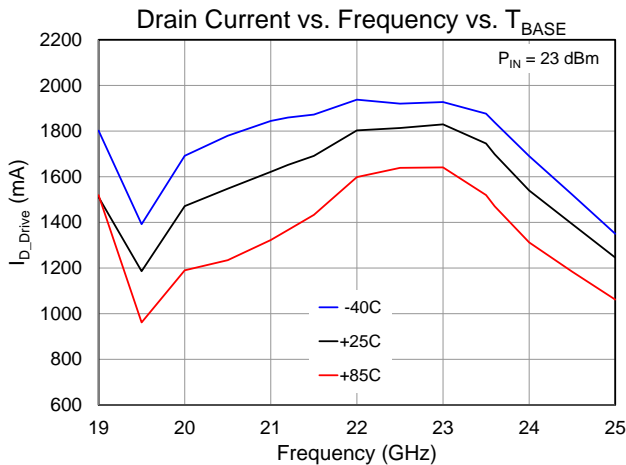
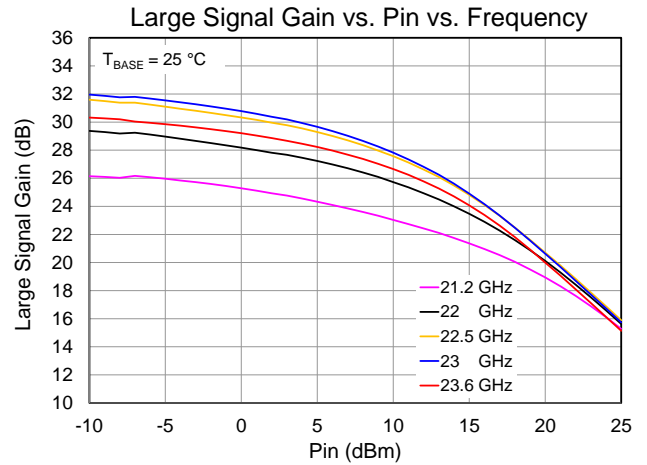
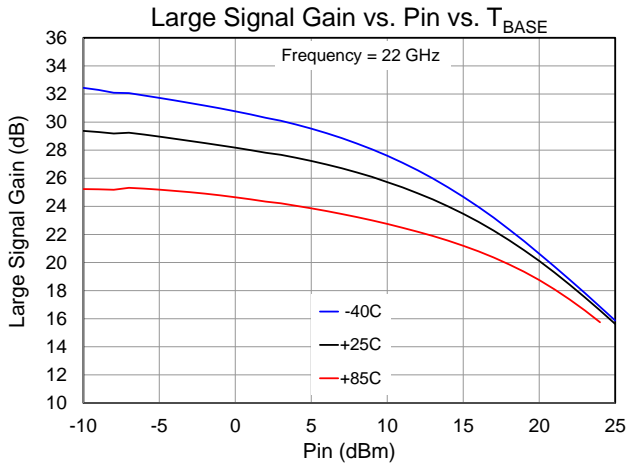
Performance Plots – Large Signal

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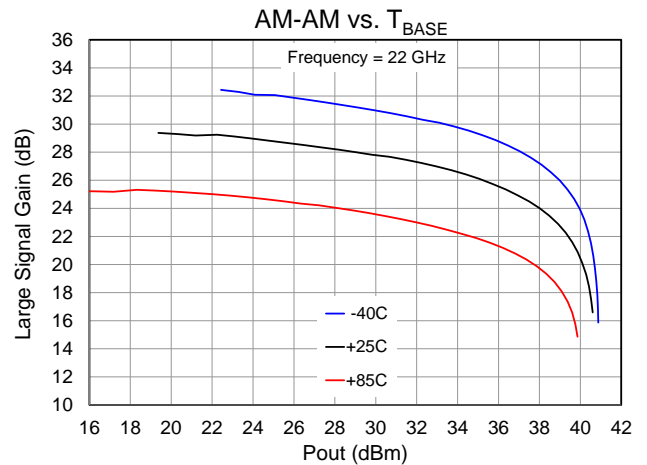
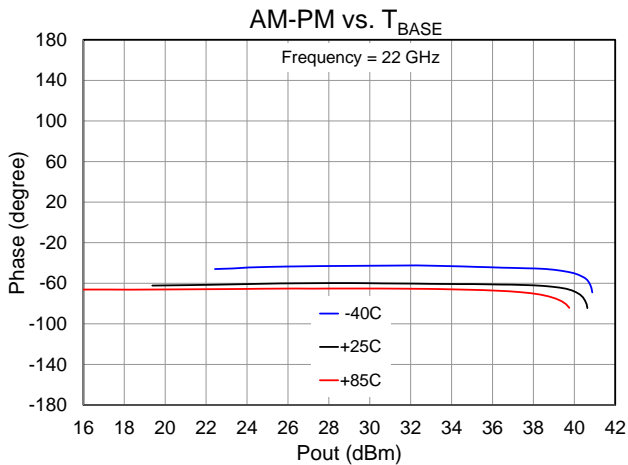
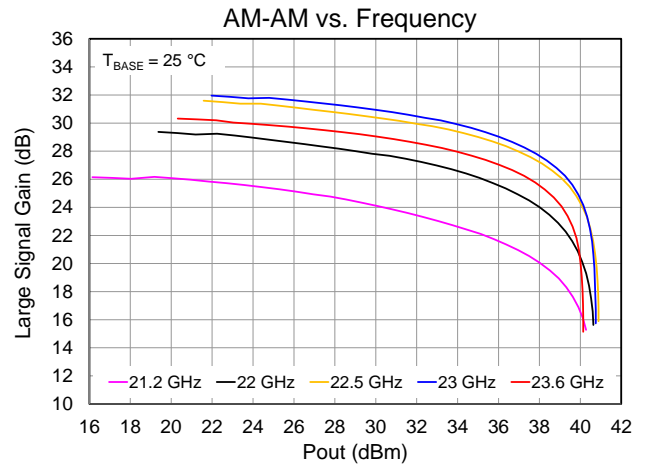
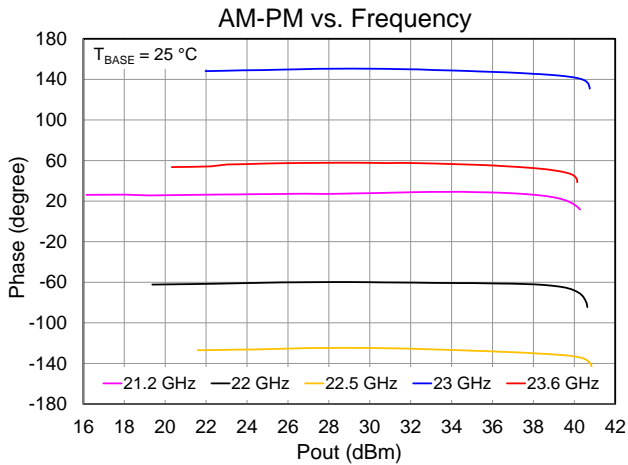
Performance Plots – Large Signal

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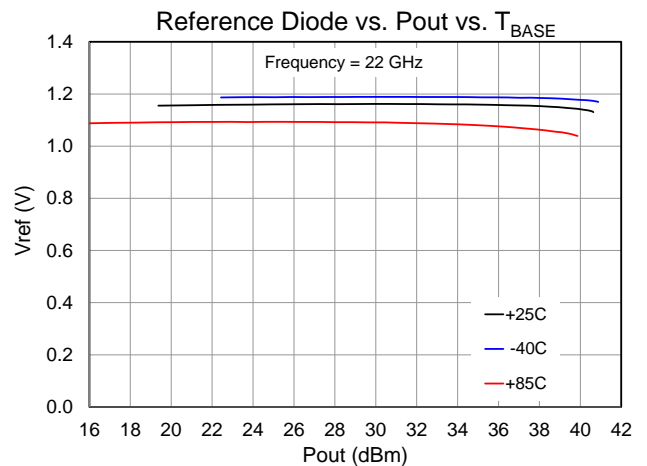
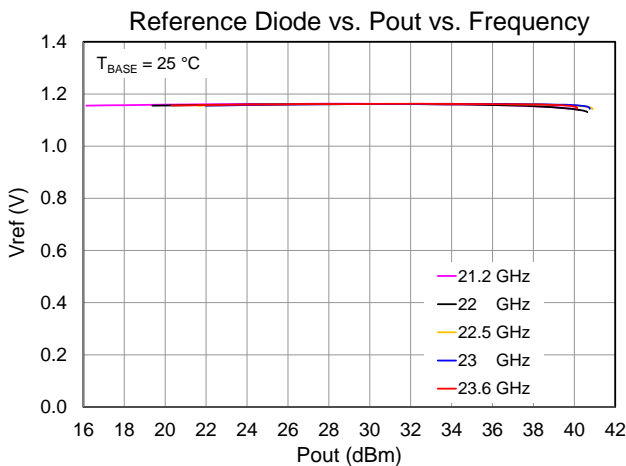
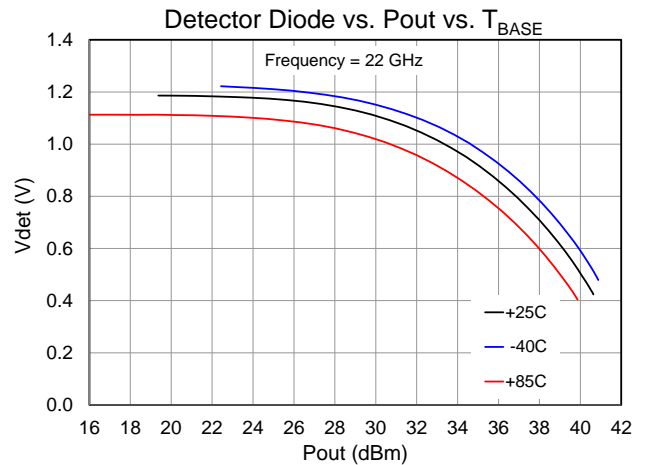
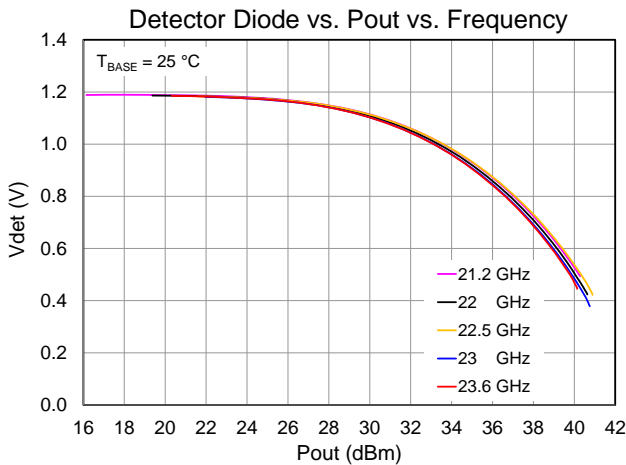
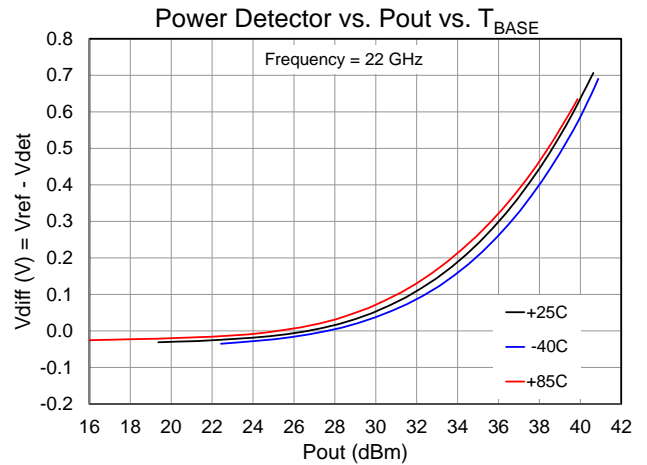
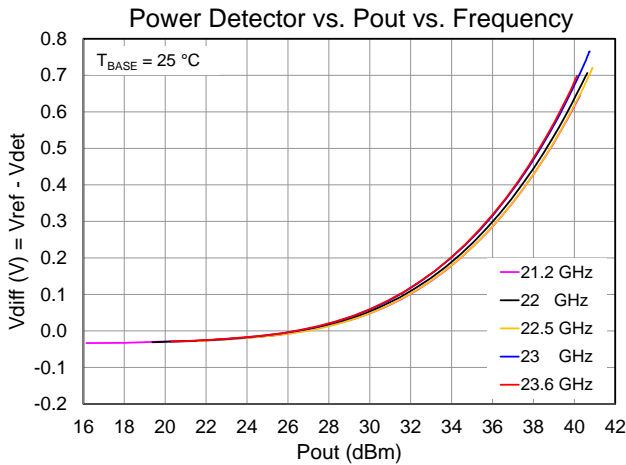
Performance Plots – Large Signal

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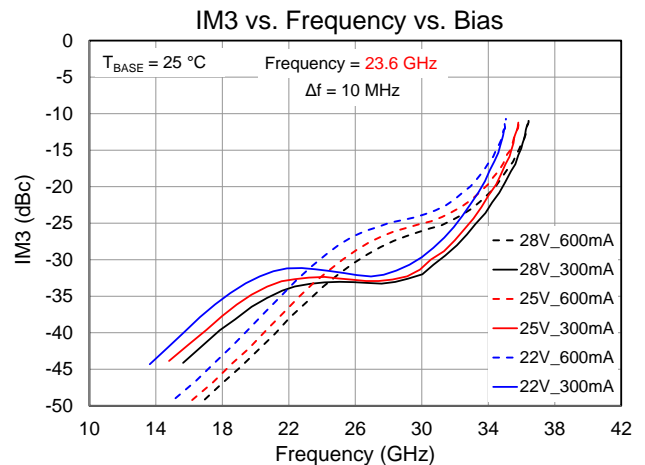
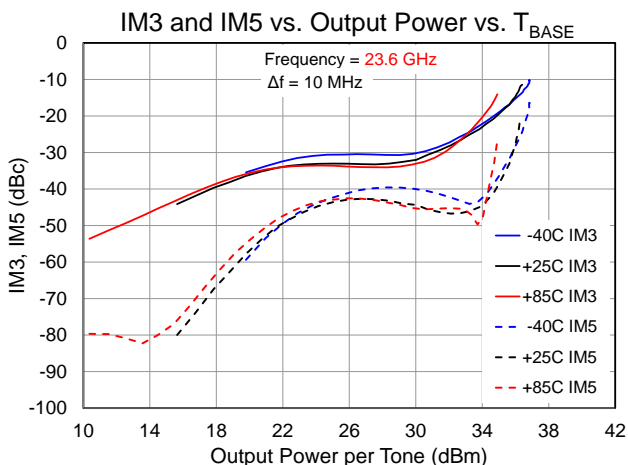
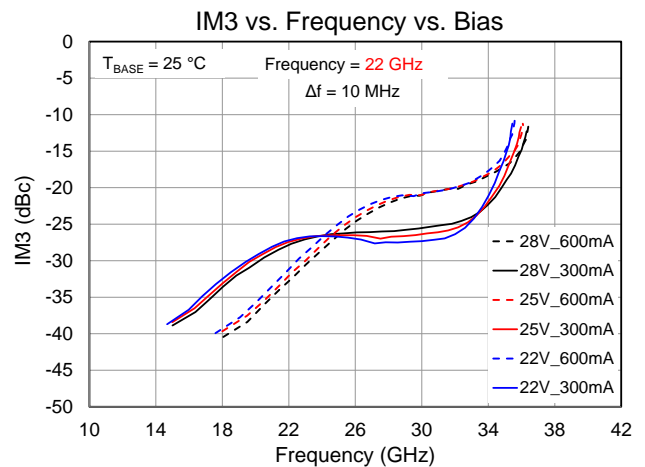
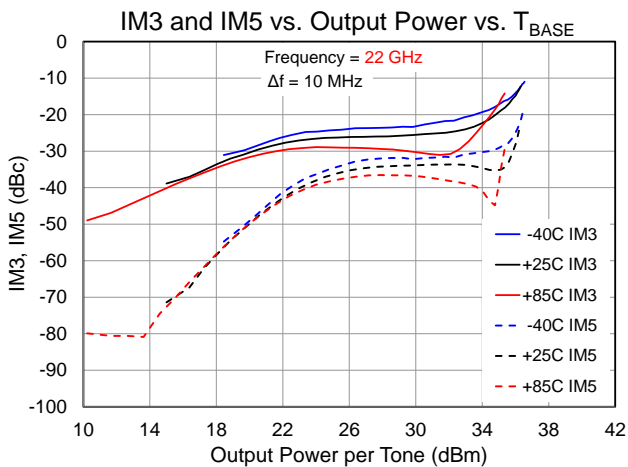
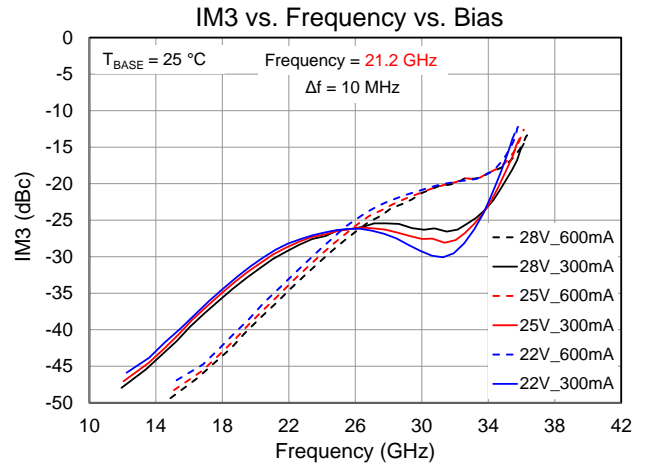
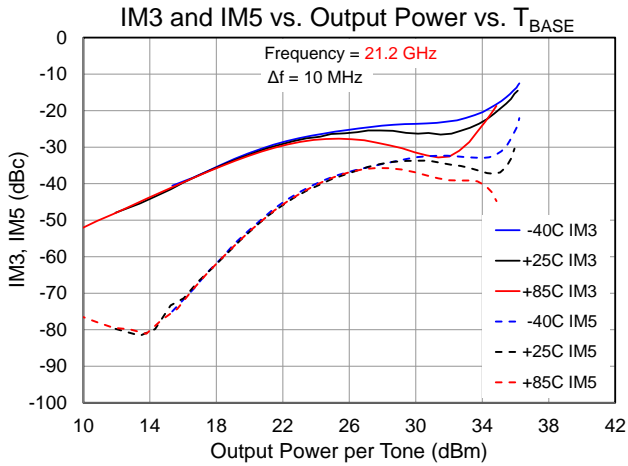
Performance Plots – Power Detector

Test conditions unless otherwise noted: CW, $V_{D1} = V_{D2} = V_{D3} = 28V$, $I_{D1} + I_{D2} + I_{D3} = 300mA$, adjusting $V_{G1} = V_{G2} = V_{G3}$, $T_{BASE} = +25\text{ }^{\circ}C$, $Z_0 = 50\ \Omega$



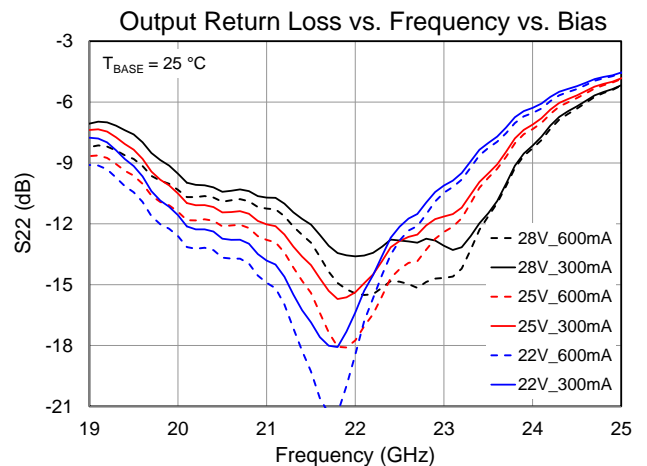
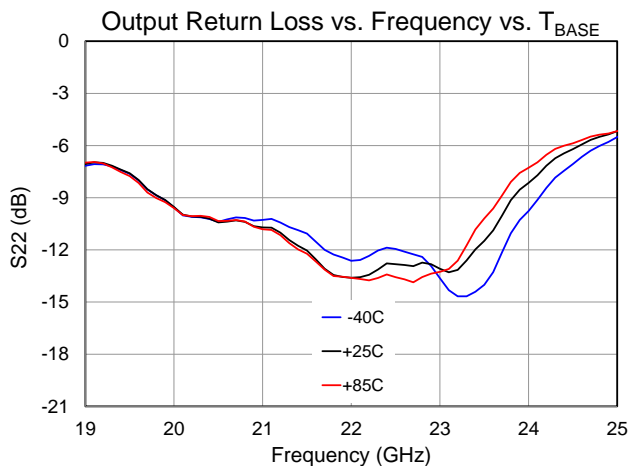
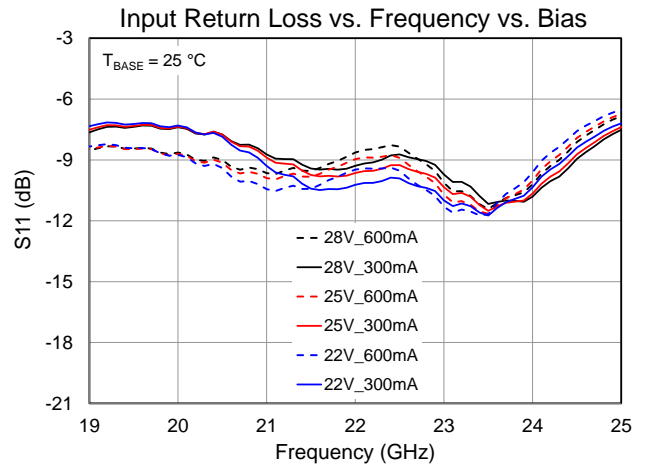
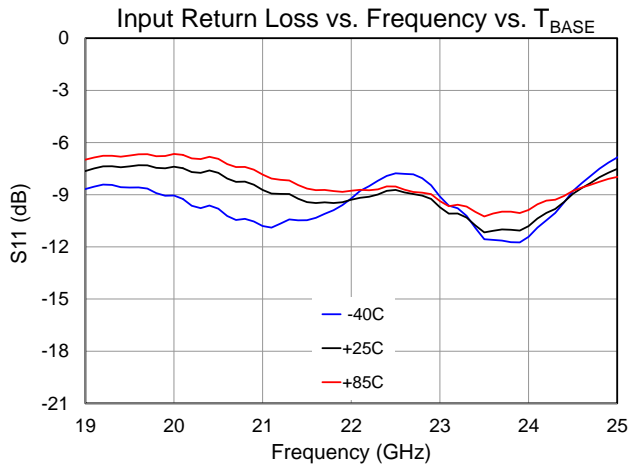
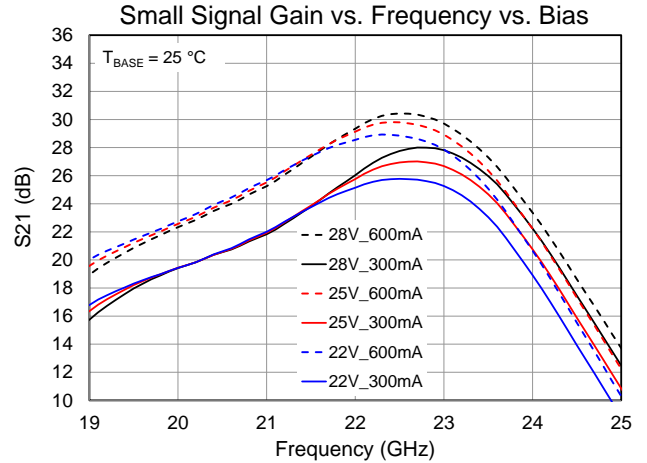
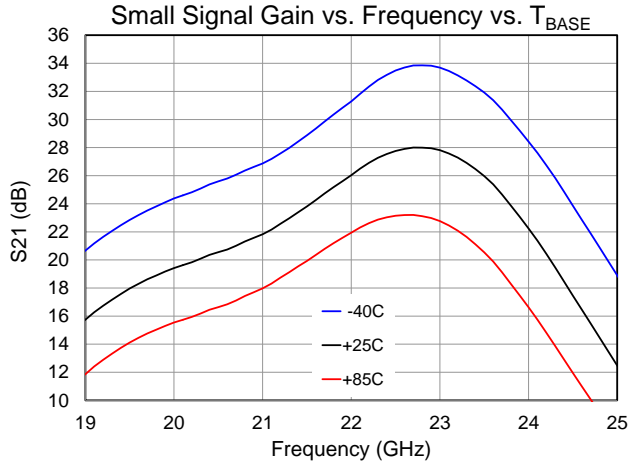
Performance Plots – Linearity

Test conditions unless otherwise noted: CW, $V_{D1} = V_{D2} = V_{D3} = 28V$, $I_{D1} + I_{D2} + I_{D3} = 300mA$, adjusting $V_{G1} = V_{G2} = V_{G3}$, $T_{BASE} = +25\text{ }^{\circ}C$, $Z_0 = 50\ \Omega$



Performance Plots – Small Signal

Test conditions unless otherwise noted: CW, $V_{D1} = V_{D2} = V_{D3} = 28V$, $I_{D1} + I_{D2} + I_{D3} = 300mA$, adjusting $V_{G1} = V_{G2} = V_{G3}$, $T_{BASE} = +25\text{ }^{\circ}C$, $Z_0 = 50\ \Omega$

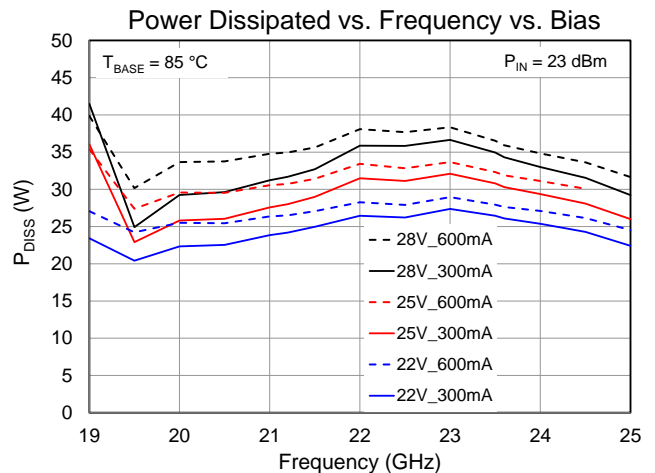
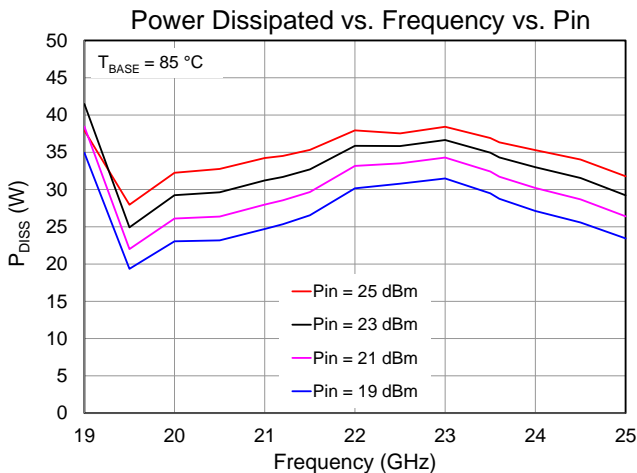
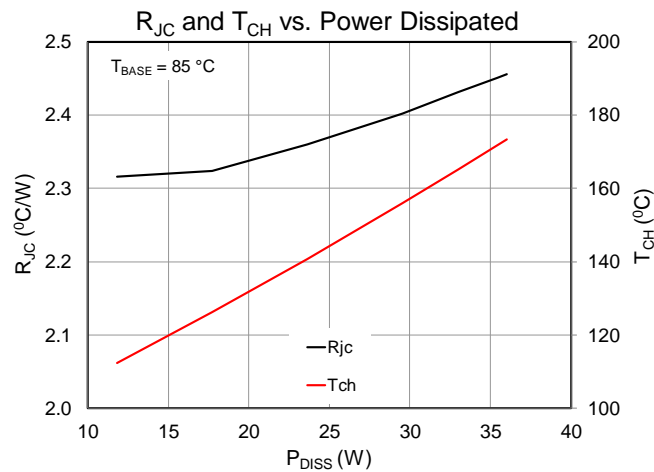


Thermal and Reliability Information

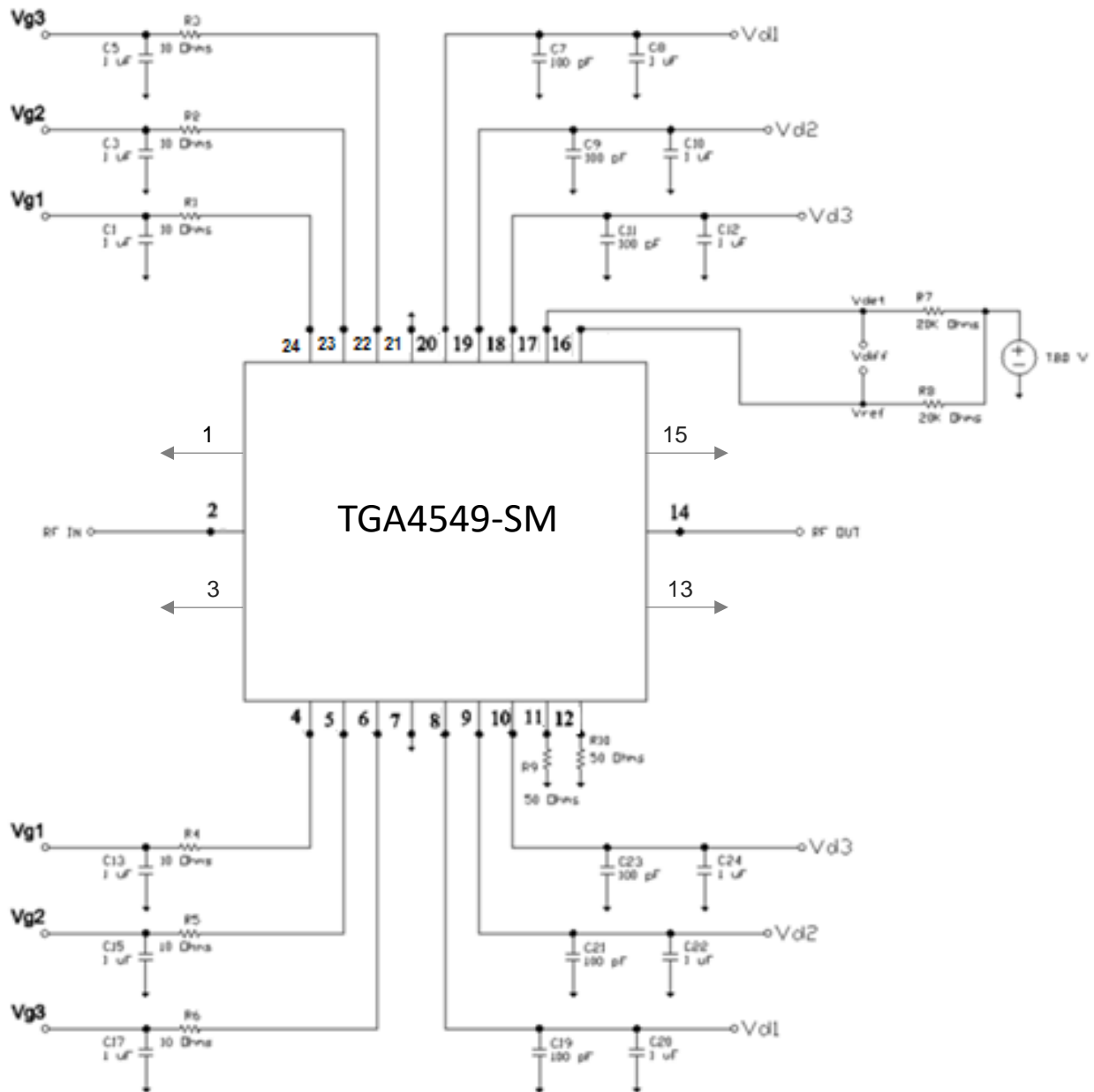
| Parameter | Test Conditions | Value | Units |
|---|---|-------|----------------------|
| Thermal Resistance (θ_{JC}) ⁽¹⁾ | $T_{BASE} = 85\text{ }^{\circ}\text{C}$, $V_D = 28\text{ V}$, $I_{DQ} = 300\text{ mA}$, Freq = 23 GHz, $P_{DISS} = 8.4\text{ W}$ | 2.38 | $^{\circ}\text{C/W}$ |
| Channel Temperature, T_{CH} (Under RF) ⁽²⁾ | | 105 | $^{\circ}\text{C}$ |
| Thermal Resistance (θ_{JC}) ⁽¹⁾ | $T_{BASE} = 85\text{ }^{\circ}\text{C}$, $V_D = 28\text{ V}$, $I_{DQ} = 300\text{ mA}$, Freq = 2 GHz, $I_{D_DRIVE} \approx 1.64\text{ A}$, $P_{IN} = 23\text{ dBm}$, $P_{OUT} = 40\text{ dBm}$, $P_{DISS} = 36\text{ W}$ | 2.44 | $^{\circ}\text{C/W}$ |
| Channel Temperature, T_{CH} (Under RF) ⁽²⁾ | | 173 | $^{\circ}\text{C}$ |

Notes:

1. Thermal resistance determined to the back of package T_{BASE}
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note "GaN Device TCHMAX Theta-JC and Reliability Estimates," located here <https://www.qorvo.com/products/d/da006480>



Recommended Application Circuit



- Notes:
1. V_{G1} , V_{G2} , and V_{G3} can be biased from either top side or bottom side; the non-biased side can be left open but bias network is required
 2. V_{D1} , V_{D2} , and V_{D3} must be biased from both sides.
 3. Tied all V_D 's together; tied all V_G 's together

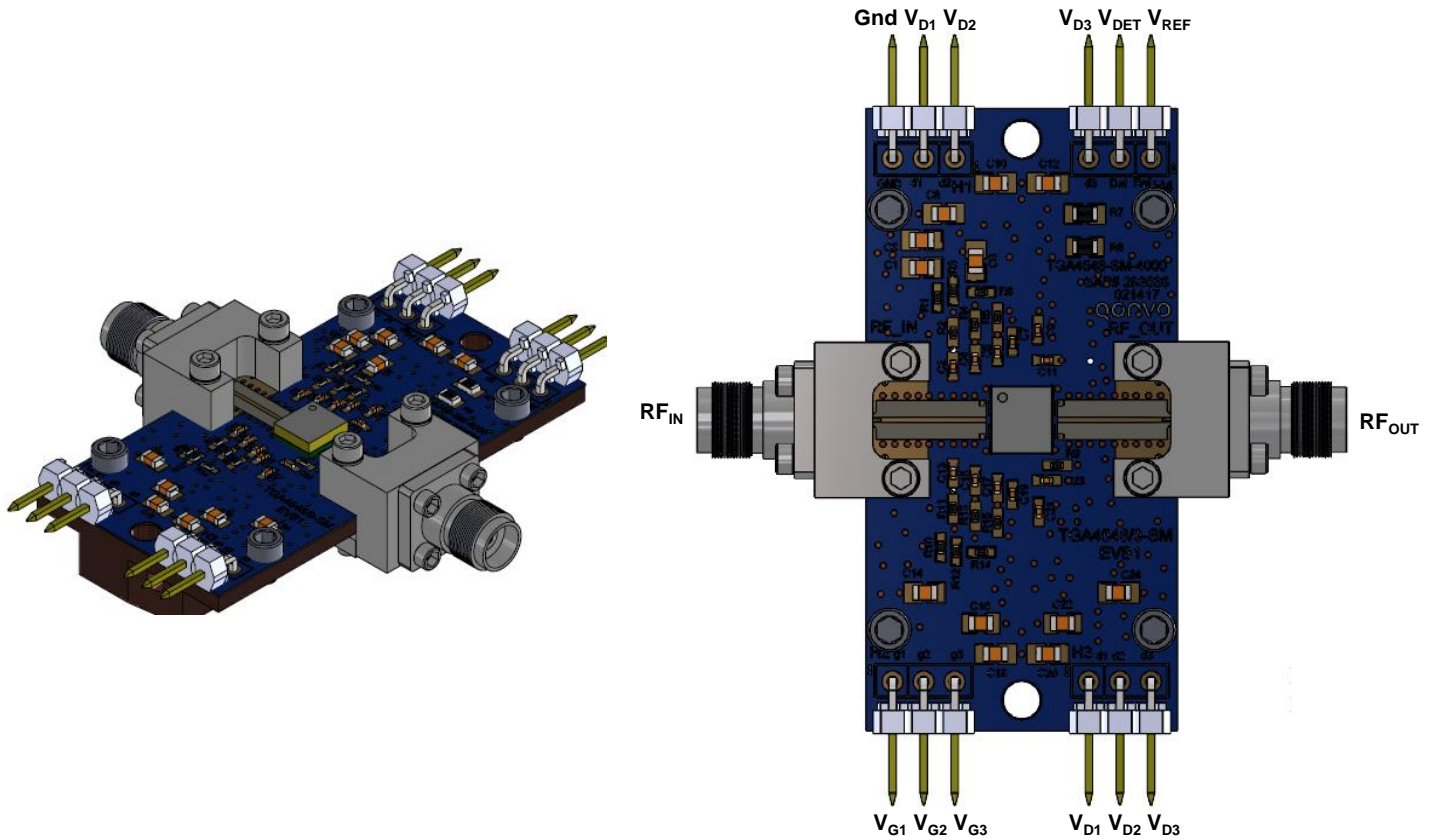
Bias Up Procedure

1. Set I_D limit to 3000 mA, I_G limit to 10 mA
2. Apply $-5V$ to V_G
3. Apply $+28V$ to V_D ; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until $I_{DQ} = 300$ mA ($V_G \sim -2.5 \pm 0.4$ V Typ.).
5. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to $-5V$; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

Application Evaluation Board (EVB)

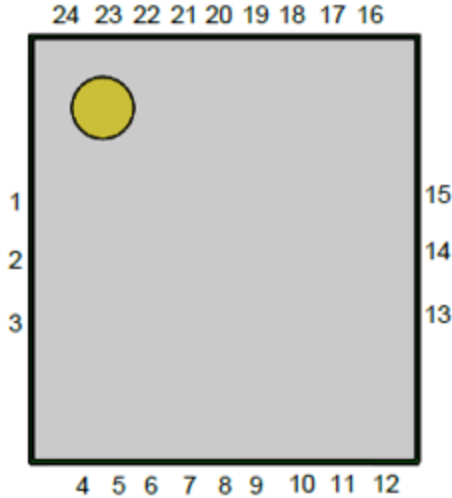


- Notes:
1. Board Material is RO4003 0.008" thickness with 1/2 oz. copper cladding
 2. Vias under the ground paddle are copper filled.

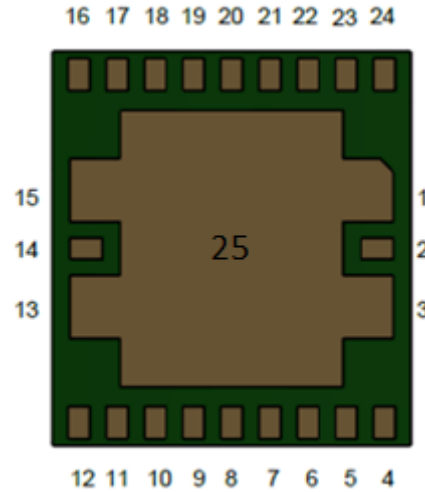
Bill of Material – Evaluation Board (EVB)

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------------------|-------|---------------------------------|---------|-------------|
| n/a | n/a | Printed Circuit Board | Qorvo | |
| U1 | n/a | 17.7 – 19.7 GHz Power Amplifier | Qorvo | TGA4549-SM |
| C7, C9, C11, C19, C21, C23 | 100pF | Cap, 0402, 50 V, 5%, COG | various | |
| C1, C3, C5, C13, C15, C17 | 1uF | Cap, 0805, 50 V, 5%, X5R | various | |
| R1-R6 | 10Ω | Resistor, 0402, 5%, 1/16W, SMD | various | |
| R7, R8 | 20kΩ | Resistor, 0805, 5%, SMD | various | |
| R9 | 50Ω | Resistor, 0402, 5%, 1/16W, SMD | various | |

Pad Configuration and Description



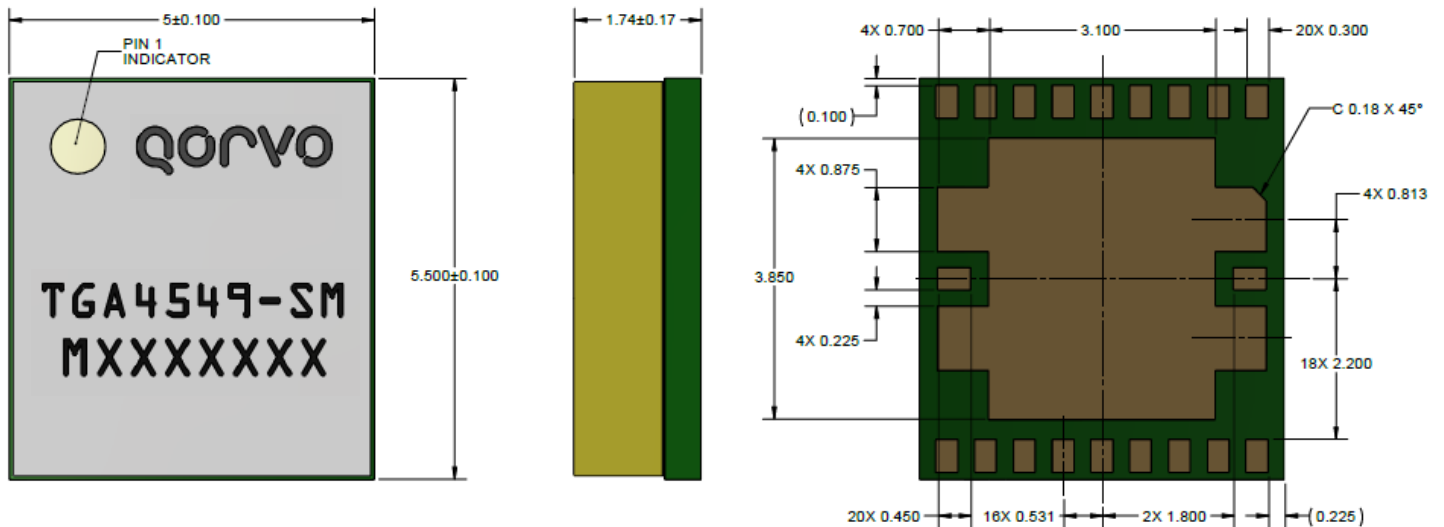
Top View



Bottom View

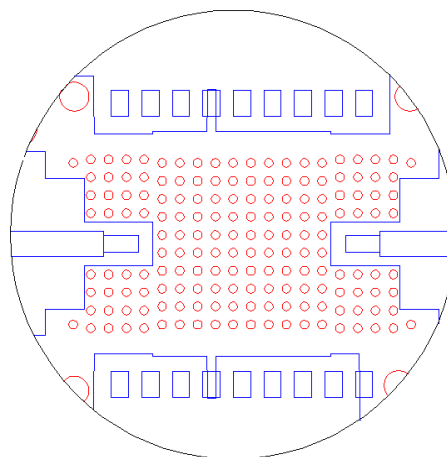
| Pad No. | Label | Description |
|---------------------|-------------------|---|
| 1, 3, 7, 13, 15, 21 | GND | Ground. Must be grounded on PCB (same as Pad 25) |
| 2 | RF _{IN} | RF input, matched to 50Ω, AC coupled. |
| 4, 24 | V _{G1} | Gate voltage, stage 1. Bias network is required; see Recommended Application Circuit on page 12 |
| 5, 23 | V _{G2} | Gate voltage, stage 2. Bias network is required; see Recommended Application Circuit on page 12 |
| 6, 22 | V _{G3} | Gate voltage, stage 3. Bias network is required; see Recommended Application Circuit on page 12 |
| 8, 20 | V _{D1} | Drain voltage, stage 1. Bias network is required; see Recommended Application Circuit on page 12 |
| 9, 19 | V _{D2} | Drain voltage, stage 2. Bias network is required; see Recommended Application Circuit on page 12 |
| 10, 18 | V _{D3} | Drain voltage, stage 3. Bias network is required; see Recommended Application Circuit on page 12 |
| 11, 17 | V _{DET} | Detector diode output voltage. Varies with RF output power. |
| 12, 16 | V _{REF} | Reference diode output voltage |
| 14 | RF _{OUT} | RF output, matched to 50Ω, AC coupled. |
| 25 | GND | Backside paddle. Multiple conductive filled vias should be employed to minimize inductance and thermal resistance; see Mounting Configuration on page 15 for suggested footprint. |

Package Marking and Dimensions



Units: millimeters
 Tolerances: unless specified
 x.xx = ± 0.25 x.xxx = ± 0.100 Angles = 0.5°
 Materials:
 Base: EHS Laminate
 Lid: Laminate
 All metalized features are gold plated; Part is epoxy sealed
 Marking:
 TGA4549-SM: Part number
 MXXXXXXX: where XXXXXXXX represents assembly lot number

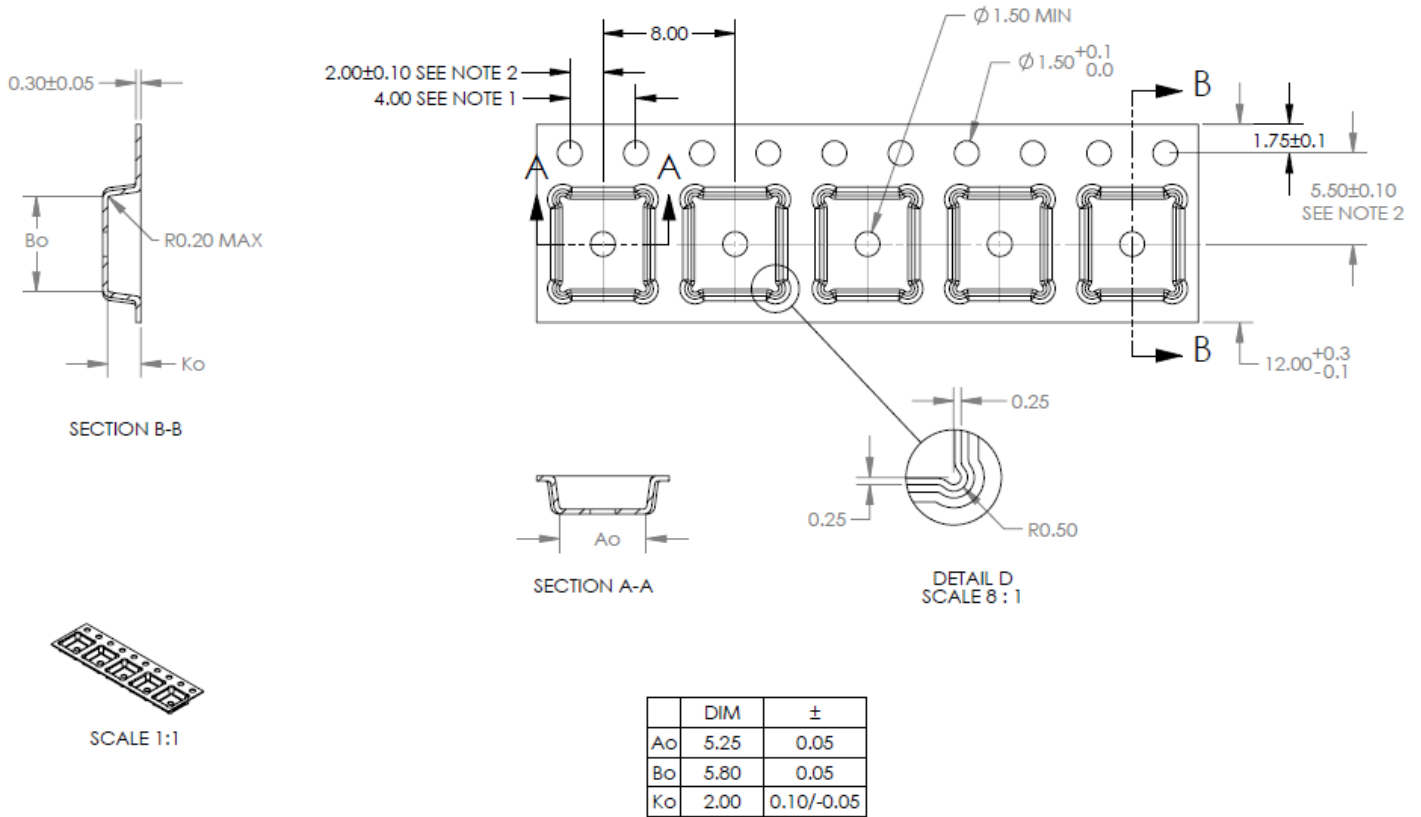
PCB Mounting Pattern



- Notes:
1. All dimensions are in millimeters. Angles are in degrees.
 2. Ground vias are critical for the proper performance of this device. Vias should have a final plated thru diameter of .1524 mm (.006”).
 3. For best thermal performance, vias under the ground paddle should be copper filled.
 4. The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Tape and reel Information

Standard T/R size = 200 pieces on a 7" reel
 Dimensions: millimeters (mm)
 Tolerances unless otherwise noted: .X = ± .2; .XX = ± .10



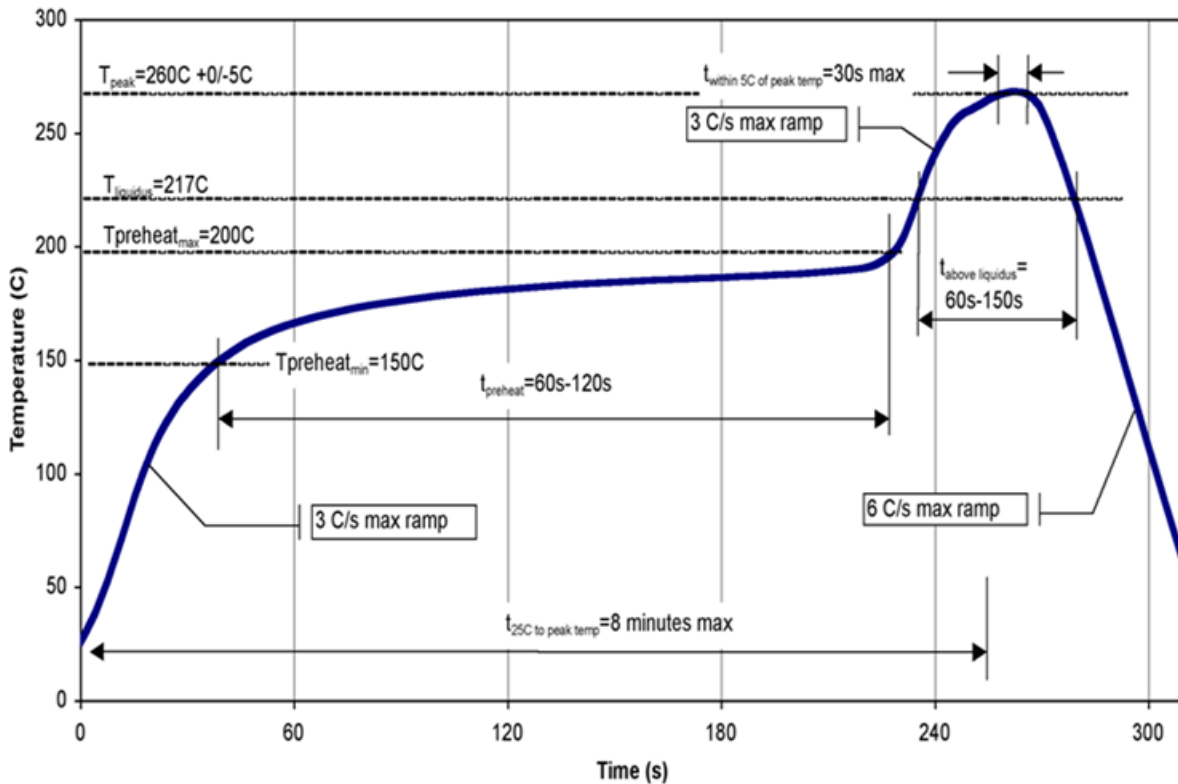
Assembly Notes

Compatible with lead-free soldering processes with 260°C peak reflow temperature.

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended.

Contact plating: Ni-Au

Solder rework not recommended



Recommended Soldering Temperature Profile

Handling Precautions

| Parameter | Rating | Standard |
|----------------------------------|--------|-----------------------|
| ESD – Human Body Model (HBM) | 1A | ANSI/ESD/JEDEC JS-001 |
| MSL – Moisture Sensitivity Level | 3 | IPC/JEDEC J-STD-020 |



Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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