TGA2512-SM

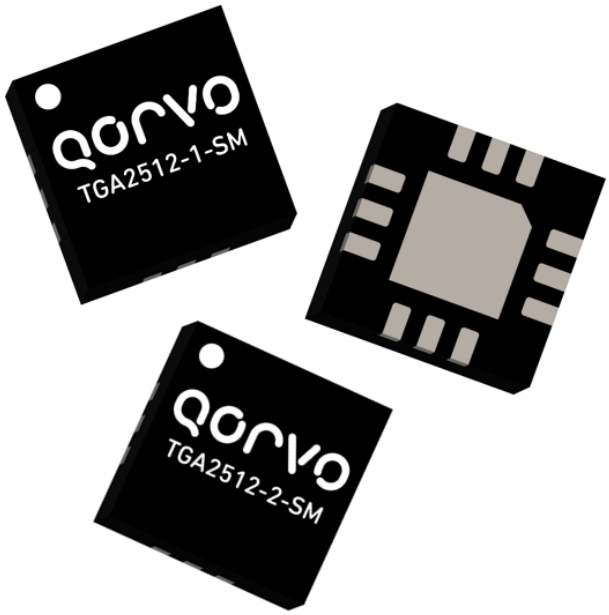
4 -14 GHz GaAs Balanced LNA

Product Description

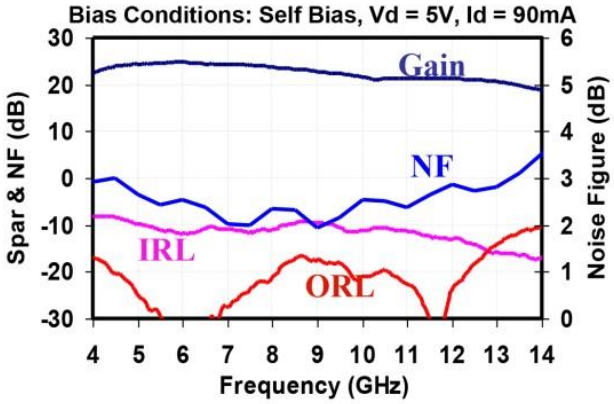
The Qorvo TGA2512-SM is a packaged X-band balanced LNA with AGC amplifier for EW, ECM, and RADAR receiver or driver amplifier applications. Based on Qorvo's GaAs 3MI pHEMT process, the TGA2512-SM provides excellent noise performance with typical midband NF of 2.3 dB, with a high gain of 25 dB from 4-14.2 GHz

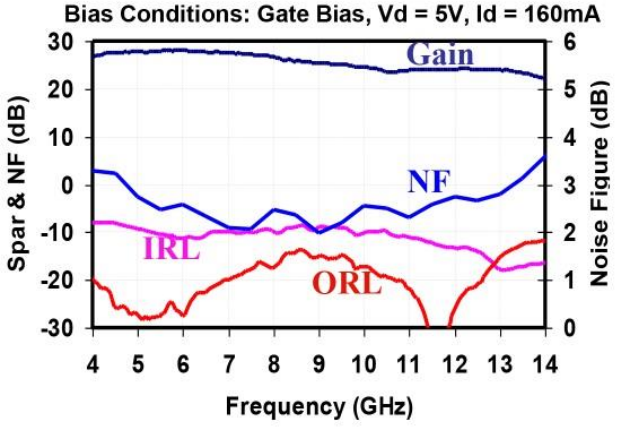
The TGA2512-SM is designed for maximum ease of use. TGA2512-SM can handle up to 21 dBm input power reliably, while the build-in gain control provides 15 dB of typical gain control range. The part can be used in self-biased mode, with a single +5 V supply connection, or in gate biased mode, allowing the user to control the current for a particular application.

In self-biased mode the TGA2512-SM achieves 6 dBm typical P1 dB, while in gate-biased mode the typical P1 dB is over 13 dBm.



Measured Data





Key Features

- Frequency Range: 4–14.2 GHz
- 2.3 dB Nominal Noise Figure
- 25 dB Nominal Gain
- 15 dB AGC Range
- 13 dBm Nominal P1dB
- 24 dBm Nominal OIP3
- Bias: 5 V, 160 mA Gate Bias, 5 V, 90 mA Self Bias
- Package Dimensions: 4.0 x 4.0 x 0.9 mm

Applications

- X-Band Radar
- EW, ECM
- Point-to-Point Radio

Ordering Information

Part No.	Package Style
TGA2512-1-SM	QFN 4 x 4 Surface Mount – **Self Bias**
TGA2512-2-SM	QFN 4 x 4 Surface Mount – **Gate Bias**
1059405	TGA2512-1-SM Evaluation Board
TGA2512-2-SMEVB1	TGA2512-2-SM Evaluation Board

MAXIMUM RATINGS 1/

Symbol	Parameter	Value	Notes
Vd	Drain Voltage	Gate Bias: [4 + (0.009)(Id)] V	2/ 3/
		Self Bias: [3.5 + (0.022)(Id)] V	
Vg	Gate Voltage Range	-1 TO +0.5 V	
Id	Drain Current (gate biased)	240 mA	2/
|Ig|	Gate Current	7.04 mA	
P_{IN}	Input Continuous Wave Power	21 dBm	
P_D	Power Dissipation	1.56 W	2/ 4/
T_{CH}	Operating Channel Temperature	200 °C	5/
	Mounting Temperature (30 Seconds)	260 °C	
T_{STG}	Storage Temperature	-65 to 150 °C	

1/. These ratings represent the maximum operable values for this device.
2/. Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.
3/. Unit for Id is mA.
4/. When operated at this bias condition with a base plate temperature of 85 °C, the median life is 9.3E4 hours.
5/. Junction operating temperature will directly affect the device median time to failure (Tm). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

Electrical Characteristics

T_A = 25 °C, Nominal

Parameter	Self Bias TGA2512-1-SM	Gate Bias TGA2512-2-SM	Units
Frequency Range	4–14.2	4–14.2	GHz
Drain Voltage, V_D	5.0	5.0	V
Drain Current, I_D	160	160	mA
Gate Voltage, V_G	-	-0.1	V
Small Signal Gain, S21	22	25	dB
Input Return Loss, S11	-10	-10	dB
Output Return Loss, S22	-20	-20	dB
Noise Figure, NF	2.3	2.3	dB
Output Power @ 1 dB Gain Compression, P1 dB	6	13	dBm
OIP3	16	24	dBm
Temperature Gain Coefficient	-0.02	-0.02	dB/°C

Note: Table II Lists the RF Characteristics of typical devices as determined by fixture measurements.

TGA2512-2-SM Electrical Characteristics

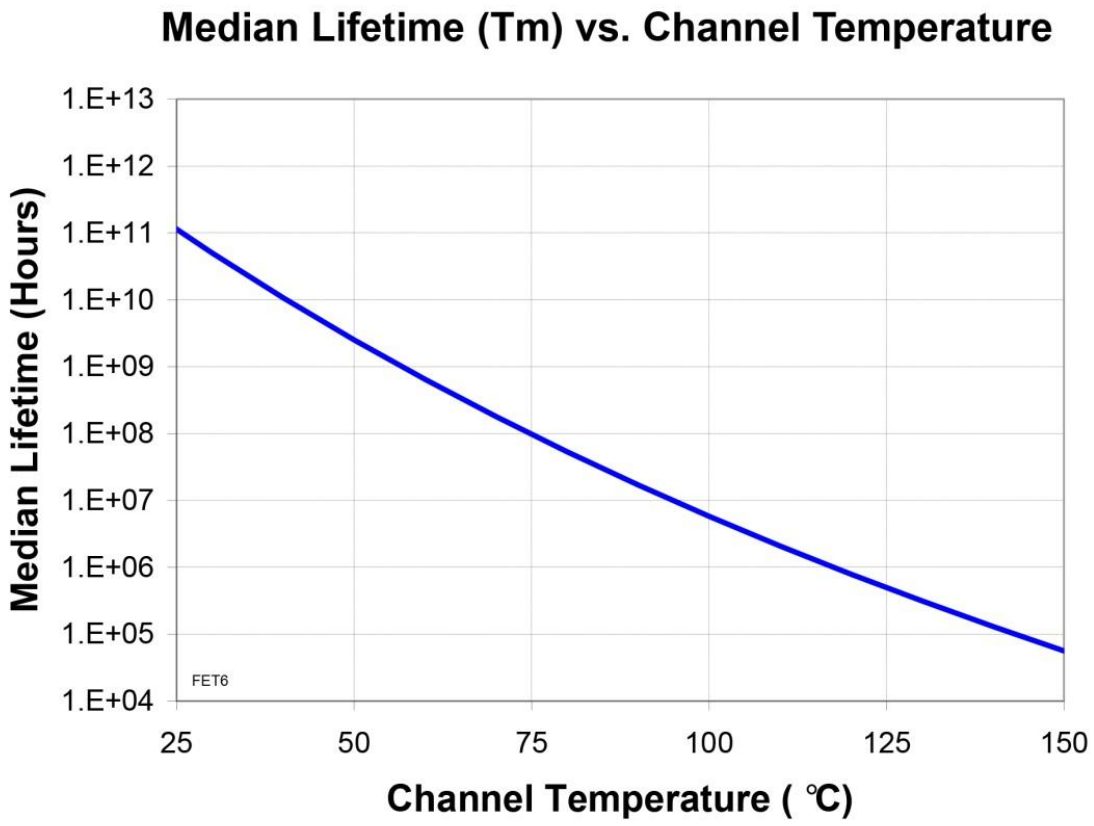
V_D = 5 V, I_D = 160 mA, V_{CTRL} = 0 V, T_A = 25 °C, Nominal

Parameter	Min	Typ	Max	Units
Frequency Range	11		14.2	GHz
Drain Current, I_D		160	200	mA
Gate Voltage, V_G	-0.4	-0.1	0.2	V
Small Signal Gain, S21	19	24		dB
Input Return Loss, S11	-7	-12		dB
Output Return Loss, S22	-7	-12		dB
Noise Figure, NF		3	4.5	dB
Output Power @ 1 dB Gain Compression, P1 dB	10	13		dBm
OIP3	16	22		dBm

Thermal Information

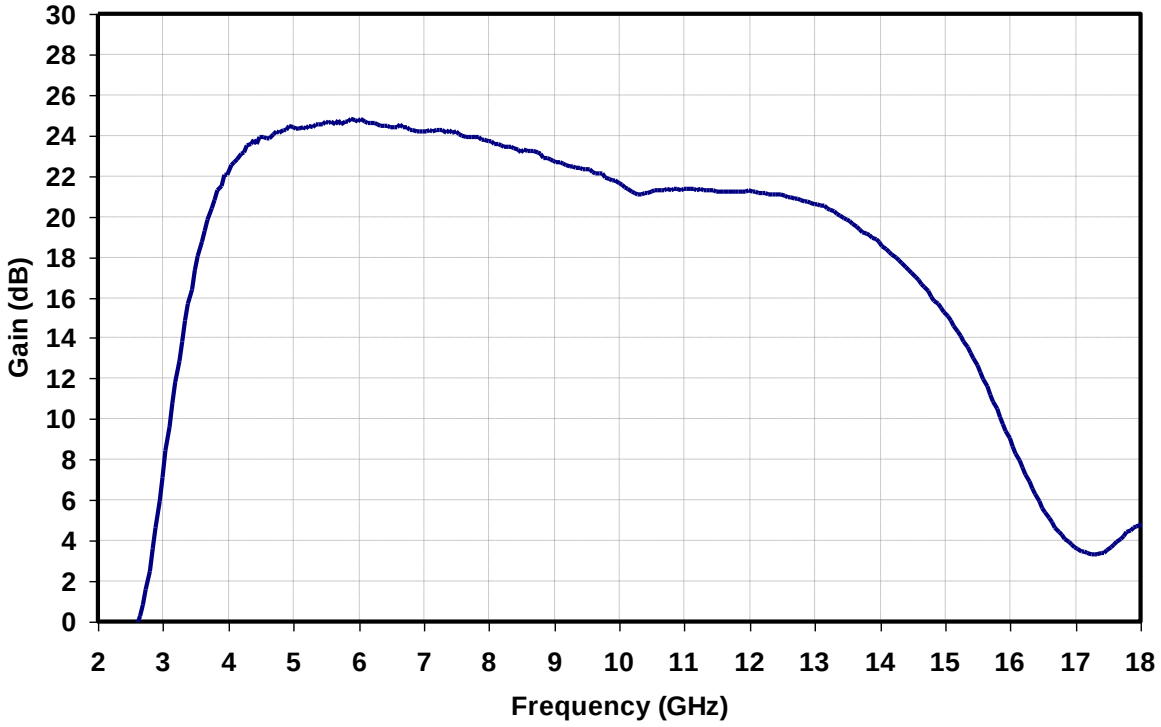
Parameter	Test Conditions	T_{CH} (°C)	Θ_{JC} (°C/W)	T_M (HRS)
θ_{JC} Thermal Resistance (channel to Case)	V_D = 5 V I_D = 160 mA Gate Bias Pdiss = 0.80 W	115	37.6	1.3E+6
θ_{JC} Thermal Resistance (channel to Case)	V_D = 5 V I_D = 90 mA Self Bias P_{DISS} = 0.45 W	97.7	28.2	7.2E+6

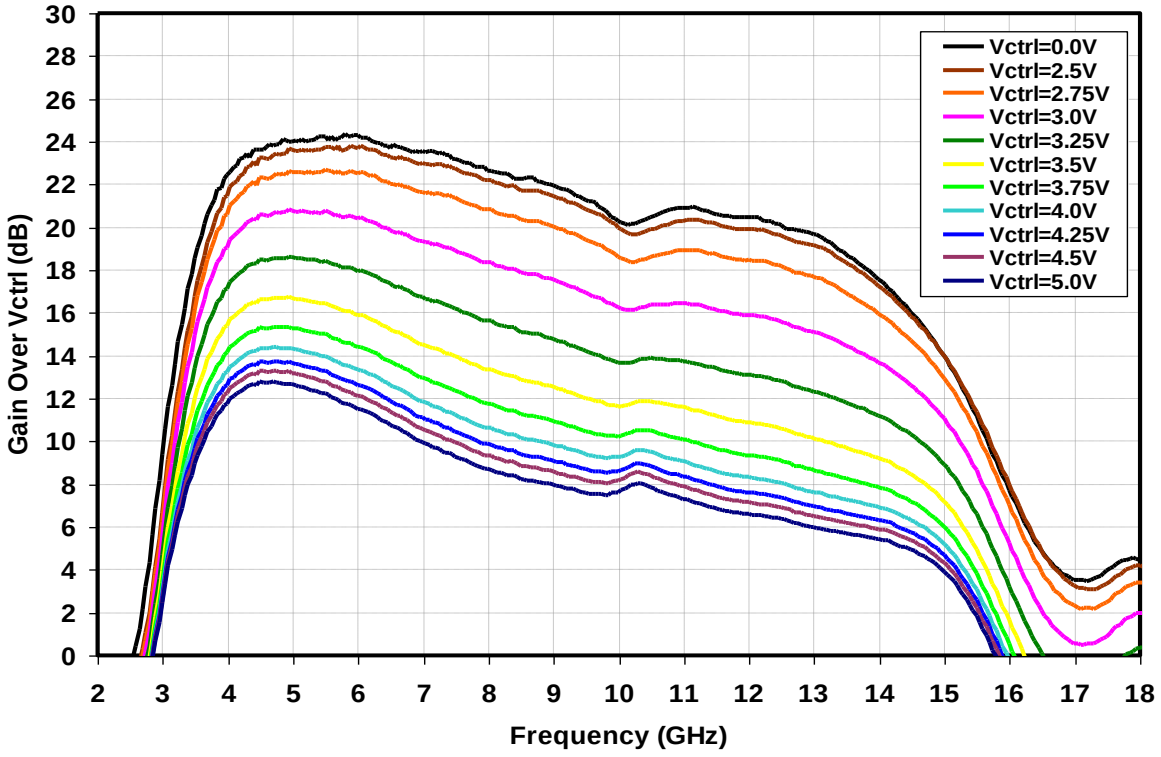
Note: Worst case condition with no RF applied. 100% of DC power is dissipated. Case temperature at 85 °C



Measured Data

Bias Conditions: Self Bias, V_D = 5 V, I_D = 90 mA





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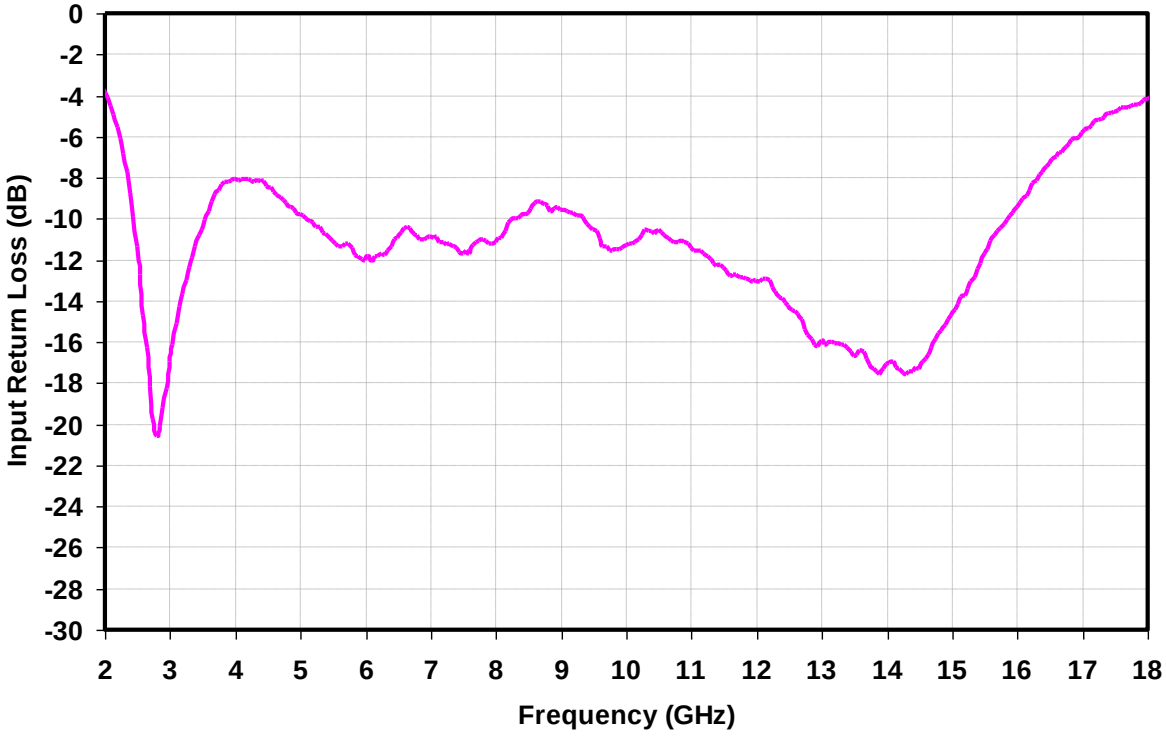

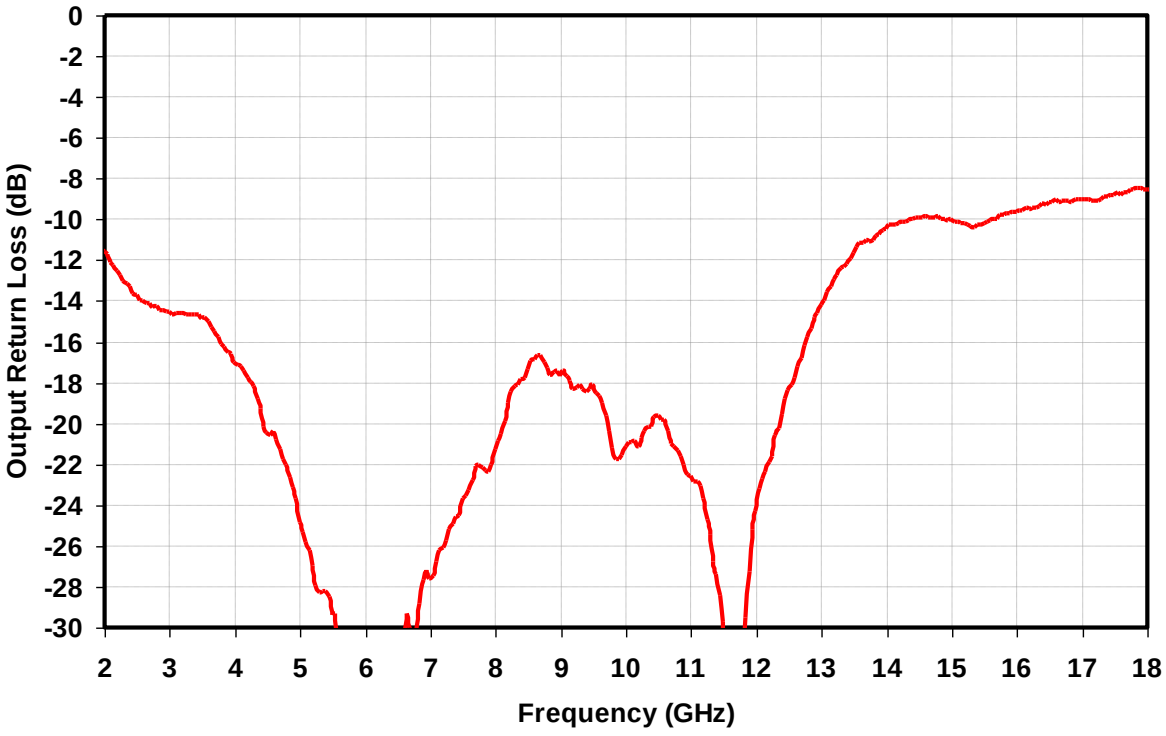

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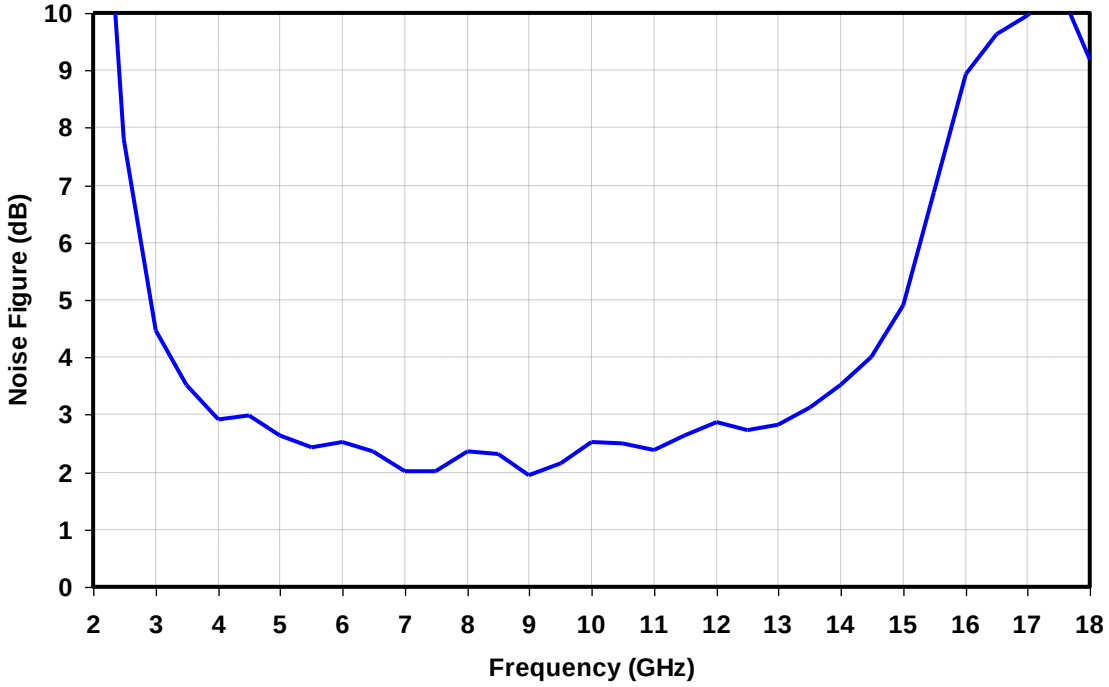

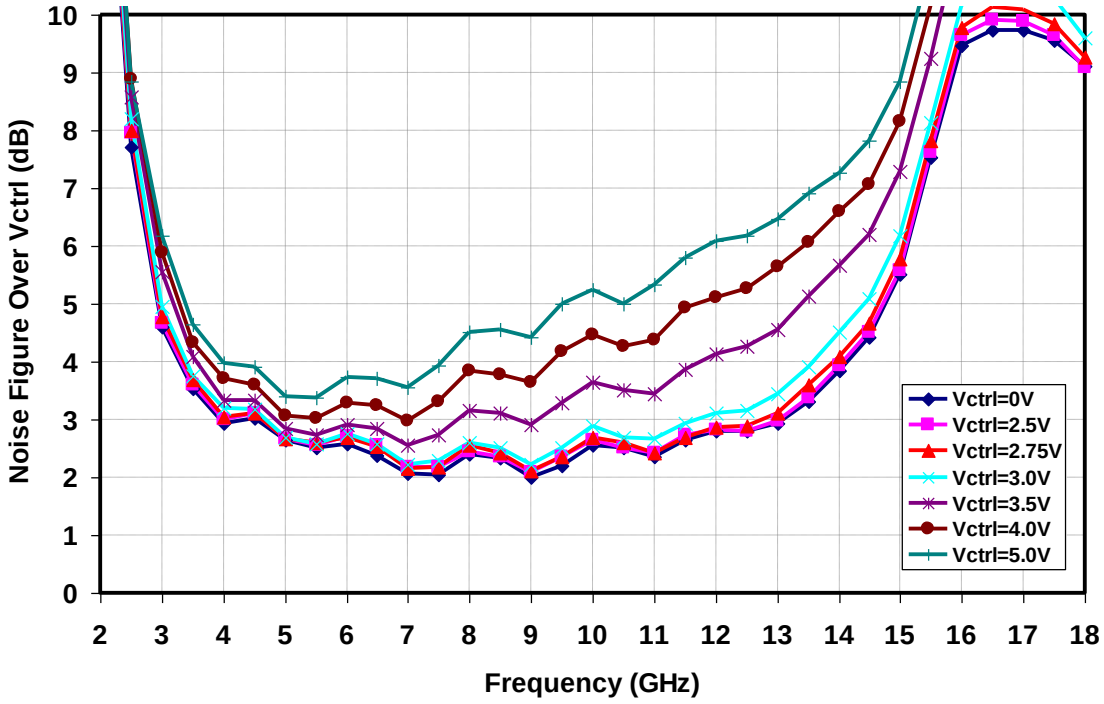

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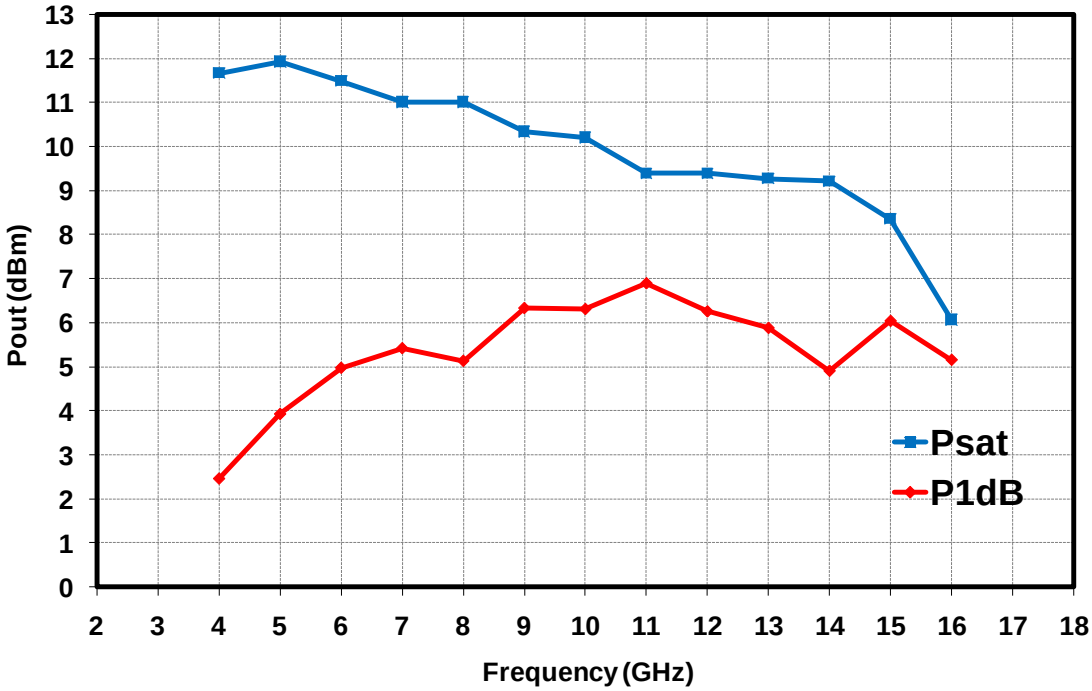

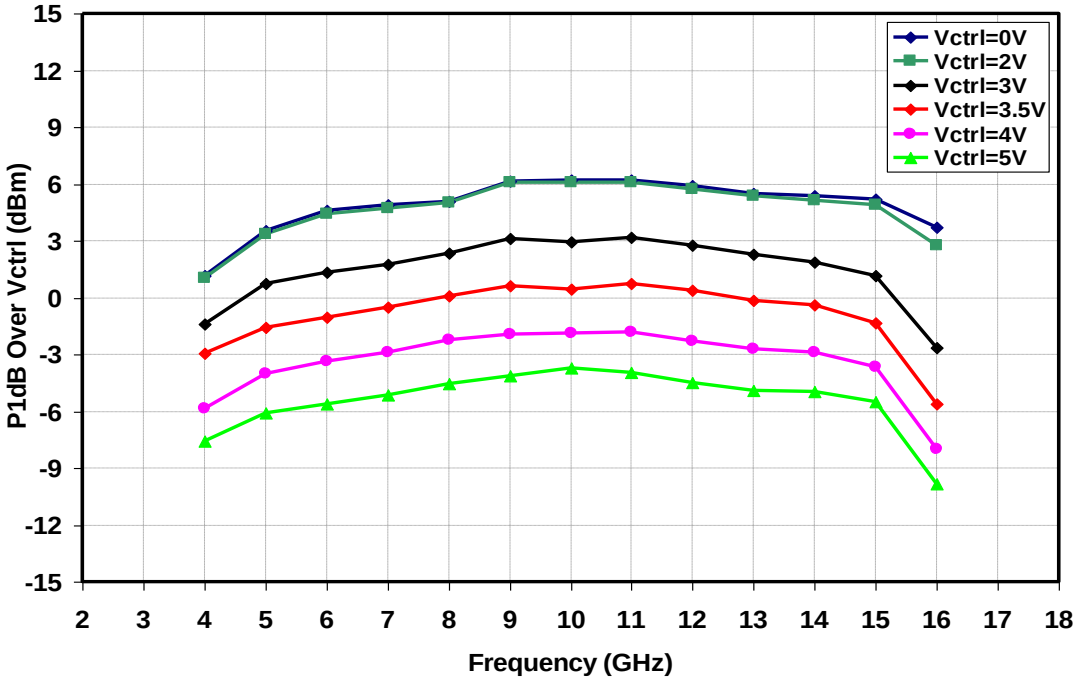

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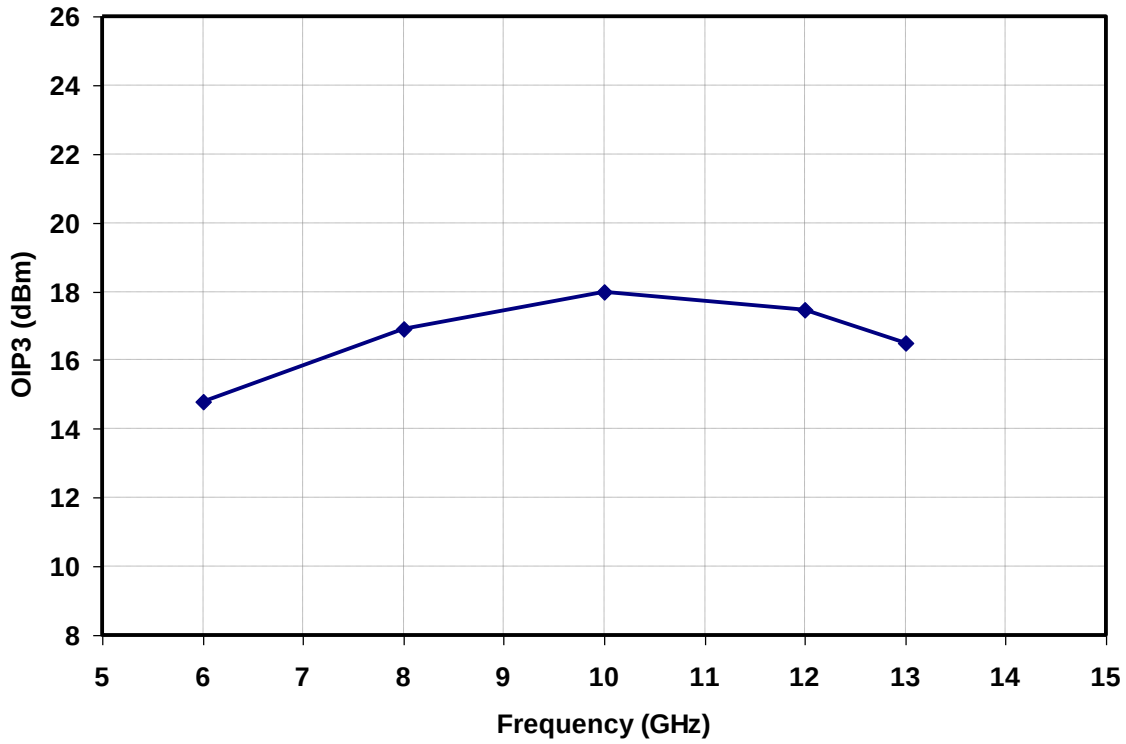
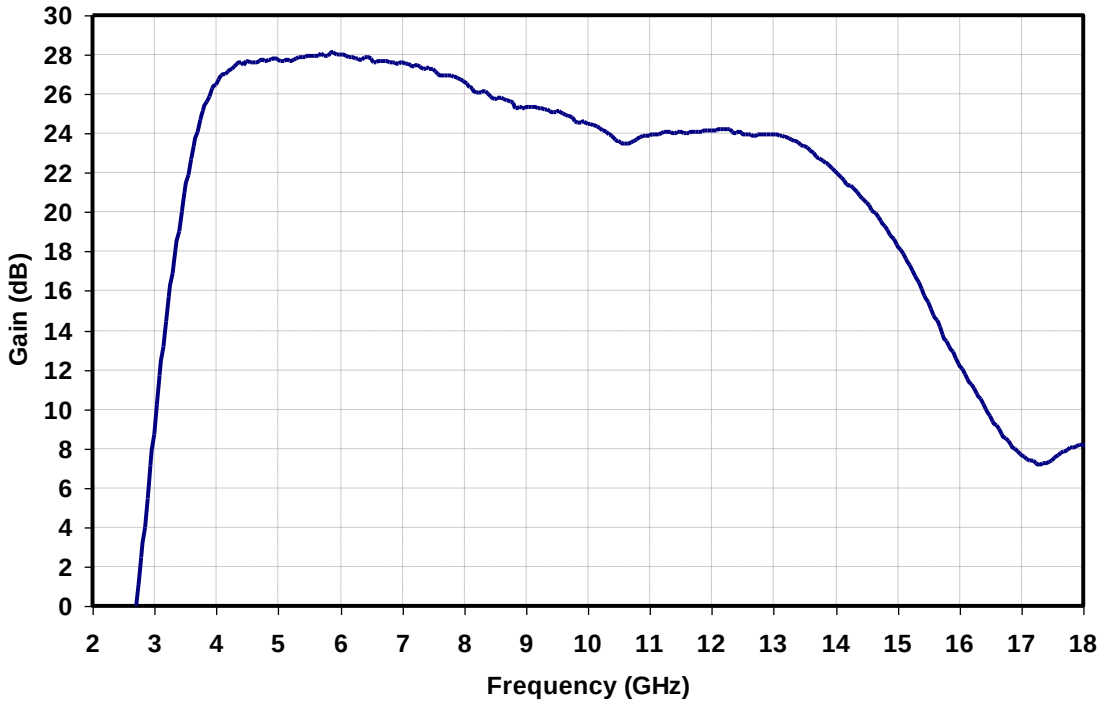
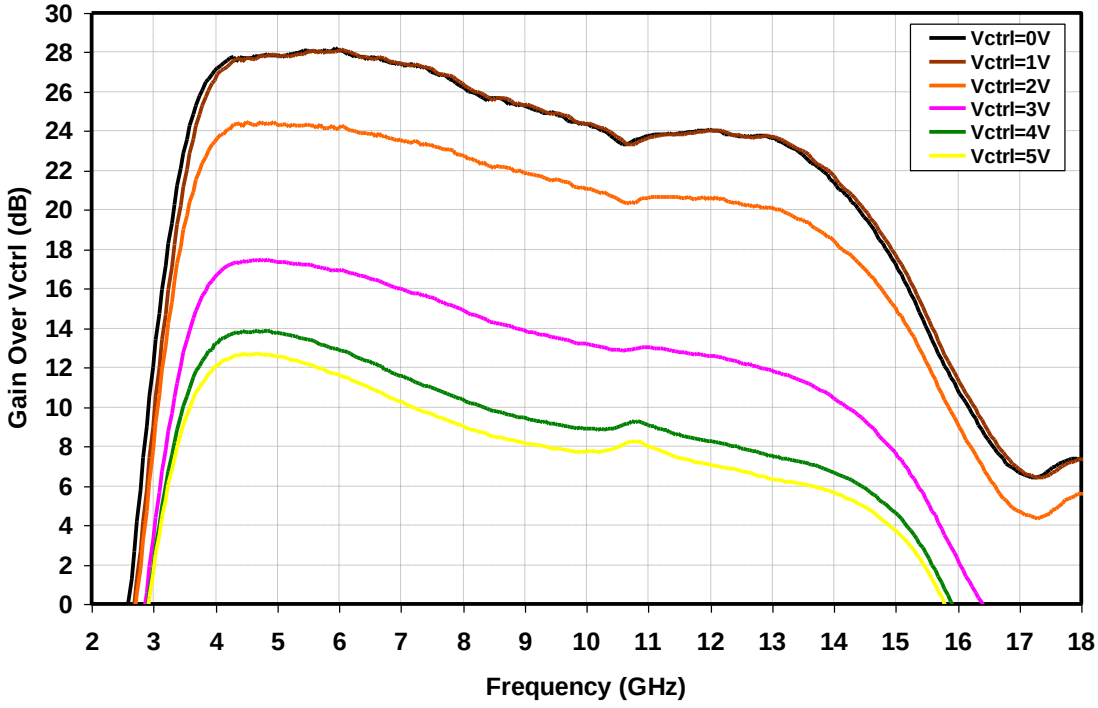


Measured Data

Bias Conditions: Gate Bias, V_D = 5 V, I_D = 160 mA





Measured Data

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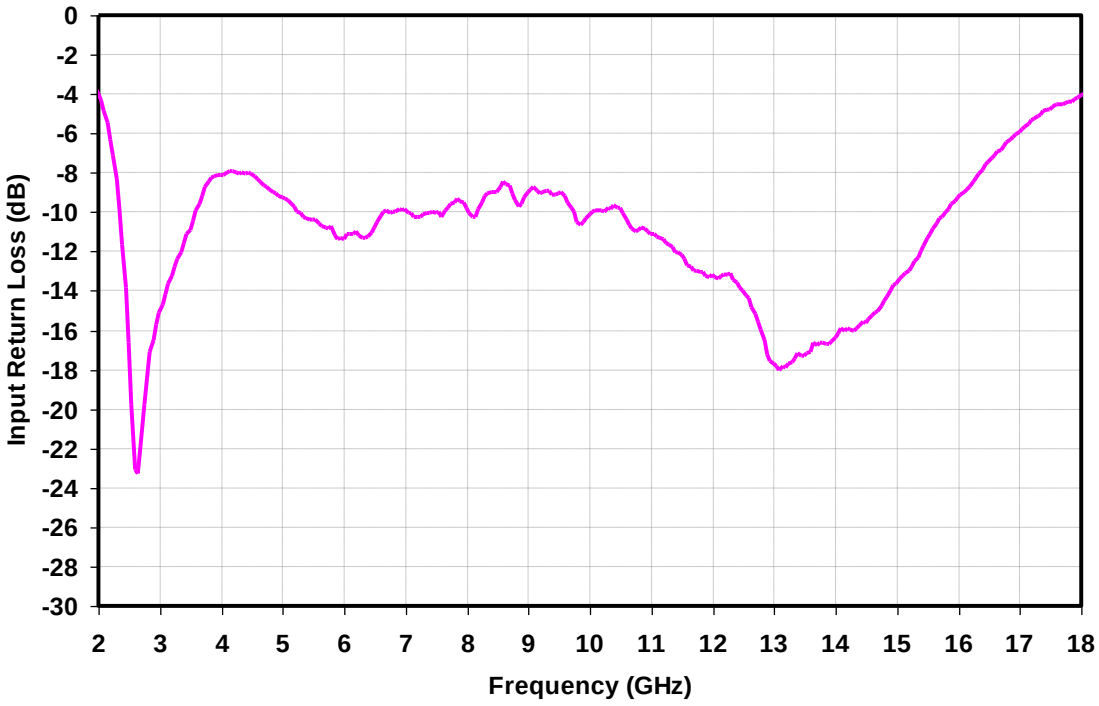

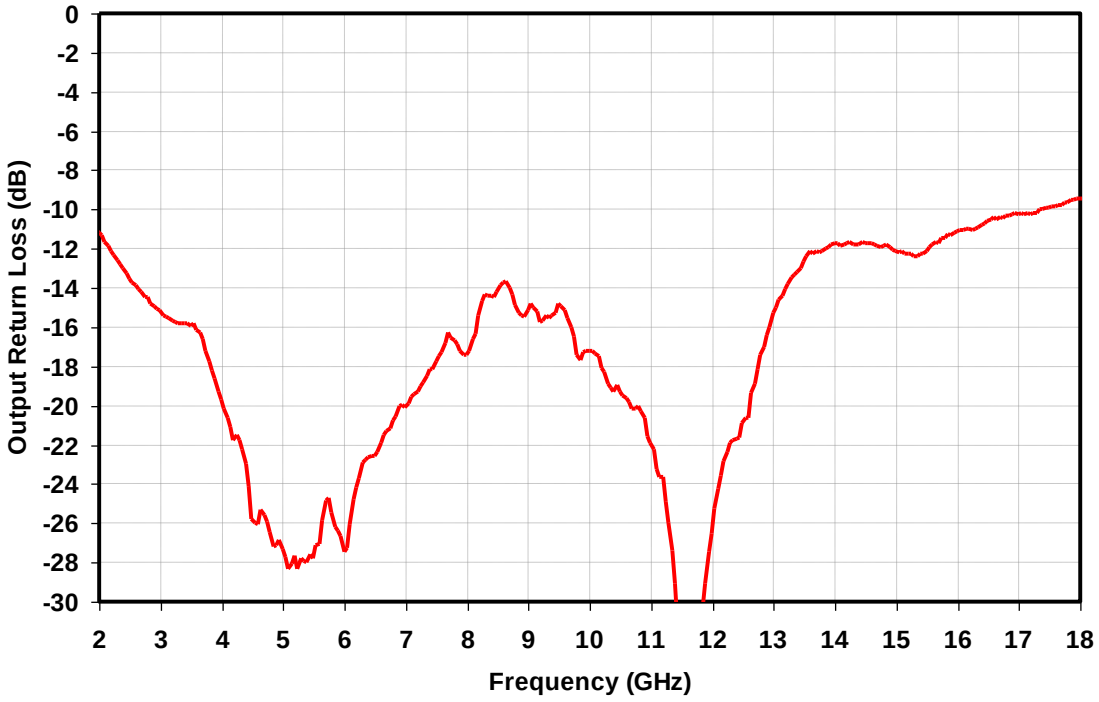

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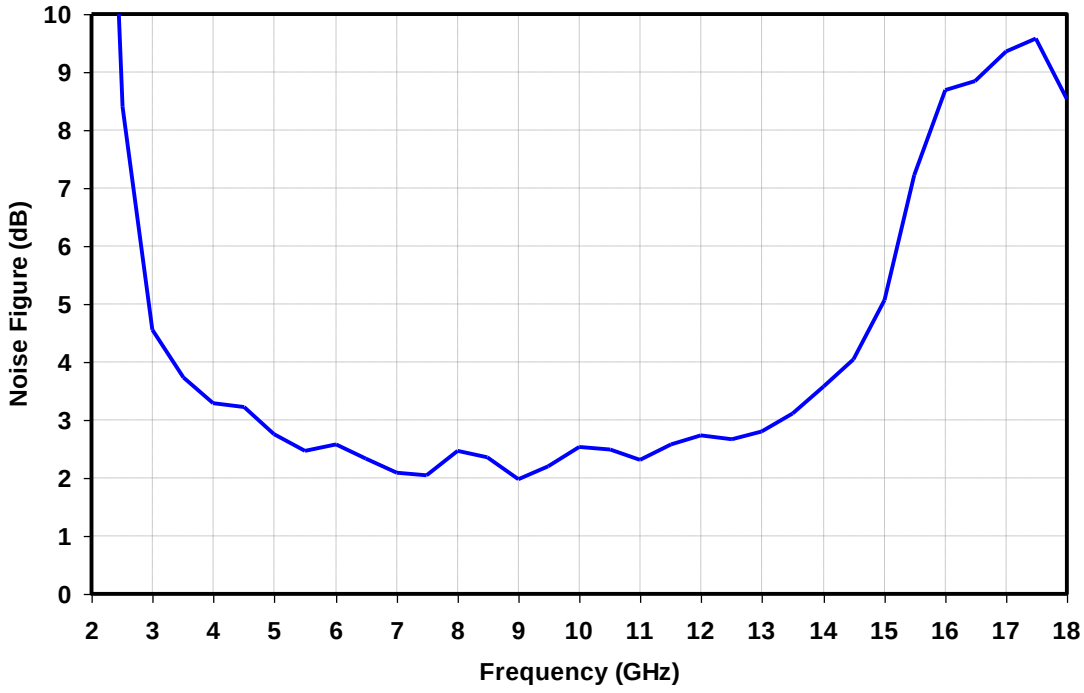

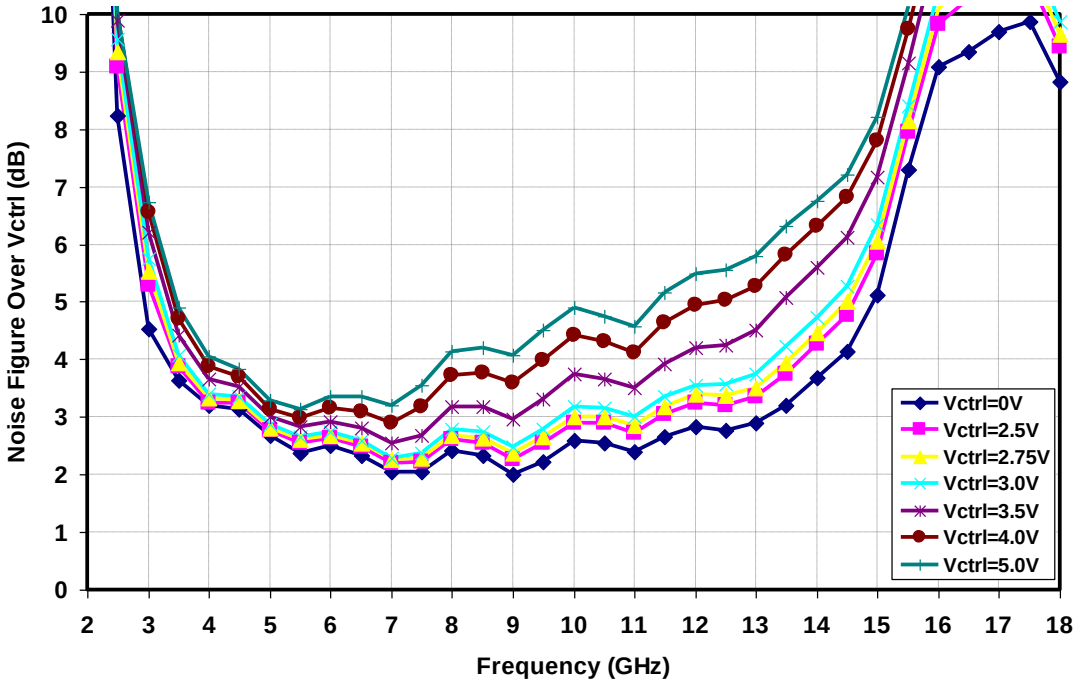

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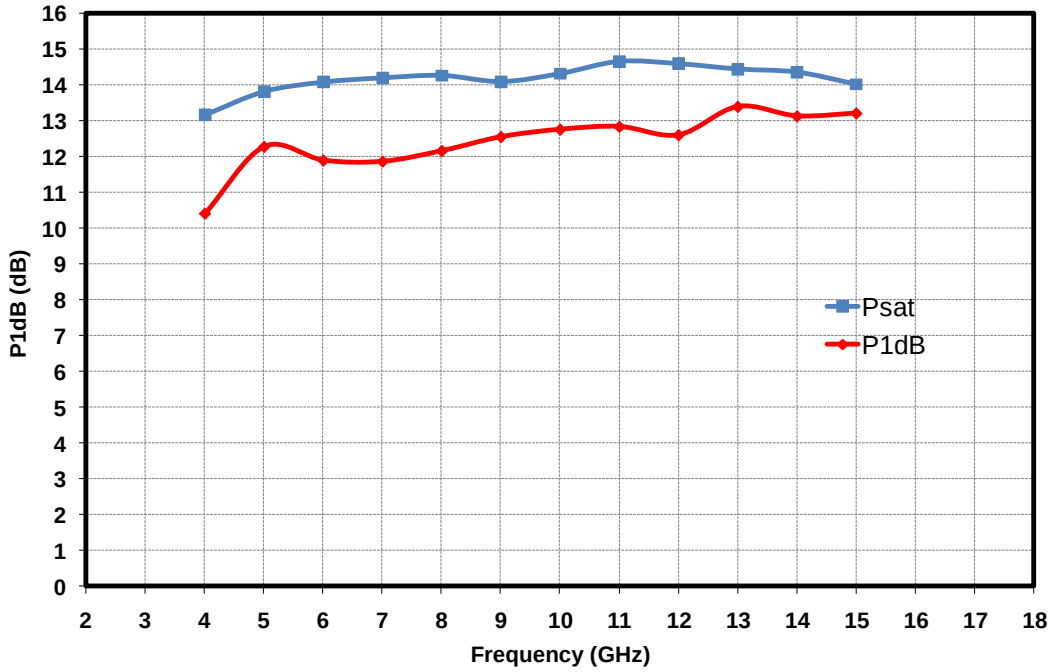

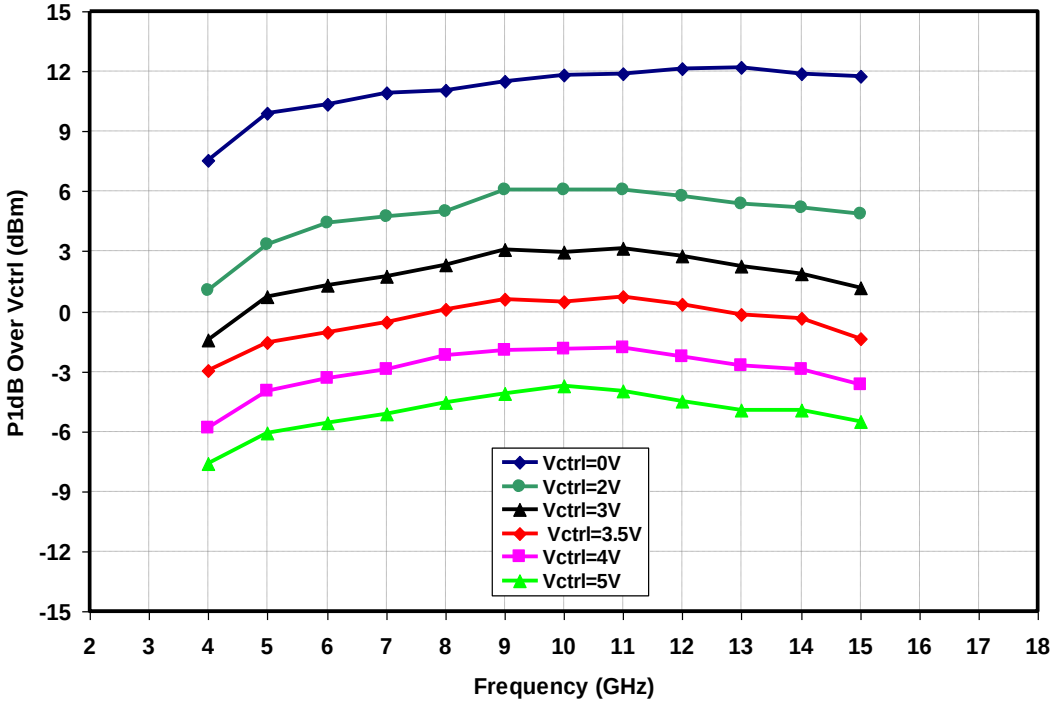

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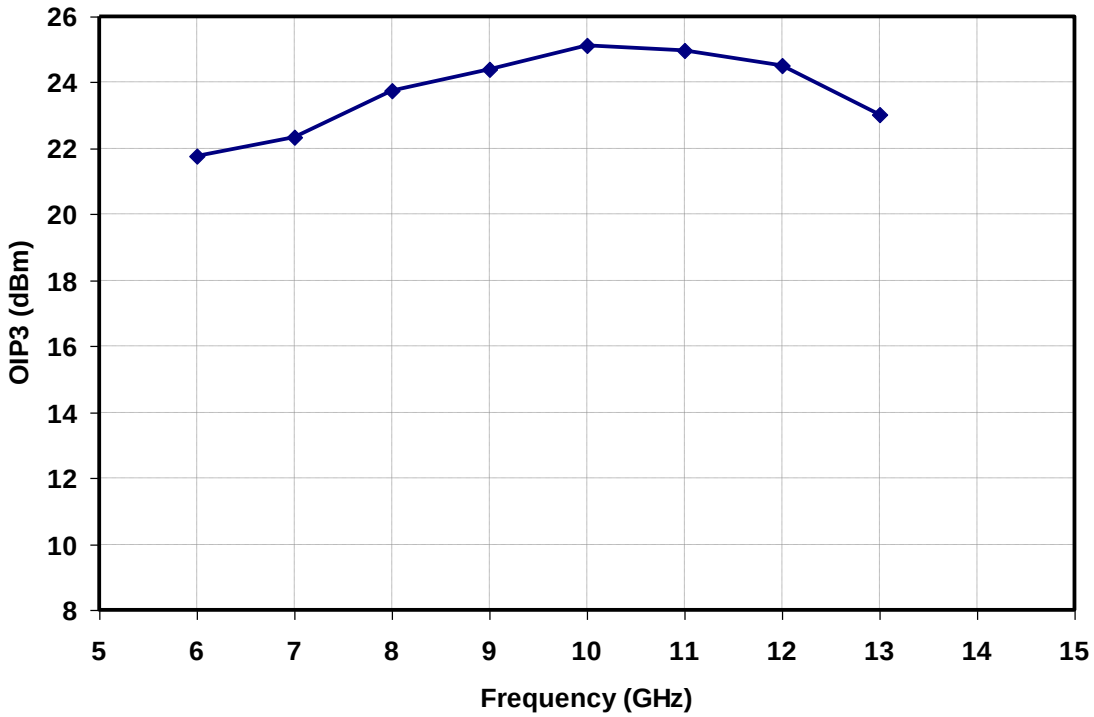
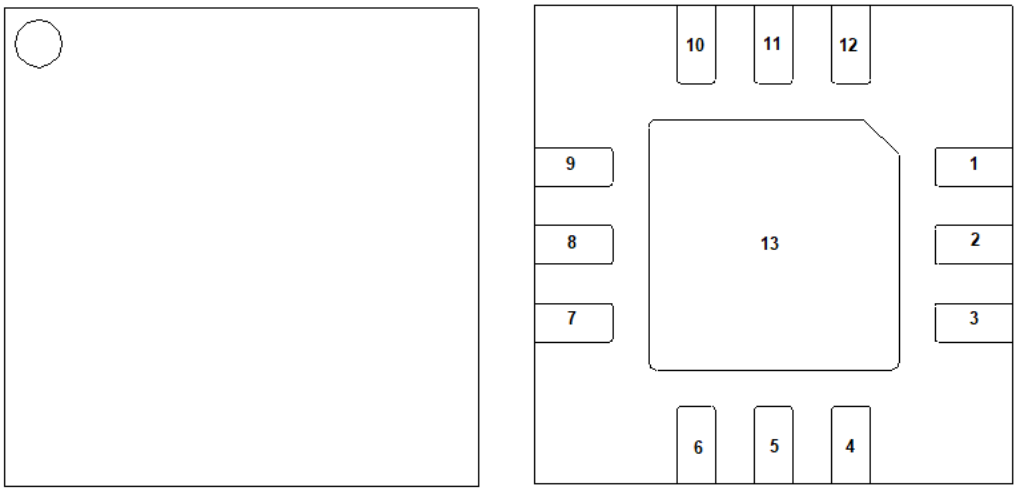


Package Pinout Diagram



Top View

Dot indicates Pin 1

Bottom View

Self Bias

Pin	Description
1,3, 4, 5, 6, 7, 9, 12	NC
2	RF Input
8	RF Output
10	Vd
11	Vctrl
13	GND

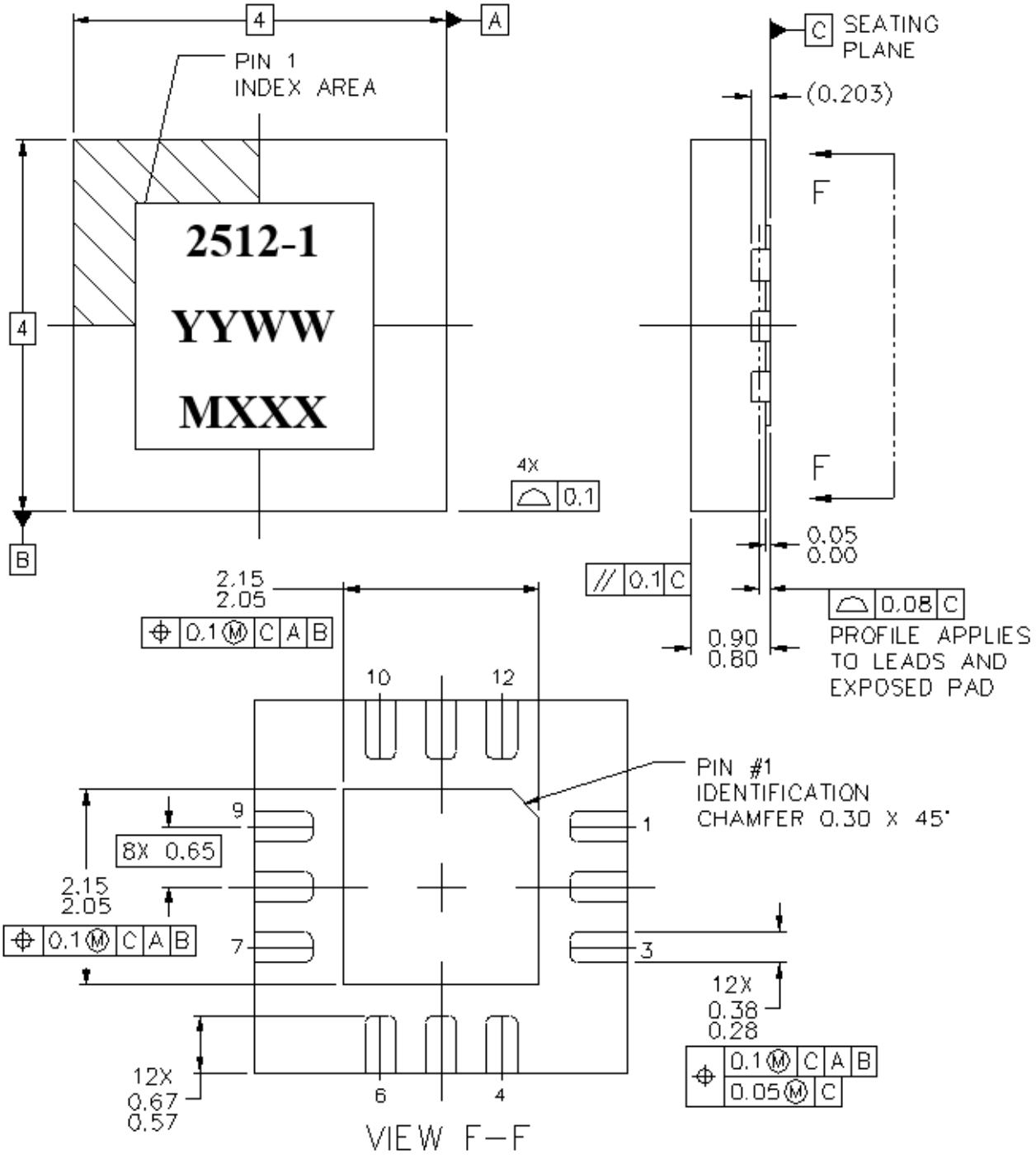
Self Bias: V_D = 5 V (I_D = ~90 mA), V_{CTRL} = 0 to +5 V for Gain adjustment

Gate Bias

Pin	Description
1,3, 4, 5, 6, 7, 9	NC
2	RF Input
8	RF Output
10	Vd
11	Vctrl
12	Vg
13	GND
13	Gnd

Gate Bias: V_D = 5 V, V_{CTRL} = 0 to +5 V for Gain adjustment V_G = Range, -0.5 to 0, typically ~ -0.1 will provide ~160 mA of Id.

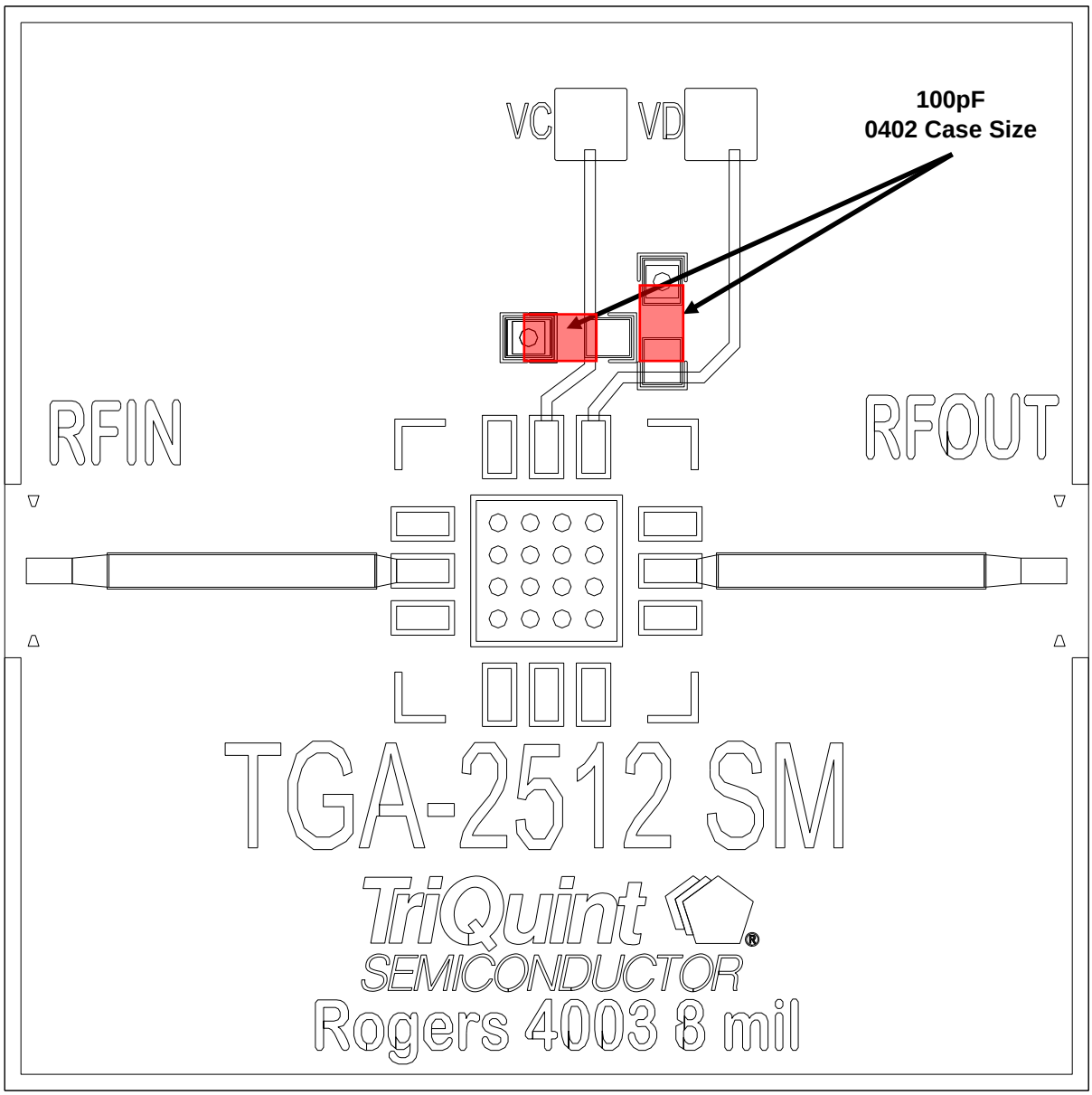
Mechanical Drawing



Dimensions in mm, package is mold encapsulated with Tin plated lead finish
Part Marking: 2512-1/2512-2: Part Number, YY = Part Assembly Year
WW = Part Assembly Week, MXXX = Batch ID

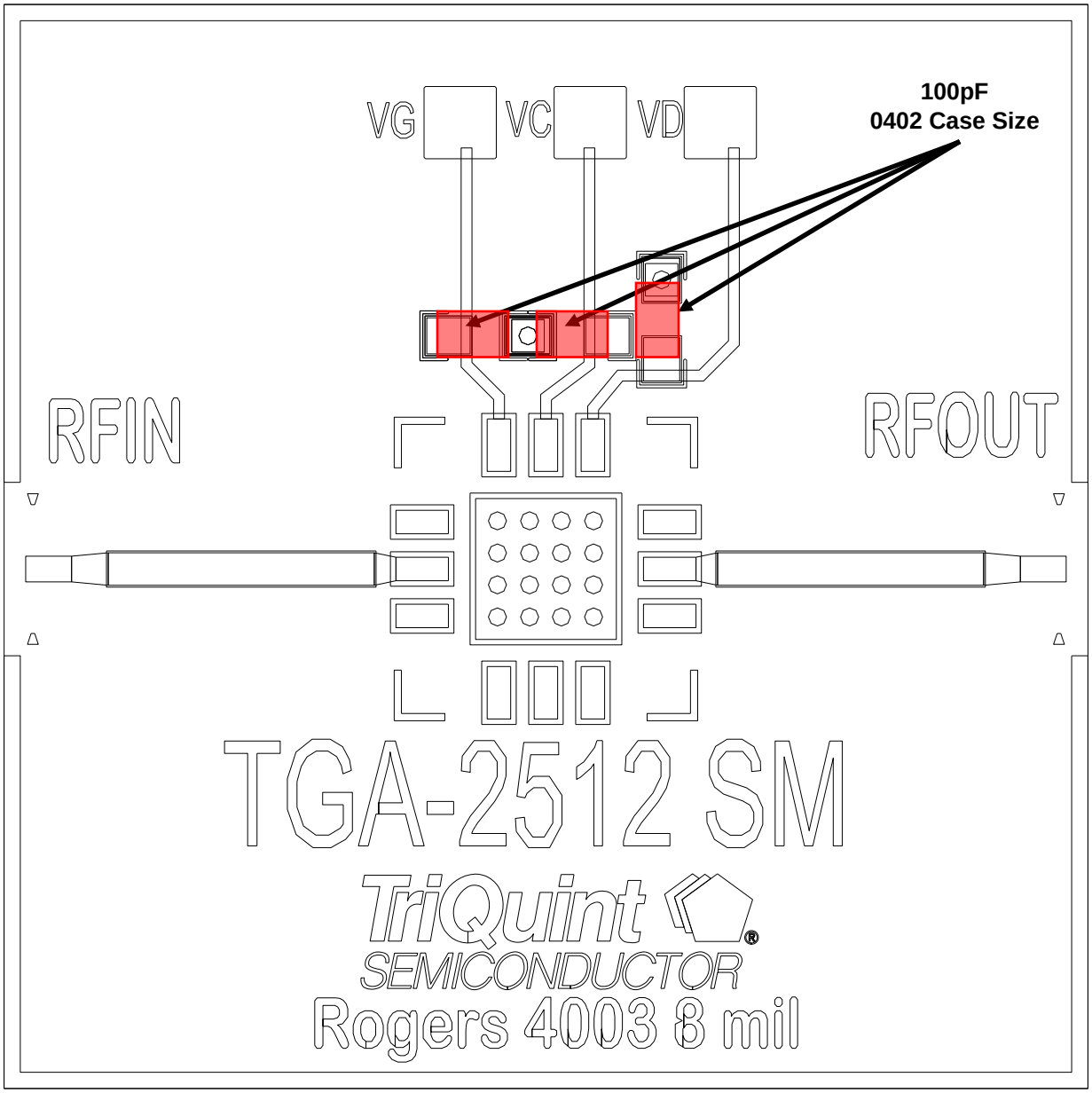
Recommended Board Layout Assembly

Self Bias



Recommended Board Layout Assembly

Gate Bias



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	TBD	ANSI/ESD/JEDEC JS-001

Caution!

ESD-Sensitive Device

Solderability

Use only AuSn (80/20) solder, and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

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