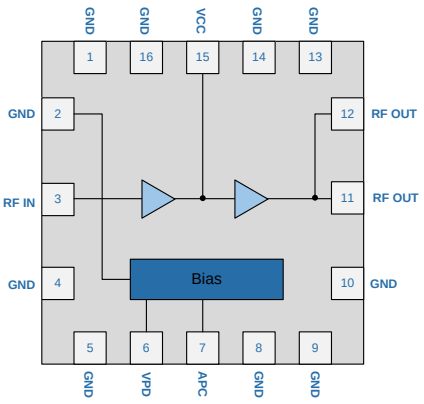
RFMD + TriQuint = Qorvo

RFPA2172

ISM Band 3.6V, 250mW AMP with Analog Gain Control

Package: QFN, 16-pin, 4.0mm x 4.0mm

The RFPA2172 is a medium-power high efficiency amplifier IC targeting 3.6 V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 2.45 GHz Bluetooth applications and frequency hopping/direct sequence spread-spectrum cordless telephones or other applications in the 902 MHz to 928 MHz ISM band. The device is packaged in a compact 4 mm x 4 mm QFN. The device features analog gain control to optimize transmit power while maximizing battery life in portable equipment requiring up to 100 mW transmit power at the antenna port.



Functional Block Diagram

Features

- 23.5dBm Typical Output Power
- 0dB to 28dB Variable Gain
- 45% Efficiency at Max Output
- On-Board Power Down Mode
- 2.4GHz to 2.5GHz Operation
- 902MHz to 928MHz Operation

Applications

- Bluetooth™ PA
- 2.4GHz to 2.5GHz ISM Band Systems
- 902MHz to 928MHz ISM Band Systems
- 3.6V Spread-Spectrum Cordless Phones
- Portable Battery-Powered Equipment
- Spread-Spectrum Systems

Ordering Information

RFPA2172	Standard 25 piece bag
RFPA2172SR	Standard 100 piece reel
RFPA2172TR13	Standard 2500 piece reel
RFPA2172TR13-5K	Standard 5000 piece reel
RFPA2172PCK-410	Fully assembled evaluation board tuned for 902MHz to 928MHz with 5 piece bag
RFPA2172PCK-411	Fully assembled evaluation board tuned for 2.4GHz to 2.5GHz with 5 piece bag

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	-0.5 to +6.0	V_{DC}
APC Current (Maximum)	+10	mA
Control Voltage (V_{PD})	-0.5 to +6.0	V_{DC}
Input RF Power	+10	dBm
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-55 to +155	°C

Caution! ESD sensitive device.

RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

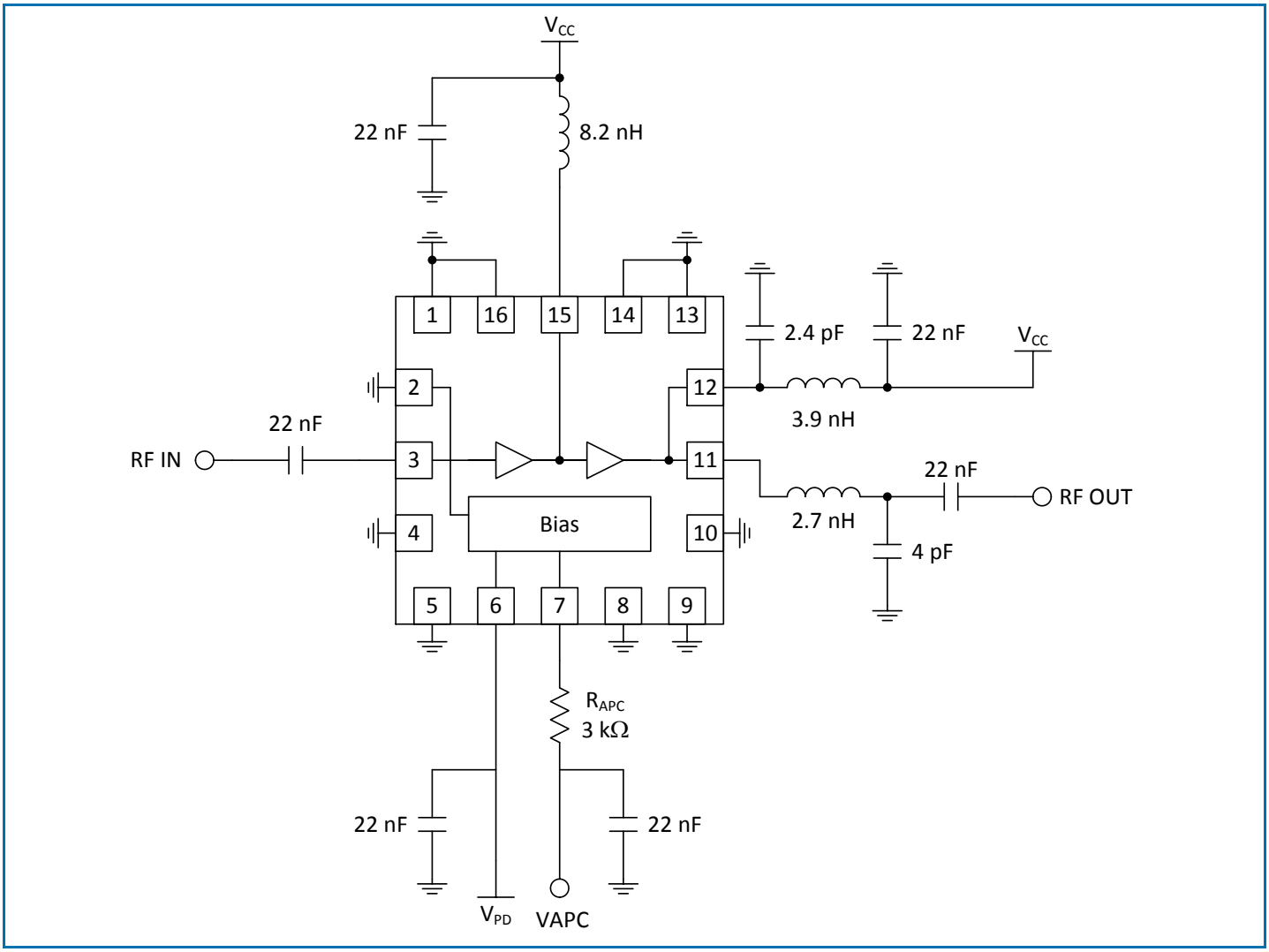
Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Nominal Operating Parameters

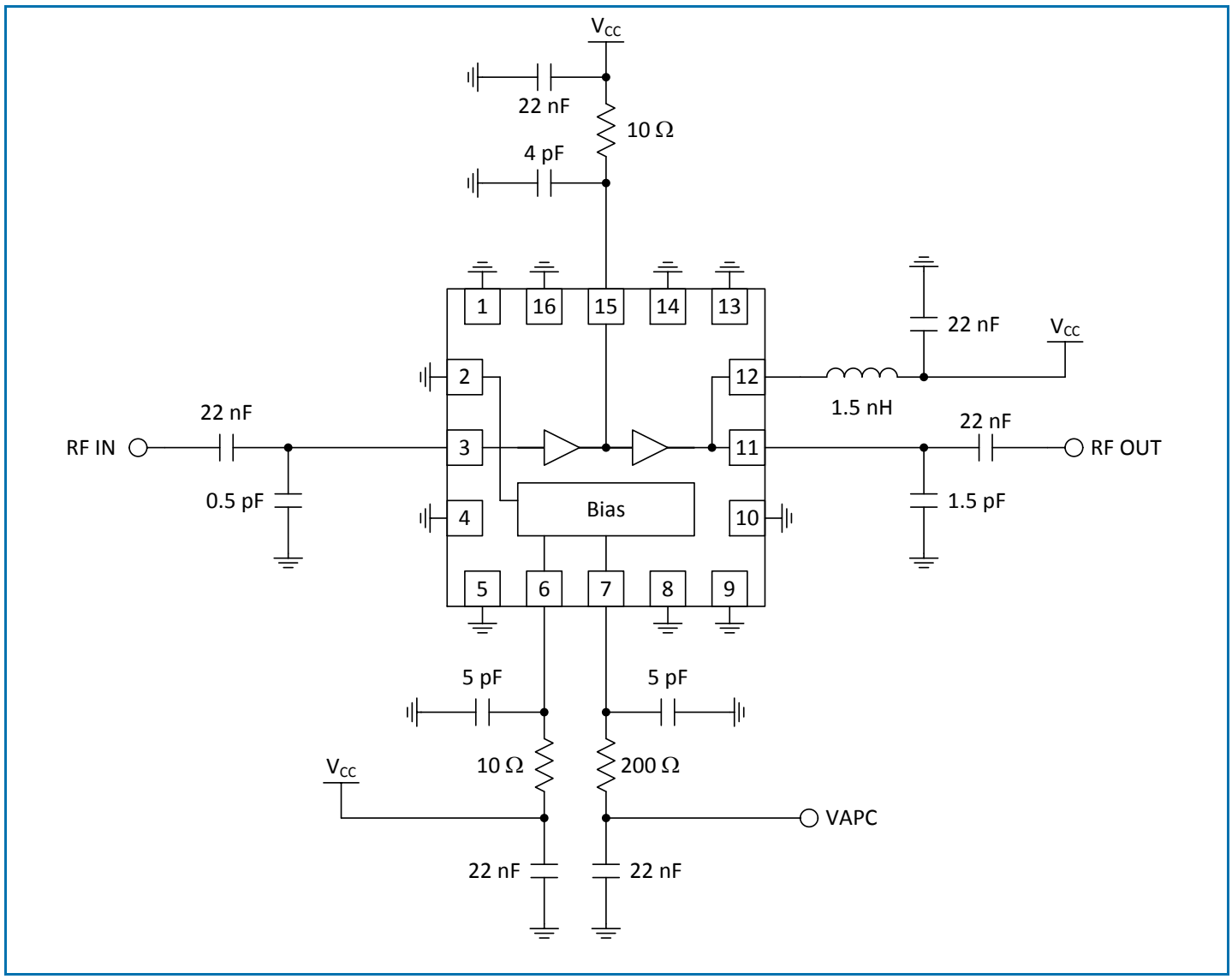
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Overall					**T= 25°C, V_{CC}= 3.6V, V_{PD}= 3.6V, V_{APC}= 3.0V**
Usable Frequency Range		400 to 2500		MHz	
Input Impedance		50		Ω	
Input VSWR		1.8:1			Without Input Match
Output Load VSWR	<10:1				0≤V_{APC}≤3.0V
	<6:1				0≤V_{APC}≤3.6V
2.45GHz Operation					**Freq= 2.4GHz to 2.5GHz, P_{IN}= 0dBm**
Operating Frequency		2.4 to 2.5		GHz	
Maximum Output Power	22	+23.5	24.5	dBm	
Total Efficiency		45		%	
Reverse Isolation		-45		dB	
Second Harmonic		-38	-34	dBc	
Third Harmonic		-45	-40	dBc	
All Other Spurious		-50		dBc	
Gain Control Voltage		0 to V_{CC}		V	
High Gain	23.5			dB	V_{APC}= 3.6V, V_{CC}= 3.6V, P_{IN}= 0dBm
Low Gain			-9	dB	V_{APC}= 0V, V_{CC}= 3.6V, P_{IN}= 0dBm
900MHz Operation					**Freq= 902MHz to 928MHz, P_{IN}= 3.0dBm**
Operating Frequency		902 to 928		MHz	
Maximum Output Power		+26		dBm	
Total Efficiency		58		%	
Reverse Isolation		-35		dB	
Second Harmonic		-40		dBc	
Third Harmonic		-40		dBc	
All Other Spurious		-50		dBc	
Gain Control Voltage		0 to V_{CC}		V	
Gain Control Slope		20	dB/V		
Gain		0 to 28	dB		

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Power Supply					
Power Supply Voltage	3.0	3.6		V	
Power Supply Current		155		mA	V_{CC}= 3.6V , V_{APC}= 3.6V, P_{IN}= -3dBm, V_{PD}= 3.6V
Power Supply Current – Low Power Mode		25		mA	T= 25°C, V_{CC}= 3.6V, V_{PD}= 3.6V, V_{APC}= 0V, P_{IN} = 0dBm
Idle Current		35	65	mA	V_{APC}= 3.6V, P_{IN}≤ -30dBm, V_{PD}= 3.6V
Power Down Current		2.8	10	µA	V_{CC}= 3.6V , V_{APC}= 0V, V_{PD}= 0V total I_{CC}
I(PD)		4.5		mA	V_{CC}= 3.6V , V_{PD}= 3.6V into PD pin
I(PD)		2.25		mA	V_{CC}= 3.0V , V_{PD}= 3.0V into PD pin

Application Schematic 915MHz



Application Schematic 2.45GHZ



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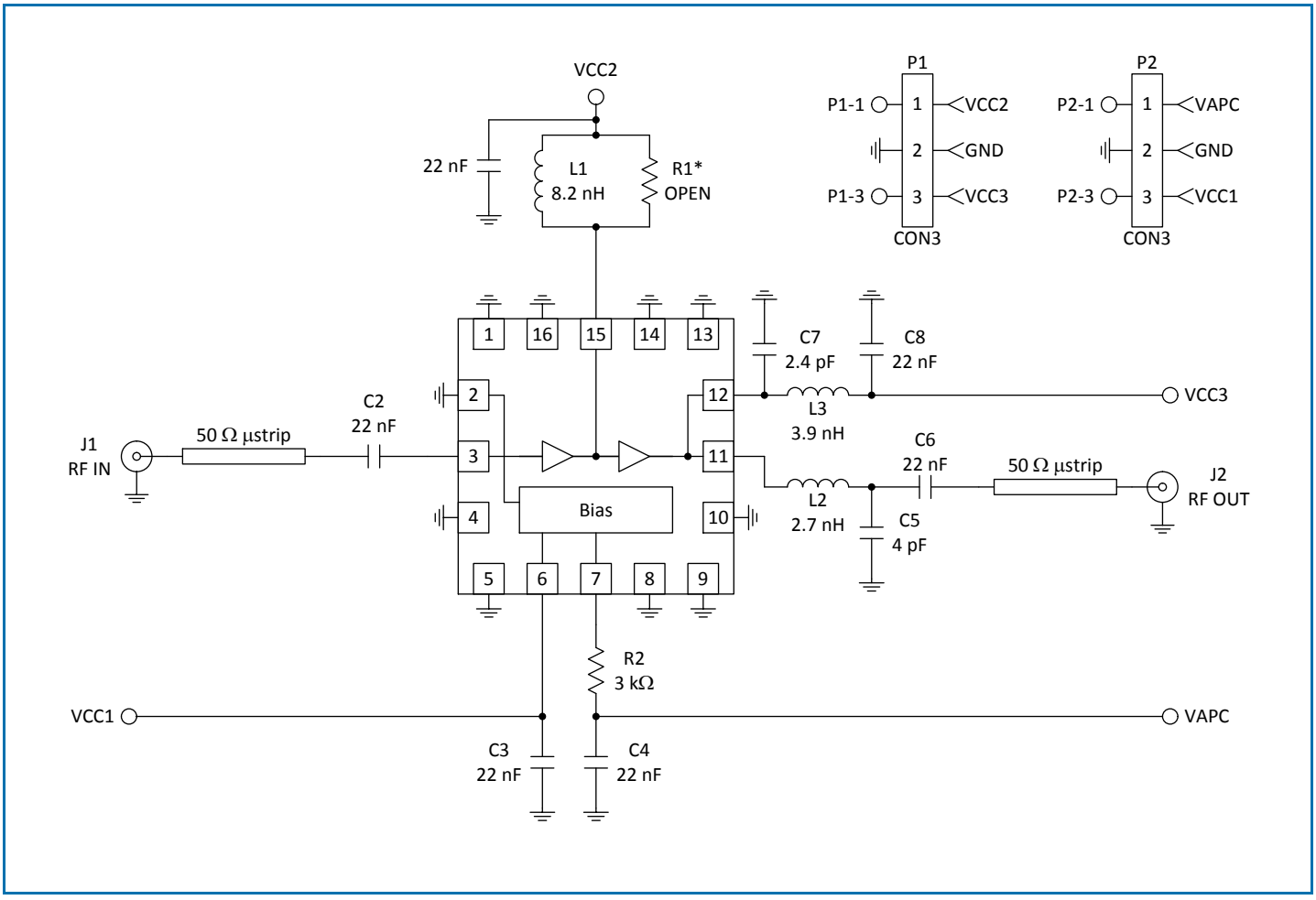
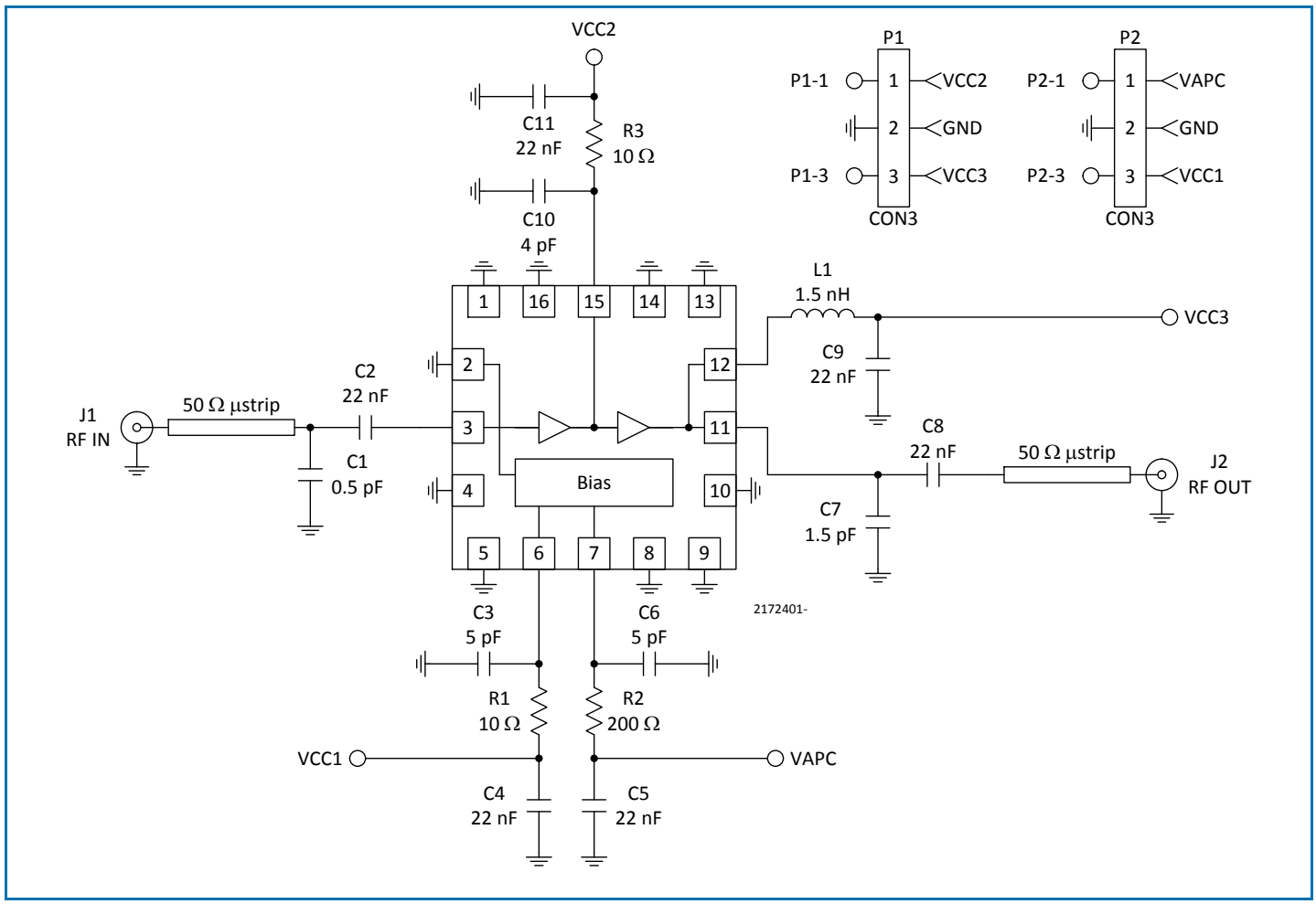
Evaluation Board Schematic 915 MHz



Evaluation Board Schematic 2.45GHz



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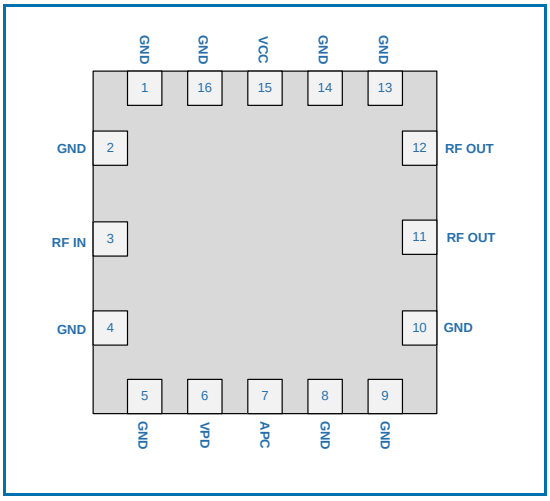
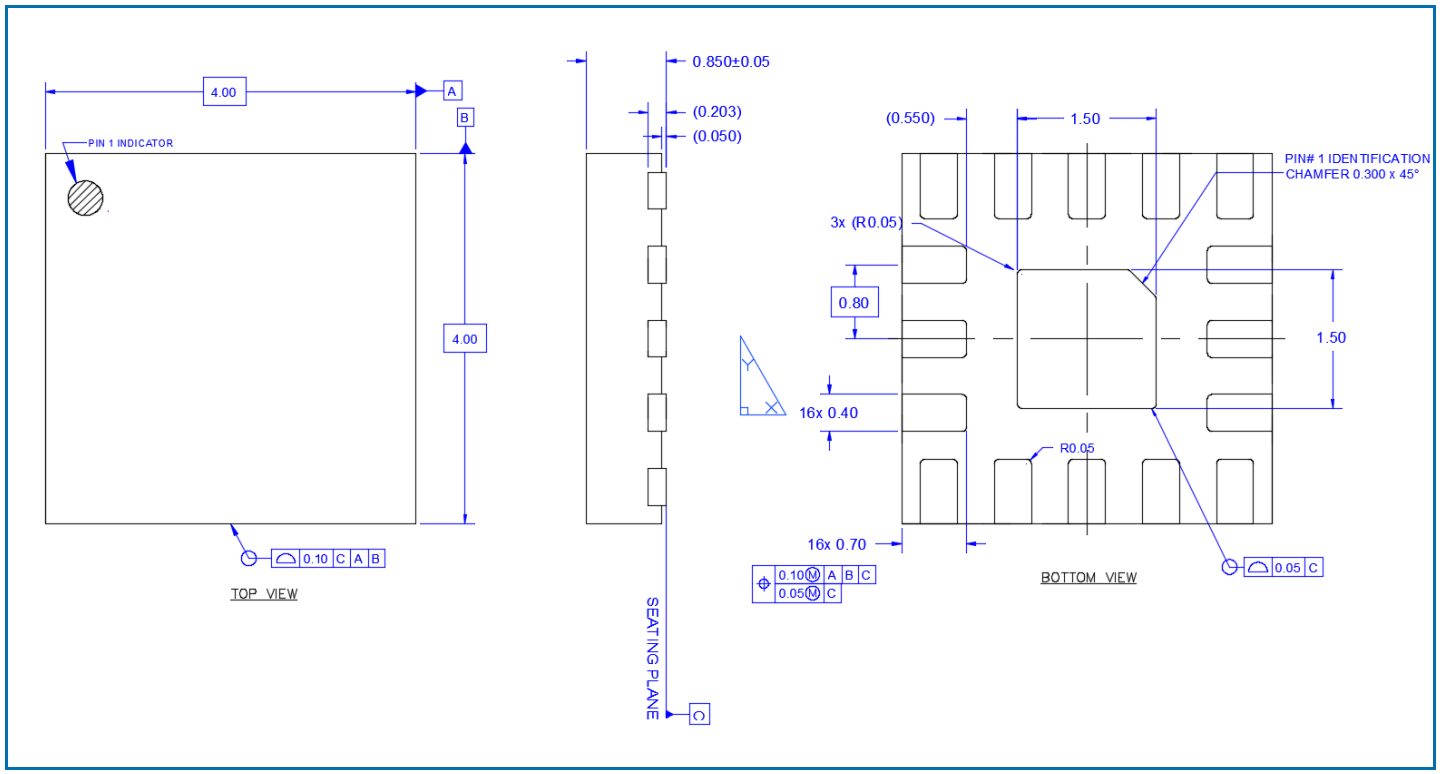
Pin Out



Package Outline Drawing (Dimensions in millimeters)



PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3 µinch to 8 µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

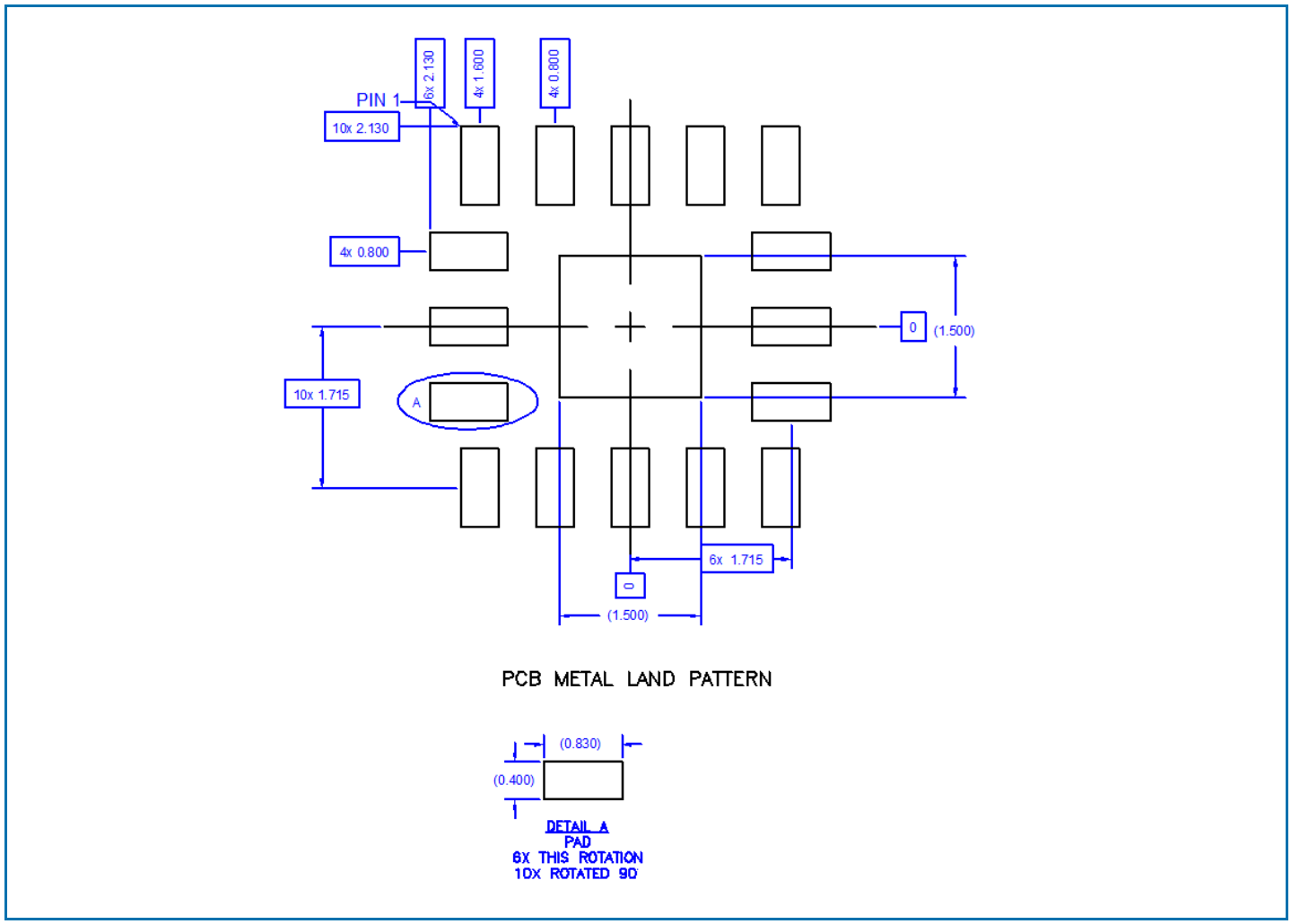


Figure 1. PCB Metal Land Pattern (Top View)

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PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

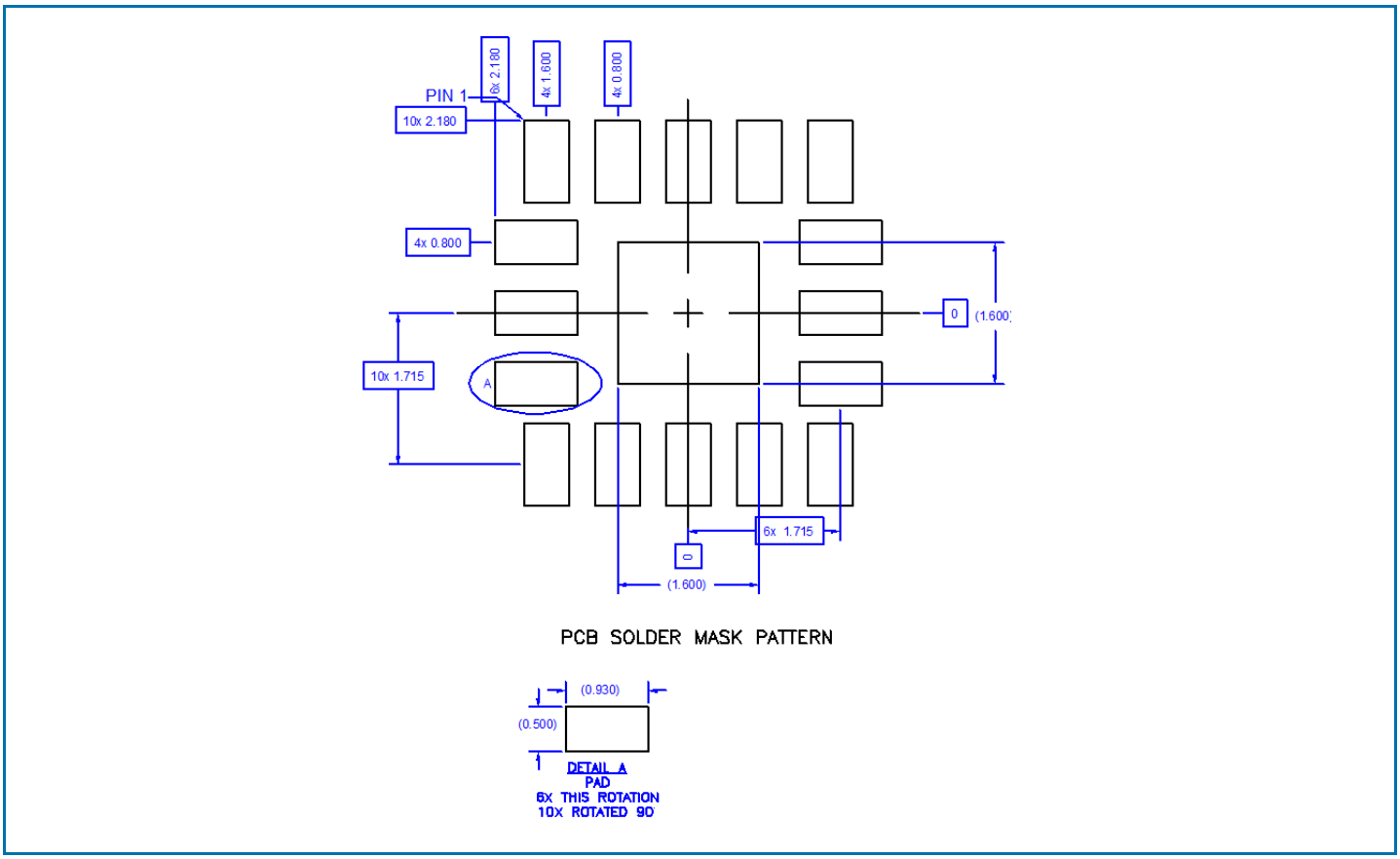


Figure 2. PCB Solder Mask (Top View)

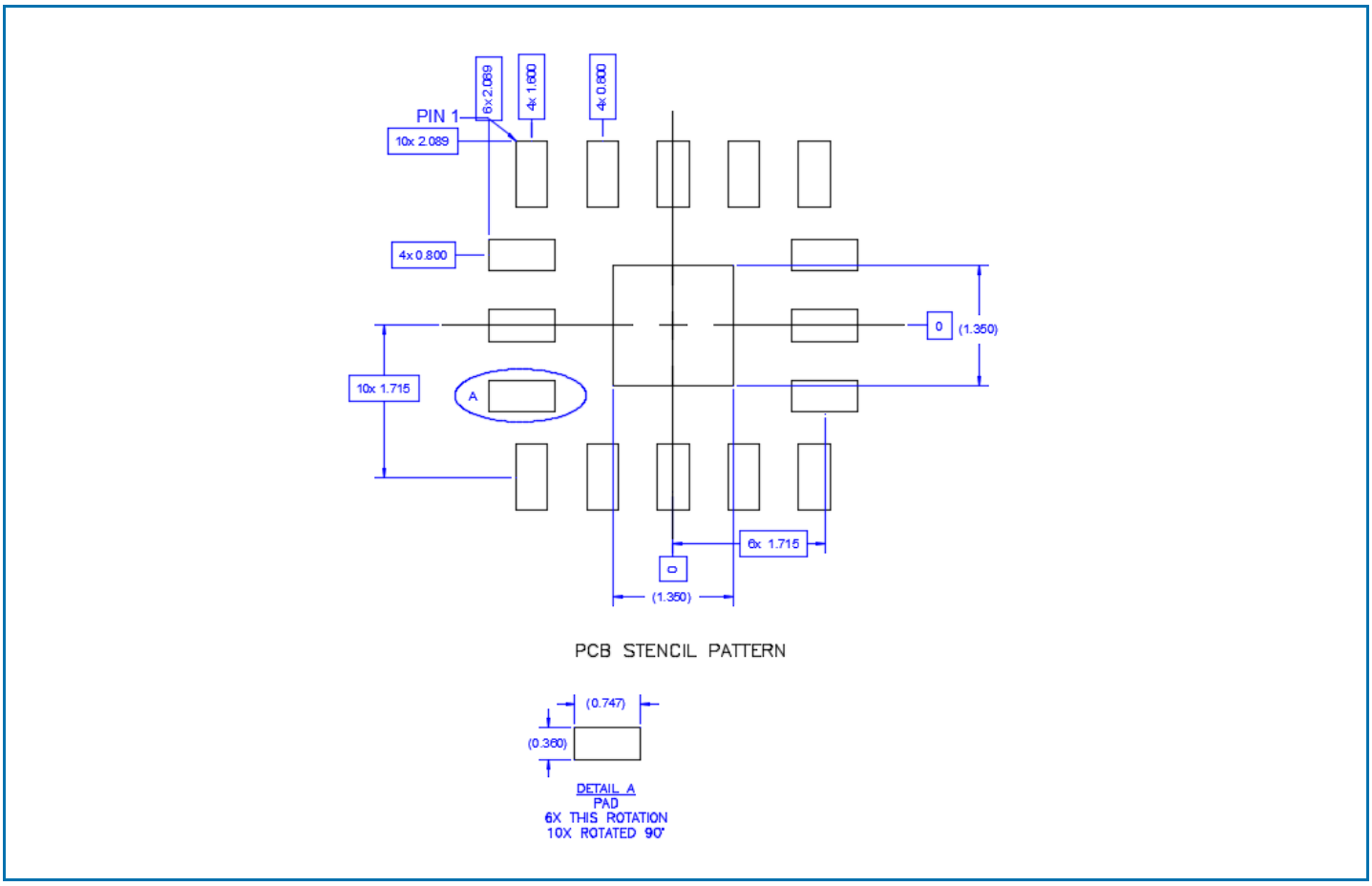


Figure 3. PCB Stencil Pattern (Top View)

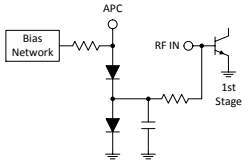
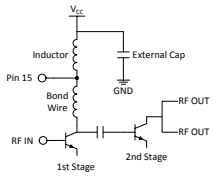
Thermal Pad and Via Design

The PCB metal land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

Pin Names and Descriptions

Pin	Name	Description	Interface Schematic
1	GND	Ground connection. For best performance, keep traces physically short and connect immediately to the ground plane.	
2	GND	Ground connection for the driver stage. For best performance, keep traces physically short and connect immediately to the ground plane.	
3	RF IN	RF input. This is a 50Ω input. No external matching is needed. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	See pin 15
4	GND	See pin 1.	
5	GND	See pin 1.	
6	VPD	Power down pin. When this pin is OV, the device will be in power down mode, dissipating minimum DC power. This pin also serves as the V_{CC} supply pin for the bias circuitry. V_{PD} should be at the supply voltage when the part is not in power down mode.	
7	APC	Analog power control. Output power varies as a function of the voltage on this pin. See graph. This pin must be driven through a series resistor with a voltage between OV and VCC. Series resistor determines dynamic range of power control. See plot "P_{OUT} versus Gain Control versus Gain Control Resistor".	
8	GND	See pin 1.	
9	GND	See pin 1.	
10	GND	See pin 1.	
11	RF OUT	RF output. An external matching network is required to provide the optimum load impedance at this pin.	See pin 15
12	RF OUT	RF output and power supply for the output stage. Bias voltage for the output stage is provided through this pin. A shunt cap resonating with the bond wire inductance at 2xfo can also be used at this pin to provide a second harmonic trap.	See pin 15
13	GND	See pin 1.	
14	GND	See pin 1.	
15	VCC	Power supply for driver stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage. Refer to the application schematic for the proper configuration. Note: Position and value of the components are important.	
16	GND	See pin 1.	
Pkg Base	GND	Ground connection for the output stage. This pad should be connected to the groundplane by vias directly under the device. A short path is required to obtain optimum performance, as well as provide a good thermal path to the PCB for maximum heat dissipation.	

Mouser Electronics

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Qorvo:

RFPA2172 RFPA2172TR13 RFPA2172SR