# QPD3640

## 150 W / 300 W, 48 V, 3.4 – 3.8 GHz, Asymmetric Doherty

## Product Overview

The QPD3640 is a dual-path discrete GaN on SiC HEMT which operates on LTE downlink Band 42 (3.4-3.6 GHz) and Band 43 (3.6-3.8 GHz). The device is a single-stage, matched, power Doherty amplifier transistor.

QPD3640 can deliver P4dB of 389 W at +50 V operation.

Lead free and RoHS compliant.


4-Lead NI780 Package

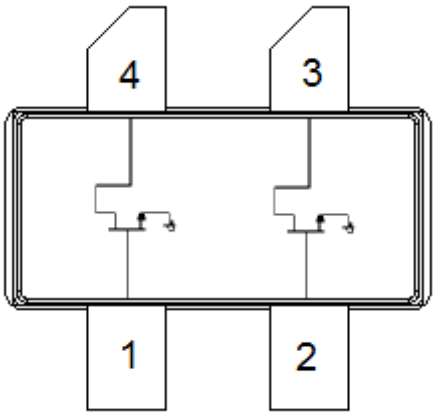
## Key Features

- Operating Frequency Range: 3.4 – 3.8 GHz
- Operating Drain Voltage: +48 V
- Doherty Output Power at P4dB: 389 W (1)
- Doherty Drain Efficiency P4dB: 57.4% (1)
- Doherty Linear Gain: 15.6 dB (1)
- 4-Lead, Earless, Ceramic NI780 Package

Note:

1. Based on pulsed P4dB performance at 3.75 GHz.

## Functional Block Diagram




## Applications

- WCDMA / LTE
- Macrocell Base Station
- Asymmetric Doherty Applications

## Ordering Information

| Part Number | Description |
|---|---|
| QPD3640SR | Short Reel – 100 Pieces |
| QPD3640TR13 | 13” Reel – 2500 Pieces |
| QPD3640EVB02 | 3.5 – 3.7 GHz Doherty Eval. Board |
| QPD3640EVB03 | 3.4 – 3.6 GHz Doherty Eval. Board |
| QPD3640EVB04 | 3.6 – 3.8 GHz Doherty Eval. Board |

## Absolute Maximum Ratings

| Parameter | Rating |
|---|---|
| Breakdown Voltage ($BV_{DG}$) | +165 V |
| Gate Voltage Range ($V_{G1,2}$) | −7 to +2 V |
| Drain Voltage ($V_{D1,2}$) | +55 V |
| Peak RF Input Power | +42 dBm |
| VSWR Mismatch, P1dB Pulse (10% Duty Cycle, 100 µs Width), T = +25°C | 10:1 |
| Storage Temperature | −65 to +150°C |

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to device may reduce device reliability.

## Recommended Operating Conditions

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Carrier Gate Voltage ($V_{G1}$) | | −2.8 | | V |
| Peaking Gate Voltage ($V_{G2}$) | | −5.5 | | V |
| Drain Voltage ($V_{D1,2}$) | | +48 | | V |
| Carrier Quiescent Current ($I_{DQ1}$) | | 342 | | mA |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Operational Frequency Range | | 3600 | | 3800 | MHz |
| Carrier Quiescent Drain Current | | | 342 | | mA |
| Linear Doherty Gain | P4dB | | 15.6 | | dB |
| Doherty Output Power | P4dB | | 55.9 | | dBm |
| Doherty Drain Efficiency | P4dB | | 57.4 | | % |
| Carrier Amplifier Gate Leakage | | | 27.5 | | mA |
| Peaking Amplifier Gate Leakage | | | 48.0 | | mA |

Test conditions unless otherwise noted: $V_{D1,2}$ = +50 V, $I_{DQ1}$ = 342 mA, $V_{G2}$ = −5.5 V, T = +25°C, Pulsed (10% Duty Cycle, 100 µs Width) at 3750 MHz on a reference design fixture.

## Thermal Information

| Parameter | Conditions | Values | Units |
|---|---|---|---|
| Thermal Resistance, Peak IR Surface Temperature at Average Power ($\theta_{JC}$) | $T_{CASE}$ = +105°C, $T_{CH}$ = 144°C<br>CW: $P_{DISS}$ = 36.9 W, $P_{OUT}$ = 42.2 W | 1.1 | °C/W |

Notes:

1. Based on expected carrier amplifier efficiency of Doherty.
2. $P_{OUT}$ assumes 25% peaking amplifier contribution of total average Doherty rated power.
3. Thermal resistance is measured to package backside.
4. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

## Carrier Amplifier Power-Matched Load Pull Performance

| Frequency (MHz) | Source Impedance (Ω) | Load Impedance (Ω) | P3dB (dBm) | Drain Efficiency (%) | G3dB (dB) |
|---|---|---|---|---|---|
| 3400 | 5.42 – j18.78 | 5.79 – j1.66 | 53.5 | 60.8 | 16.2 |
| 3600 | 8.92 – j22.51 | 3.84 – j2.29 | 53.5 | 59.7 | 16.9 |
| 3800 | 13.12 – j9.38 | 3.06 – j4.53 | 53.2 | 57.1 | 15.7 |

Test conditions unless otherwise noted: $V_{D1}$ = +50 V, $I_{DQ1}$ = 342 mA, T = +25°C, Pulsed (10% Duty Cycle, 100 µs Width), P3dB.

## Carrier Amplifier Efficiency-Matched Load Pull Performance

| Frequency (MHz) | Source Impedance (Ω) | Load Impedance (Ω) | P3dB (dBm) | Drain Efficiency (%) | G3dB (dB) |
|---|---|---|---|---|---|
| 3400 | 5.42 – j18.78 | 10.84 – j7.86 | 51.6 | 73.1 | 18.6 |
| 3600 | 8.92 – j22.51 | 11.09 – j1.54 | 51.4 | 72.7 | 20.1 |
| 3800 | 13.12 – j9.38 | 5.40 – j2.12 | 52.1 | 68.1 | 18.2 |

Test conditions unless otherwise noted: $V_{D1}$ = +50 V, $I_{DQ1}$ = 342 mA, T = +25°C, Pulsed (10% Duty Cycle, 100 µs Width), P3dB.

## Peaking Amplifier Power-Matched Load Pull Performance

| Frequency (MHz) | Source Impedance (Ω) | Load Impedance (Ω) | P1dB (dBm) | Drain Efficiency (%) | G1dB (dB) |
|---|---|---|---|---|---|
| 3400 | 3.81 – j15.15 | 11.42 – j7.78 | 55.2 | 62.2 | 15.0 |
| 3600 | 10.48 – j14.41 | 9.16 – j4.02 | 55.1 | 59.9 | 14.8 |
| 3800 | 5.02 – j4.01 | 7.68 – j2.60 | 55.2 | 58.1 | 13.9 |

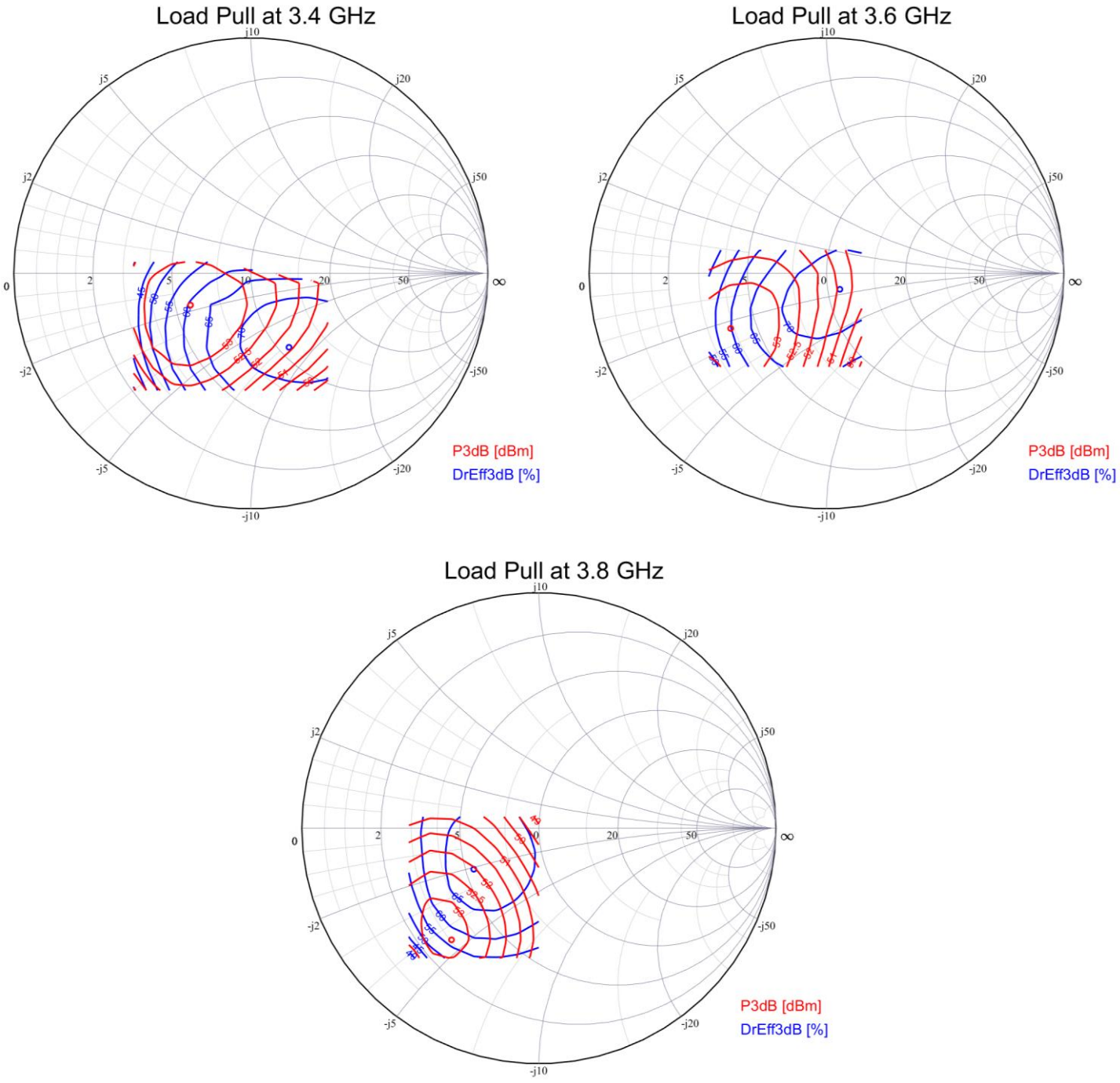
Test conditions unless otherwise noted: $V_{D2}$ = +50 V, $V_{G2}$ = −4.5 V, T = +25°C, Pulsed (10% Duty Cycle, 100 µs Width), P1dB.

## Peaking Amplifier Efficiency-Matched Load Pull Performance

| Frequency (MHz) | Source Impedance (Ω) | Load Impedance (Ω) | P1dB (dBm) | Drain Efficiency (%) | G1dB (dB) |
|---|---|---|---|---|---|
| 3400 | 3.81 – j15.15 | 6.34 – j13.35 | 53.7 | 73.9 | 16.0 |
| 3600 | 10.48 – j14.41 | 9.15 – j11.99 | 53.5 | 71.7 | 15.6 |
| 3800 | 5.02 – j4.01 | 13.28 – j9.19 | 53.7 | 68.2 | 14.4 |

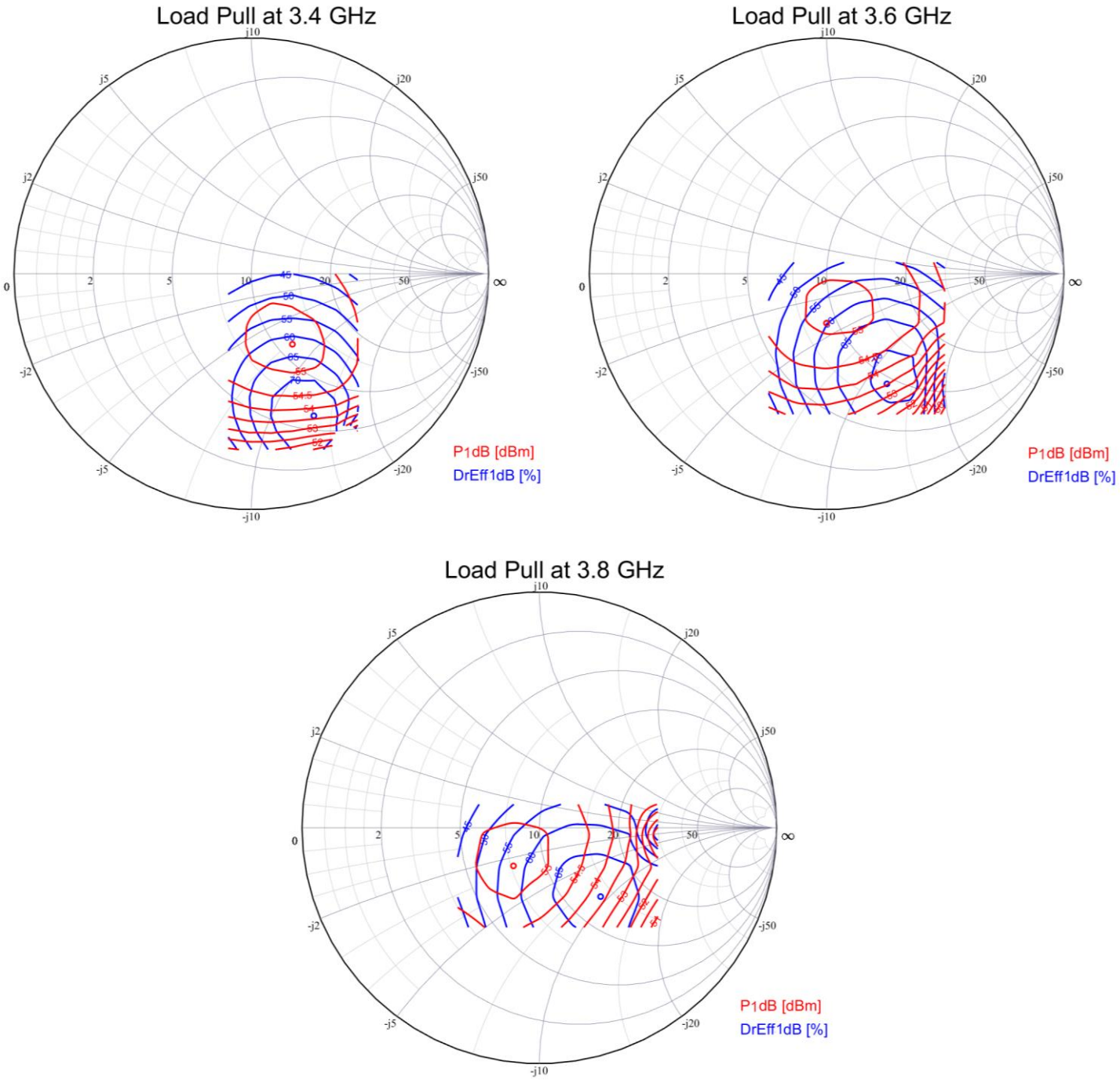
Test conditions unless otherwise noted: $V_{D2}$ = +50 V, $V_{G2}$ = −4.5 V, T = +25°C, Pulsed (10% Duty Cycle, 100 µs Width), P1dB.

## Carrier Amplifier Load Pull Plots




Test conditions unless otherwise noted: $V_{D1}$ = +50 V, $I_{DQ1}$ = 342 mA, T = +25°C, Pulsed (10% Duty Cycle, 100 µs Width), P3dB.

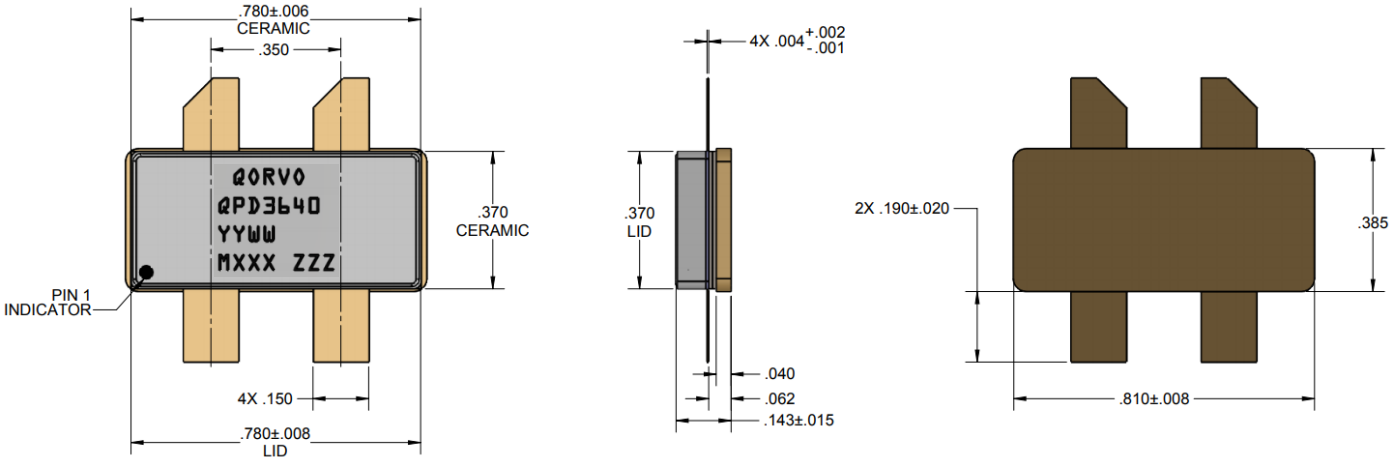
## Peaking Amplifier Load Pull Plots




Test conditions unless otherwise noted: $V_{D2}$ = +50 V, $V_{G2}$ = −4.5 V, T = +25°C, Pulsed (10% Duty Cycle, 100 µs Width), P1dB.

## Package Marking and Dimensions

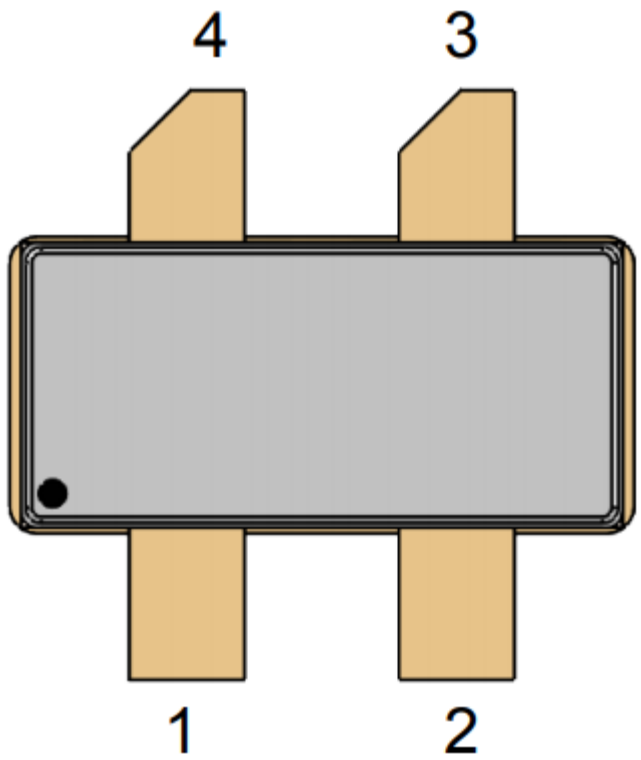
Marking: Qorvo Logo
Part Number – QPD3640
Date Code – YYWW
Lot Code – MXXX
Serial Number – ZZZ



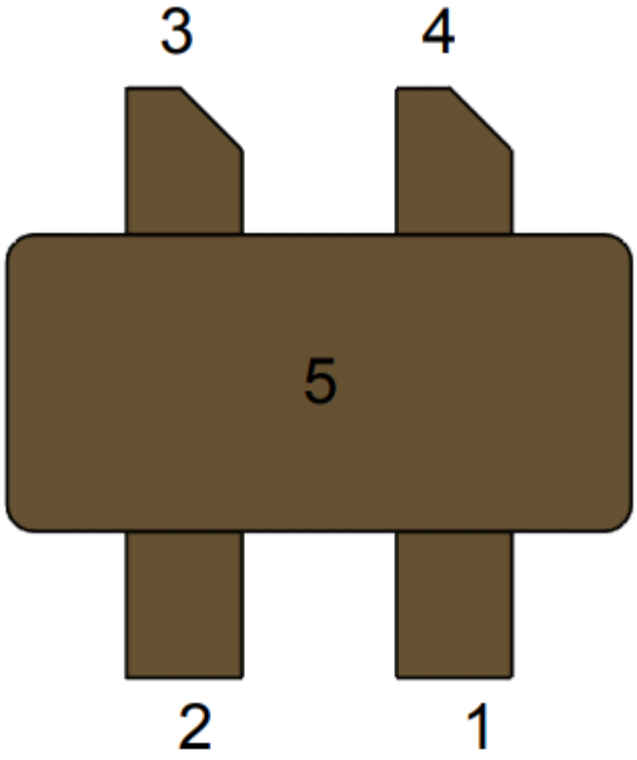

Notes: Unless Otherwise Specified;

1. Material:
   Package Base: Ceramic/Metal
   Package Lid: Ceramic
2. Package exposed metal base and leads are NiAu plated. Au thickness is minimum 60 µin.
3. Part is epoxy sealed.
4. Part meets industry standard NI780 footprint.
5. Body dimensions do not include lid shift or epoxy run out, which can be up to 0.020 inches per side.
6. All dimensions are in inches. Angles are in degrees.
7. General tolerance is ±0.005 unless otherwise shown.

## Pin Configuration and Description




Top View



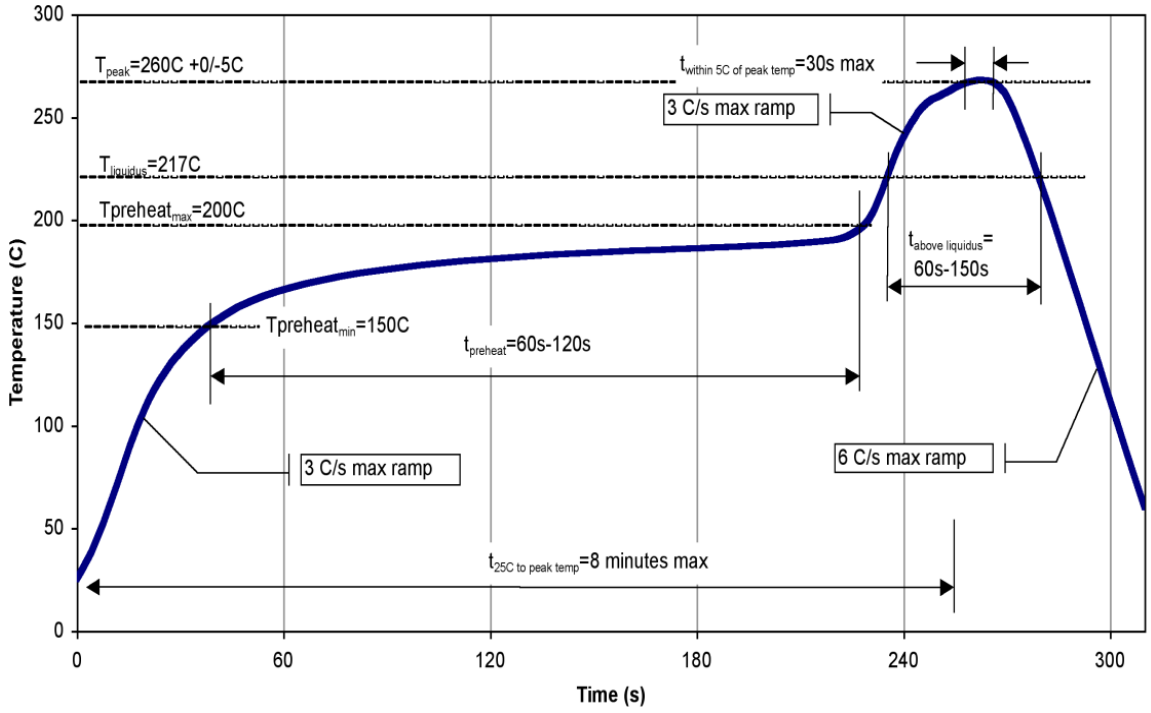

Bottom View

| Pin Number | Label | Description |
|---|---|---|
| 1 | RF IN 1, VG1 | Carrier Amplifier RF Input, Gate Bias |
| 2 | RF IN 2, VG2 | Peaking Amplifier RF Input, Gate Bias |
| 3 | RF OUT 2, VD2 | Peaking Amplifier RF Output, Drain Bias |
| 4 | RF OUT 1, VD1 | Carrier Amplifier RF Output, Drain Bias |
| 5 (Backside Paddle) | RF/DC GND | RF/DC Ground |

## Doherty Biasing Procedure

| Bias On | Bias Off |
|---|---|
| 1. Turn ON $V_{G1}$ and $V_{G2}$ to −4 V.<br>2. Turn ON $V_{D1}$ and $V_{D2}$ to +50 V.<br>3. Adjust $V_{G2}$ until $I_{D2}$ = 600 mA ($V_{G2\_SET}$).<br>4. Subtract 2.5 V from $V_{G2\_SET}$ ($V_{G2}$ = $V_{G2\_SET}$ – 2.5 V). (Typically, $V_{G2}$ = −5.5 V.)<br>5. Adjust $V_{G1}$ until $I_{D1}$ = 342 mA. (Typically, $V_{G1}$ = −2.8 V.)<br>6. Turn ON RF. | 1. Turn OFF RF.<br>2. Adjust $V_{G1}$ and $V_{G2}$ to −5 V.<br>3. Turn OFF $V_{D1}$ and $V_{D2}$.<br>4. Wait two (2) seconds to allow drain capacitor charge to dissipate.<br>5. Turn OFF $V_{G1}$ and $V_{G2}$. |

## Recommended Solder Temperature Profile



## Handling Precautions

| Parameter | Rating | Standard |
|---|---|---|
| ESD – Human Body Model (HBM) | Class 1B (500 V) | ANSI/ESDA/JEDEC Standard JS-001 |
| ESD – Charged Device Model (CDM) | Class C3 (1000 V) | ANSI/ESDA/JEDEC Standard JS-002 |
| MSL – Moisture Sensitivity Level | Level 3 | IPC/JEDEC Standard J-STD-020 |

Caution!
ESD-Sensitive Device

## Solderability

Compatible with lead-free (260°C maximum reflow temperature) soldering processes.
The use of no-clean solder to avoid washing after soldering is recommended.
Package lead plating is NiAu. Au thickness is minimum 60 µin.

## RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free


## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Web:** www.qorvo.com **Tel: 1-844-890-8163**

**Email:** customer.support@qorvo.com

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