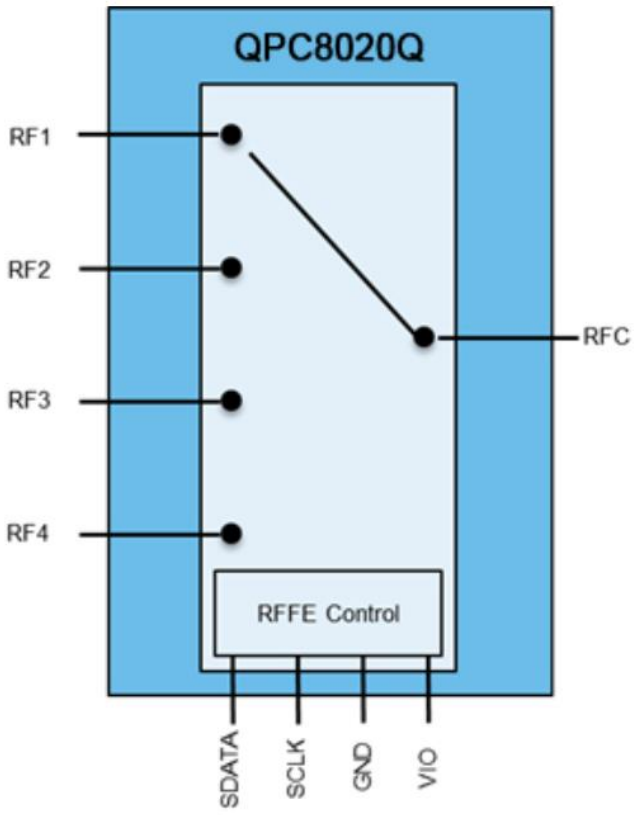
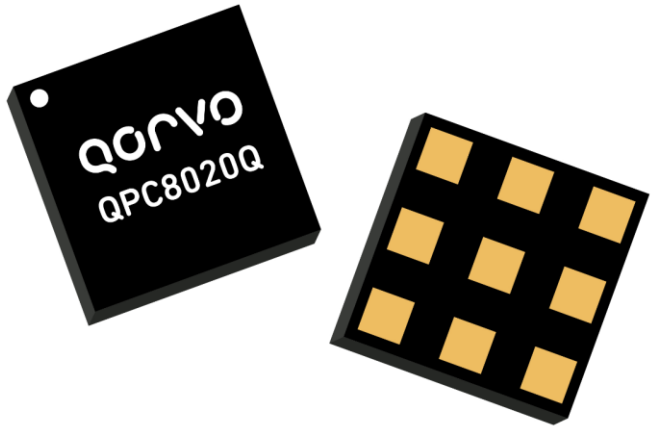
QPC8020Q
SP4T RFFE GSM HIGH POWER SWITCH

Product Description

The QPC8020Q is a low loss, high isolation SP4T switch with performance optimized for GSM, CDMA, WCDMA, & LTE applications requiring high linearity and high power handling. The QPC8020Q is packaged in a compact 1.1mm x 1.1mm, 9-pin module which allows for a small solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

Functional Block Diagram





9 Pin 1.1 x 1.1 x 0.44 mm Package

Feature Overview

- Qualified to AEC-Q100 Grade 2
- Low Insertion Loss
- High Port-to-Port Isolation
- RFFE 2.0 compatible (52MHz Write speed)
- Capable of 1.8V operation
- Usable up to 6GHz
- HBM Rating > 1kV on all ports
- Compact size: 1.1mm x 1.1mm x 0.44mm
- DC blocking capacitors are not required in typical applications

Applications

- Telematics Modules
- Cellular Technology Applications
- Multi-Mode GSM, EDGE, WCDMA, and LTE Applications

Ordering Information

PART NO.	DESCRIPTION
QPC8020QSB	5-pc Sample Bag
QPC8020QSR	100-pc, 7” Reel
QPC8020QTR13	5000-pc, 13” Reel
QPC8020QDK	Fully Assembled Evaluation Kit

Absolute Maximum Ratings

PARAMETER	RATING
Storage Temperature	-65 to +150 °C
Operating Junction Temperature	+125° C
V_{IO}	2.5 V
SDATA, SCLK	2.5 V
Maximum Power Handling	39 dBm, 1:1 VSWR, +25°C, 25% duty cycle

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

PARAMETER	MIN.	TYP.	MAX.	UNITS
Operating Ambient Temperature	-40	+25	+105	°C
V_{IO} Supply Voltage	1.65	1.8	1.95	V
V_{IO} Supply Current (Active Mode)		30	55	µA
V_{IO} Supply Current (Low Power Mode)		3		µA
SDATA, SCLK Logic Low (Input)	0.00	0.00	0.3 x VIO	V
SDATA, SCLK Logic High (Input)	0.7 x VIO	1.8	VIO	V
SDATA Logic Low (Output)	0.00	0.00	0.2 x VIO	V
SDATA Logic High (Output)	0.8 x VIO	1.8	VIO	V
SDATA, SCLK Logic High Current		0.1	5	µA
Turn-On Time			20	µs
Switching Speed (50% of rising edge of last SCLK to 90% RF)		2	4	µs

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications[1]

Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, Input and Output = 50Ω, T = 25°C, V_{IO} = 1.8V, SDATA/SCLK = 1.8 V / 0 V

PARAMETER	CONDITIONS[1]	MIN.	TYP.	MAX.	UNITS
Frequency Range		600		6000	MHz
Insertion Loss					
RF1/2/3/4 to RFCOM	600 MHz to 960 MHz		0.22	0.45	dB
RF1/2/3/4 to RFCOM	1700 MHz to 2200 MHz		0.29	0.6	dB
RF1/2/3/4 to RFCOM	2300 MHz to 2700 MHz		0.34	0.65	dB
RF1/2/3/4 to RFCOM	3300 MHz to 4200 MHz		0.46	0.85	dB
RF1/2/3/4 to RFCOM*			0.6		dB
RF1/2/3/4 to RFCOM	4400 MHz to 5000 MHz		0.9		dB
RF1/2/3/4 to RFCOM*			0.7		dB
RF1/2/3/4 to RFCOM	5000 MHz to 6000 MHz		1.55		dB
RF1/2/3/4 to RFCOM*			0.85		dB
Isolation					
Port to Port / Port to RFCOM	Refer to Isolation Matrix				
Harmonics					
3Fo (B17)	Fo = 704MHz; P_{in} = 25dBm; CW		-88		dBm
2Fo (B13)	Fo = 786.5MHz; P_{in} = 25dBm; CW		-91		dBm
2Fo (B8)	Fo = 897.5MHz; P_{in} = 25dBm; CW		-93		dBm
2Fo (GSM 850/900)	Fo = 824 – 915MHz; Pin = 35dBm; CW		-69	-61	dBm
3Fo (GSM 850/900)	Fo = 824MHz; Pin = 27dBm; CW		-83	-64	dBm
≥ 4Fo - 8GHz (GSM 850/900)	Fo = 824 – 915MHz; Pin = 35dBm; CW		-96		dBm
2Fo (GSM DCS/PCS)	Fo =1910MHz; Pin = 33dBm; CW		-70	-56	dBm
3Fo (GSM DCS/PCS)	Fo =1910MHz; Pin = 33dBm; CW		-62	-45	dBm
4Fo (GSM DCS/PCS)	Fo = 1710 – 1980MHz; Pin = 32dBm; CW		-93		dBm
2Fo (B7)	Fo = 2570MHz; Pin = 27dBm; CW		-81		dBm
IMD2	Ftx = 20dBm; Fint = -15dBm				
Band VIII	Ftx = 880 MHz, Fint = 1805 MHz, Fmeas = 925 MHz, Measure on all Pins		-122		dBm
Band II	Ftx = 1880 MHz, Fint = 3840 MHz, Fmeas = 1960 MHz, Measure on all Pins		-120		dBm
Band VII	Ftx = 2535 MHz, Fint = 5190 MHz, Fmeas = 2655 MHz, Measure on all Pins		-119		dBm
IMD3	Ftx = 20dBm; Fint = -15dBm				
Band VIII	Ftx = 897.5 MHz, Fint = 852.5 MHz, Fmeas = 942.5 MHz, Measure on all Pins		-126		dBm
Band II	Ftx = 1880 MHz, Fint = 1800 MHz, Fmeas = 1960 MHz, Measure on all Pins		-127		dBm
Band VII	Ftx = 2535 MHz, Fint = 2415 MHz, Fmeas = 2655 MHz, Measure on all Pins		-125		dBm

* See tuning schematic for 5000MHz to 6000MHz insertion loss

[1] Recommended EVB schematic/layout/BOM/PCB should be followed in order to achieve specified performance.

PARAMETER	CONDITIONS[1]	MIN.	TYP.	MAX.	UNITS
VSWR					
RF1, RF2, RF3, RF4, RFCOM	600 MHz to 960 MHz		1.15		:1
RF1, RF2, RF3, RF4, RFCOM	1700 MHz to 2700 MHz		1.3		:1
RF1, RF2, RF3, RF4, RFCOM	3300 MHz to 4200 MHz		1.45		:1
RF1, RF2, RF3, RF4, RFCOM	4400 MHz to 5000 MHz		2.0		:1
RF1, RF2, RF3, RF4, RFCOM	5000 MHz to 6000 MHz		2.8		:1
RF1, RF2, RF3, RF4, RFCOM*	5000 MHz to 6000 MHz		1.6		:1

* See tuning schematic for 5000MHz to 6000MHz insertion loss
[1] Recommended EVB schematic/layout/BOM/PCB should be followed in order to achieve specified performance.

Isolation Matrix

Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, Input and Output = 50Ω, T = 25°C, V_{IO} = 1.8V, SDATA/SCLK = 1.8 V / 0 V

SW STATE	INSERTION PORT	ISOLATION 617 – 960MHZ, TYPICAL (DB)			
		RF1	RF2	RF3	RF4
RF1	RF1		53	45	46
RF2	RF2	54.5		45	46
RF3	RF3	39.5	53		52.5
RF4	RF4	53.5	40	51.5	
RF1	RFCOM		47	41	40.5
RF2	RFCOM	46		41	40.5
RF3	RFCOM	46	47		40.5
RF4	RFCOM	46	47	41	

SW STATE	INSERTION PORT	ISOLATION 1710 – 2170MHZ, TYPICAL (DB)			
		RF1	RF2	RF3	RF4
RF1	RF1		38.5	32.5	36
RF2	RF2	38.5		35	33.5
RF3	RF3	30	39		37.5
RF4	RF4	39	30.5	37	
RF1	RFCOM		36	30.5	30.5
RF2	RFCOM	35		30.5	30.5
RF3	RFCOM	35	36		30.5
RF4	RFCOM	35	36	30.5	

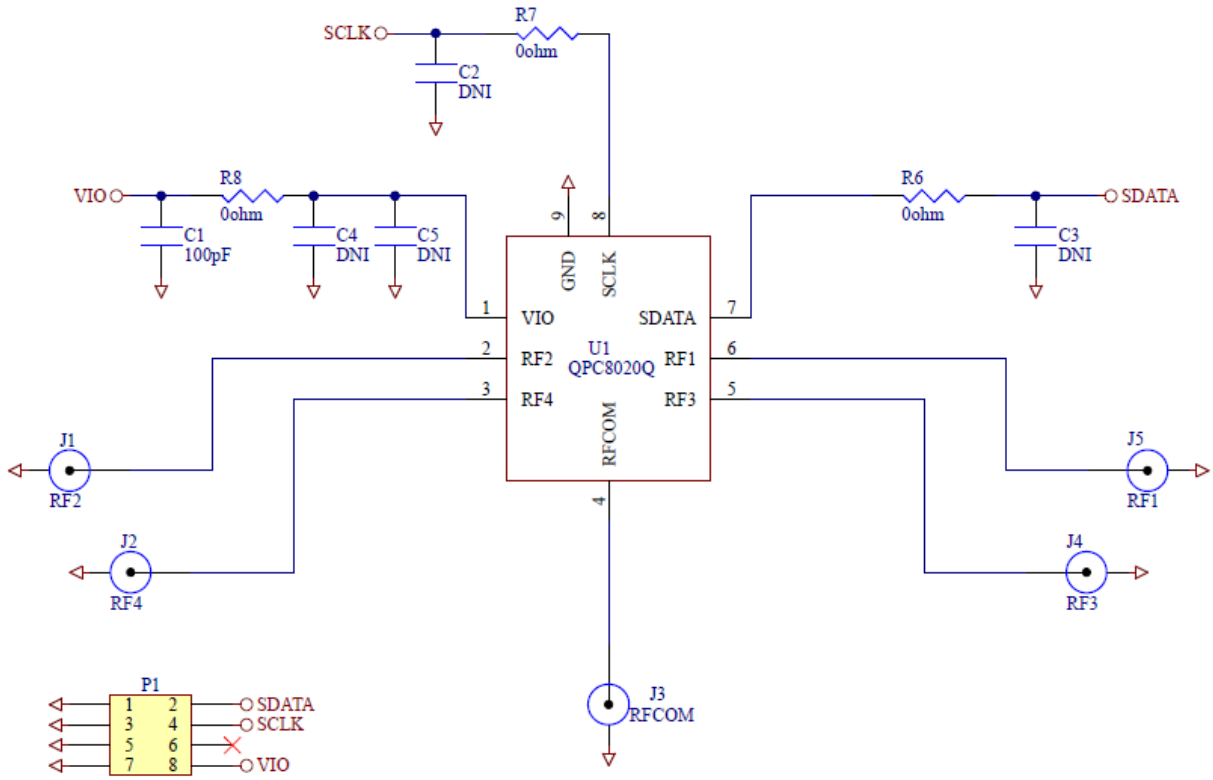
SW STATE	INSERTION PORT	ISOLATION 2300 – 2700MHZ, TYPICAL (DB)			
		RF1	RF2	RF3	RF4
RF1	RF1		35	29	33
RF2	RF2	34.5		32	29.5
RF3	RF3	27	35		33.5
RF4	RF4	34.5	28	33	
RF1	RFCOM		32.5	27	27
RF2	RFCOM	31.5		27	27
RF3	RFCOM	31.5	32.5		27
RF4	RFCOM	31.5	32.5	27	

SW STATE	INSERTION PORT	ISOLATION 3300 – 4200MHZ, TYPICAL (DB)			
		RF1	RF2	RF3	RF4
RF1	RF1		27.5	22	26.5
RF2	RF2	27		26	22.5
RF3	RF3	22	28		26
RF4	RF4	27.5	22.5	25.5	
RF1	RFCOM		26.5	21.5	22
RF2	RFCOM	26		21.5	22
RF3	RFCOM	26	26.5		22
RF4	RFCOM	26	26.5	21.5	

SW STATE	INSERTION PORT	ISOLATION 4400 – 5000MHZ, TYPICAL (DB)			
		RF1	RF2	RF3	RF4
RF1	RF1		24	18	23.5
RF2	RF2	24		23.5	19
RF3	RF3	19	24		22
RF4	RF4	23.5	19.5	22	
RF1	RFCOM		23	18.5	19
RF2	RFCOM	23		18.5	19
RF3	RFCOM	23	23		19
RF4	RFCOM	23	23	18.5	

SW STATE	INSERTION PORT	ISOLATION 5000 – 6000MHZ, TYPICAL (DB)			
		RF1	RF2	RF3	RF4
RF1	RF1		22	16	21.5
RF2	RF2	21.5		21.5	16.5
RF3	RF3	16.5	21.5		19.5
RF4	RF4	21.5	17	19.5	
RF1	RFCOM		21.5	16.5	16.5
RF2	RFCOM	21		16.5	16.5
RF3	RFCOM	21	21.5		16.5
RF4	RFCOM	21	21.5	16.5	

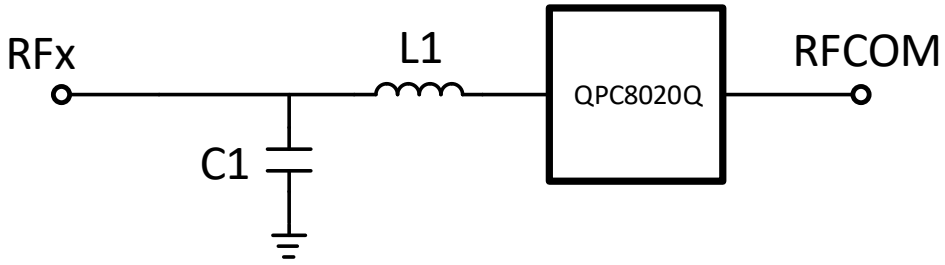
Application Circuit Schematic



Application Circuit BOM

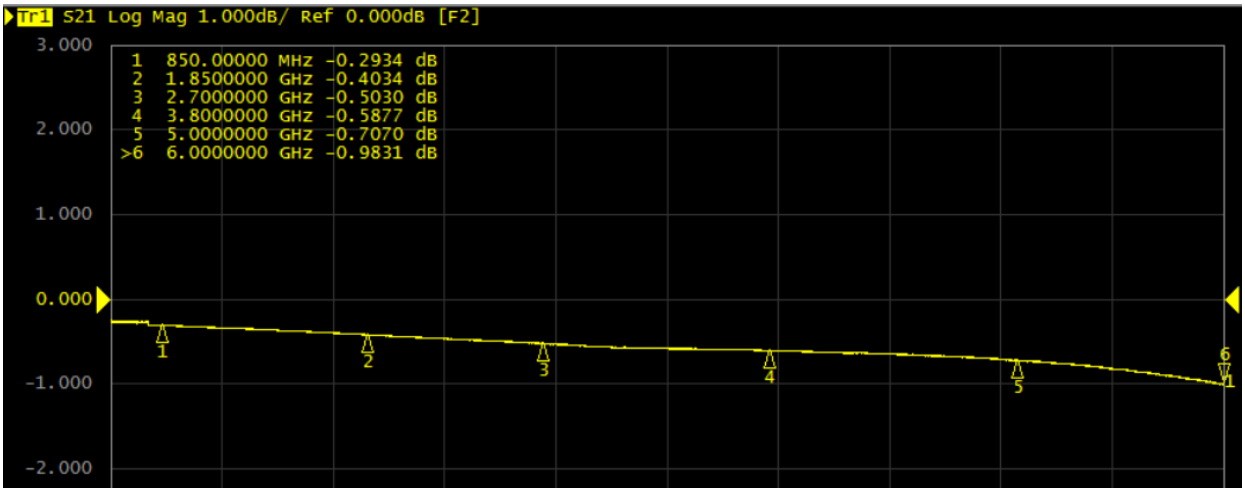
Material#	Rev	Qty	Ref Des	Description
QPC8020SB	A	1	DUT	Automotive RFFE GSM SP4T Switch
293481		1	PCB	PCB, QPC8020Q
21239		1	C1	CAP, 100pF, 5%, 25V, C0G, 0201
21253		3	R6,R7,R8	RES, 0 OHM, 5%, 1/20W, 0201
262452		5	RF1,RF2,RF3,RF4,RFCOM	CONN, SMA, EL MINI FLT 0.068" SPE-000303
274947	A	1	P1	CONN, HDR, SHRD, RT-ANG, 2x4, 0.100"
4XXX1		4	C2*,C3*,C4*,C5*	NOT POPULATED ITEM-1

Tuning Schematic for 5000MHz – 6000MHz

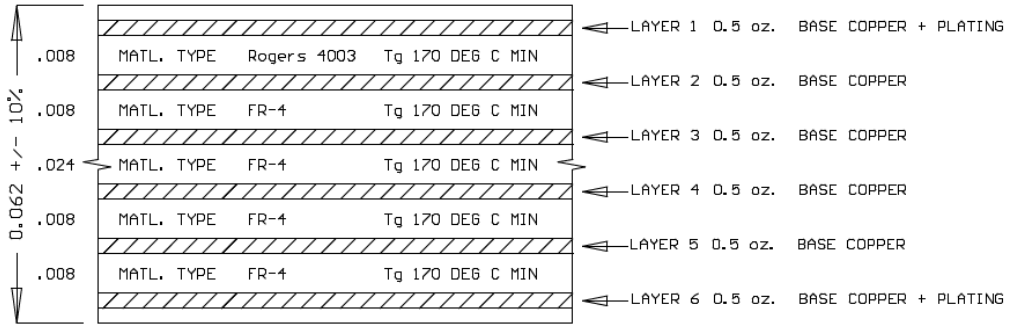


NAME	VALUE	PACKAGE	DESCRIPTION
C1	0.4pF	0201	Matching for optimized RF performance*
L1	1.3nH	0201	Matching for optimized RF performance*

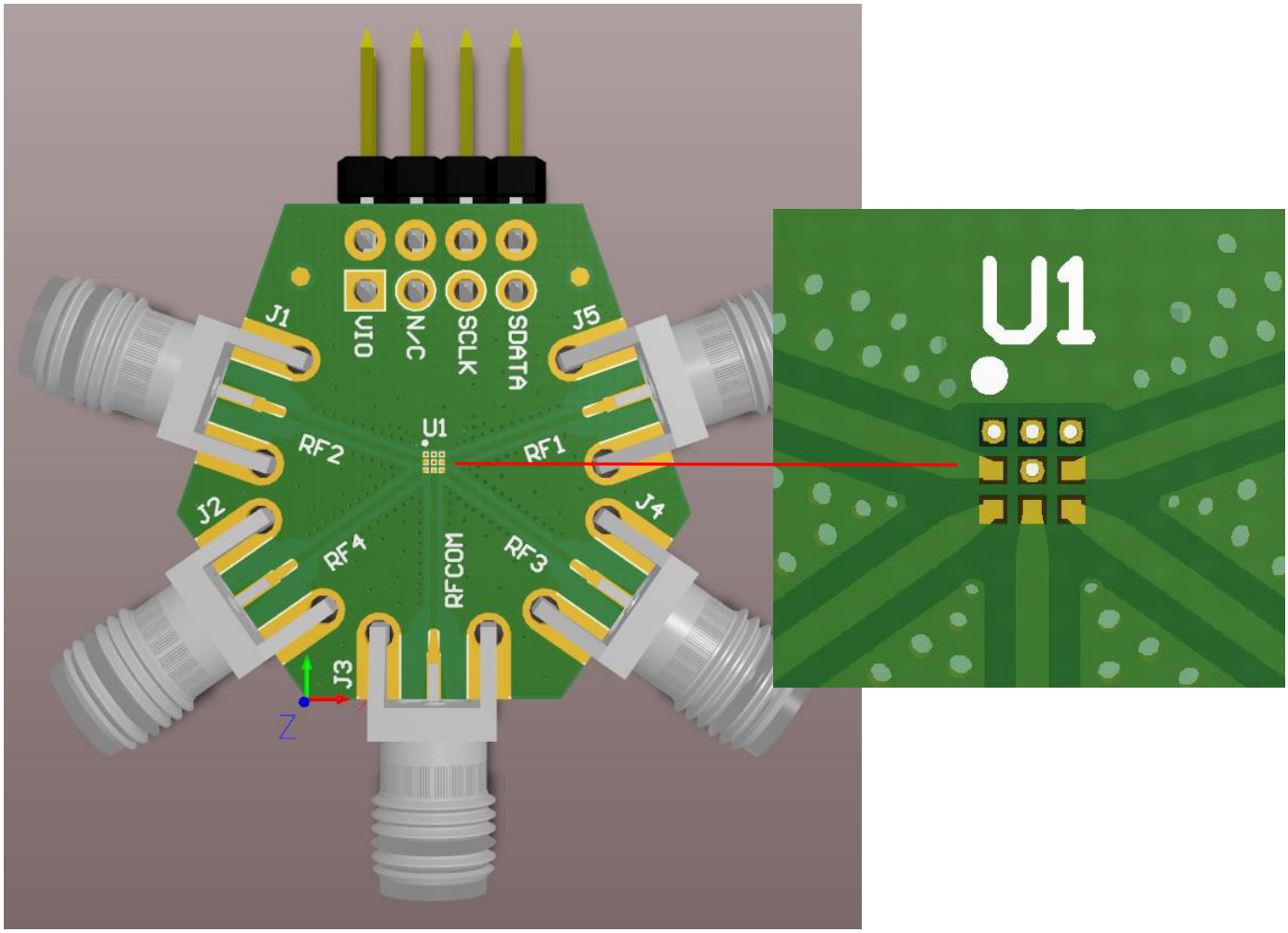
*** Matching elements are subject to change based on specific system application**



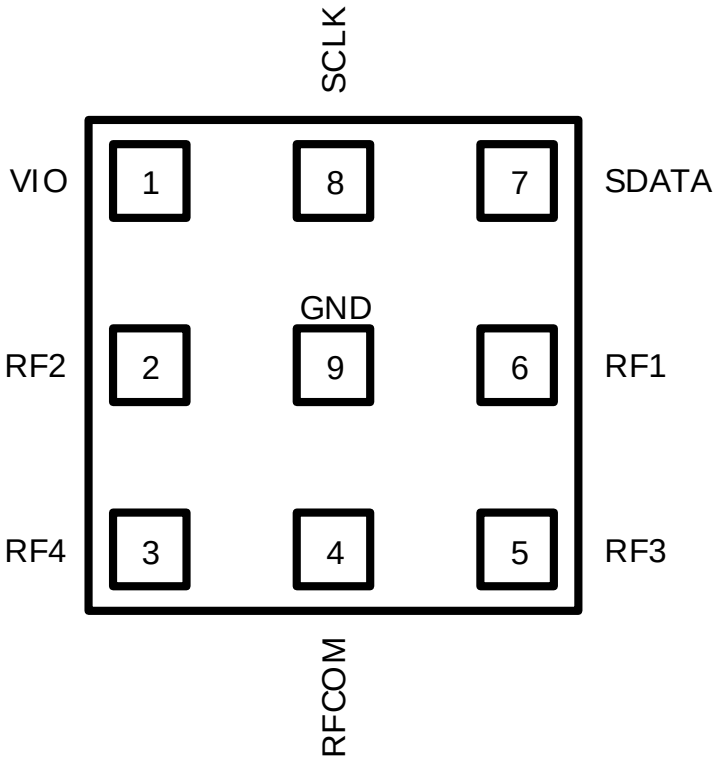
Evaluation Board PCB Information



Evaluation Board



Pin Configuration and Description



Top View

PIN NO.	LABEL	DESCRIPTION
1	VIO	Voltage Supply
2	RF2	RF port
3	RF4	RF port
4	RFCOM	RF common port
5	RF3	RF port
6	RF1	RF port
7	SDATA	RFFE Data Signal
8	SCLK	RFFE Clock Signal
9	GND	Ground

RFFE Register Map

Register 0x0000 – SW_CTRL0

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	SPARE	Reserved for future use	0x0	No	0 - 2	R/W
3:0	SW_CTRL	0x00: Isolation 0x01: RF1 - RFC 0x02: RF2 - RFC 0x04: RF3 - RFC 0x08: RF4 - RFC	0x00	No	0-2	R/W

Register 0x0001 – SPARE

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	SPARE	Reserved for future use	0x00	No	0 - 2	R/W

Register 0x001A – RFFE_STATUS

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	No	No	W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x001B – GSID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x001C – PM_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W

7:6	PWR_MODE[1:0]	00: ACTIVE - Normal Operation 01: STARTUP - Reset all registers to default settings 10: ACTIVE - Low Power - Antenna in isolation 11: STARTUP - Reset all registers to default settings *Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.*	0b10	B/G	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register.* *If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0b000	No	No	R/W
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.*	0b000	B/G	No	W

Register 0x001D — PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[7:0]	Lower eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x17	No	No	R

Register 0x001E — MANUFACTURER_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	MFG_ID[7:0]	Lower eight bits of MIPI Manufacturer ID *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x34	No	No	R

Register 0x001F — MAN_USID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	RESERVED	Reserved for future use	0b00	No	No	R

5:4	MFG_ID[9:8]	Upper two bits of MIPI Manufacturer ID *Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.*	0b01	No	No	R
3:0	USID[3:0]	Programmable Unique Slave ID *Note: USID is only writeable using a special programming sequence. See MIPI 6.6.2 for details.*	0x8	No	No	R/W

Register 0x0021 — REVISION_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	MAJOR_REV[1:0]	Major Revisions - all layer	0b00	No	No	R
5:4	MINOR_REV[1:0]	Minor Revisions - metal only	0b00	No	No	R
3:0	MISC_REV[3:0]	Misc Revisions - mask variants	0b0001	No	No	R
		Note: The REVISION_ID register contains this product's revision number which is set by Qorvo according to manufacture date. The value may change throughout the product life cycle.				

Power On and Off Sequence

It is very important that the user adheres to the correct timing sequences in order to avoid damaging the device. Figures are NOT drawn to scale.

1. Once VIO is powered down to 0V, wait a minimum of 10 µs to reapply power to VIO. (see figure 1)

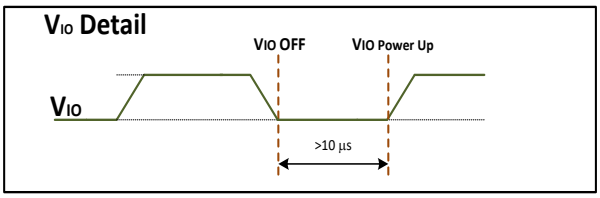


Figure 1 Digital Supply Detail

2. VIO must be applied for a minimum of 120 ns before sending SDATA/SCLK to ensure correct data transmission. (see figure 2)
3. VIO must be applied for a minimum of 15 µs before applying RF power. (see figure 2)
4. Wait a minimum of 2.7 µs after RFFE bus is idle to apply an RF signal. (see figure 2)

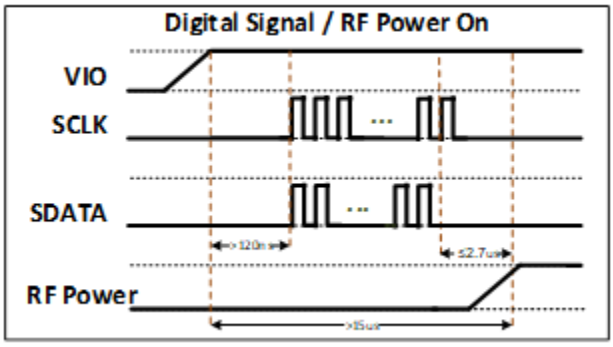


Figure 2 Digital Signal / RF Power-On Detail

5. RF power must not be applied during switching events. To ensure this, remove RF power before completing a register write that will change the switch mode. (see figure 3)

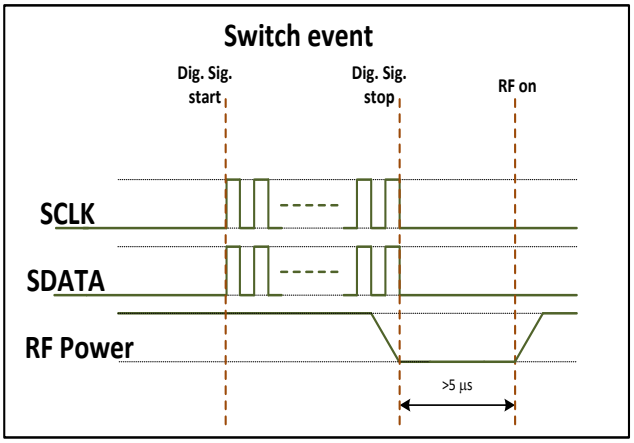


Figure 3 Switch Event Timing

6. If “Low Power Mode” is utilized, there must be a delay of 10 μs before exiting “Low Power Mode”. (see figure 4)

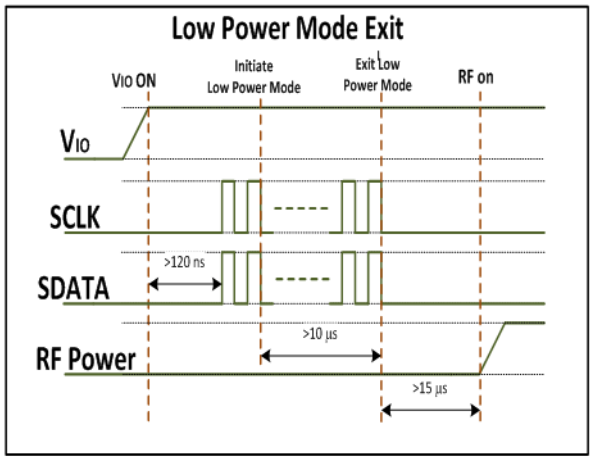


Figure 4 Low Power Mode Exit Timing

Tape and Reel Information

Table 1. Tape and Reel

Qorvo Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units Per Reel
QPC8020QTR13-5K	13 (330)	4 (102)	8	4	Single	5000
QPC8020QSR	7 (178)	2.5 (63)	8	4	Single	100

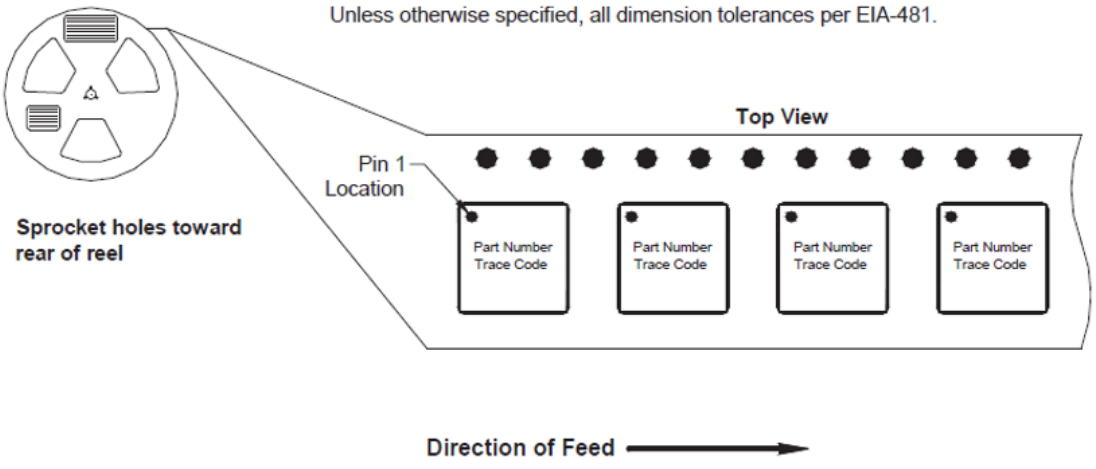
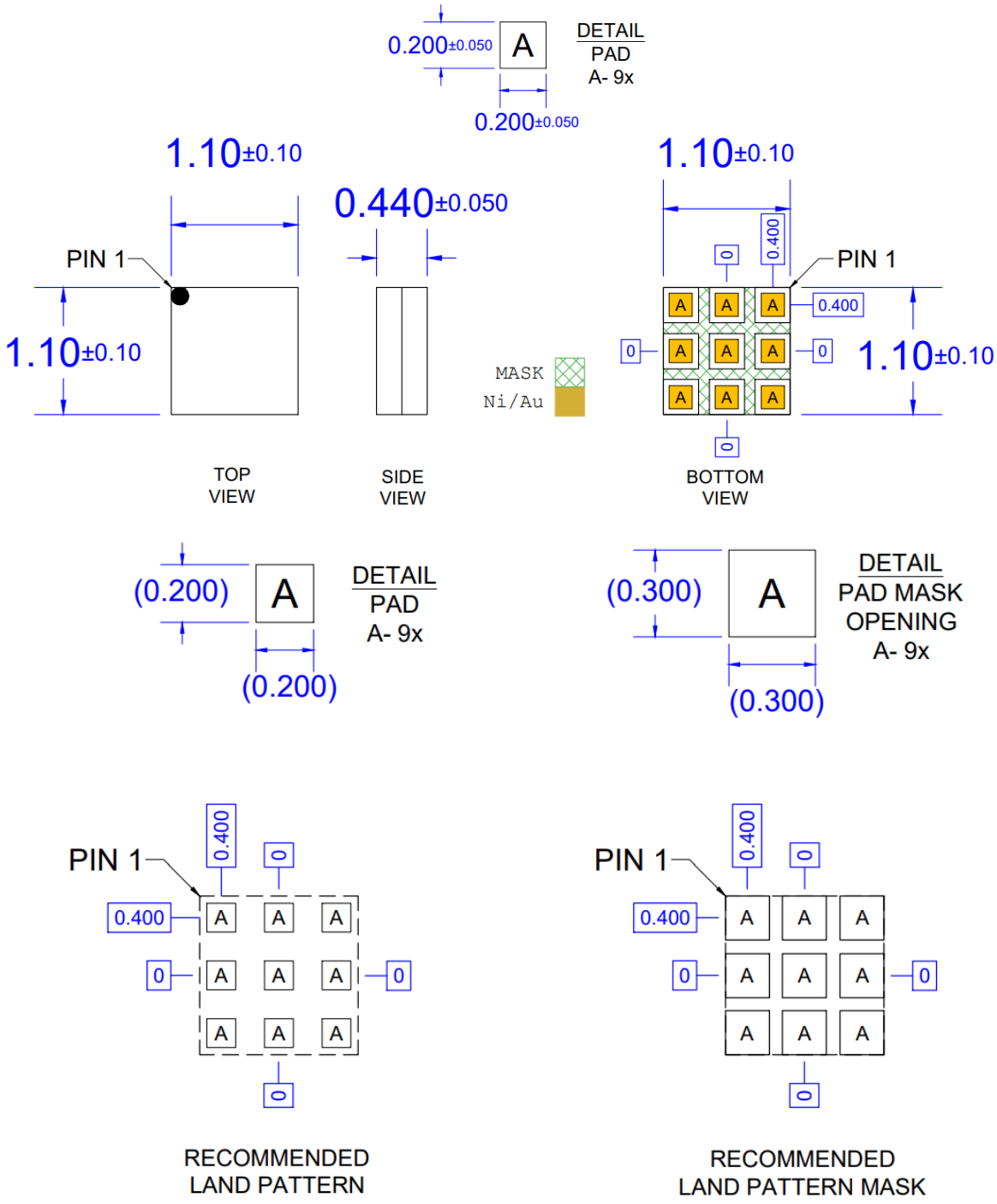


Figure 1. 1.10 mm x 1.10 mm (Carrier Tape Drawing with Part Orientation).

Mechanical Information

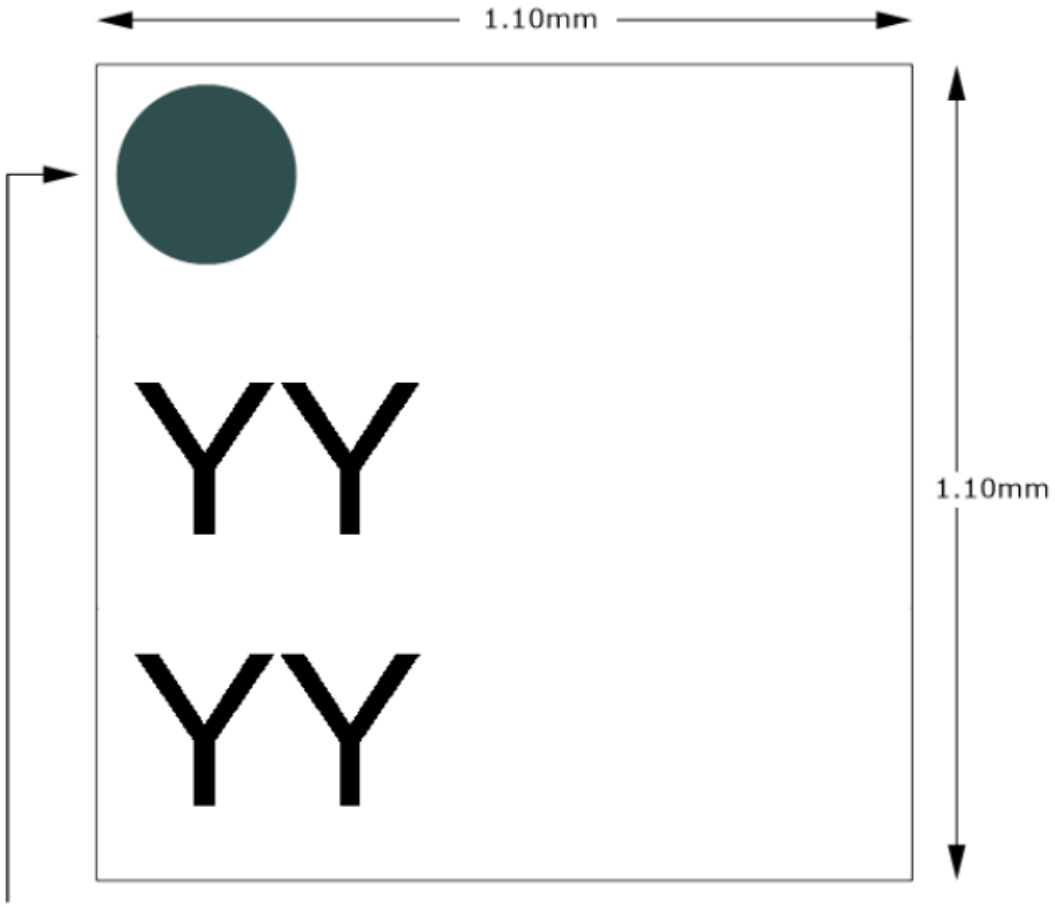
Package Drawing



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Branding Diagram



Pin 1 Indicator
Trace Code to be assigned by SubCon
(where YYYY indicates the Trace Code)

Handling Precautions

PARAMETER	RATING	STANDARD
ESD – Human Body Model (HBM)	Class 1C (1000V)	ANSI/ESDA/JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C3 (1000V)	ANSI/ESDA/JEDEC JS-002
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: ENEPIG

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free
- PFOS Free

Revision History

Revision	Comments
Rev 1	Initial Release
Rev 1.1	Updated format for Automotive
NOV19,19	Updated Max specs
Dec2,19	Updated typical specs from testing and 6GHz matching circuit with plot
Dec 11, 2019	Removed Preliminary and made various formatting changes.
JAN15,2020	Updated for 8020Q
JAN24,2020	Updated for EVB info
MAR17, 2020	Added more insertion loss specs for matching
MAY5, 2020	Release Rev B; update from RVTM CHAR data
MAY11, 20	Updated marking diagram
JAN6, 2021	Added B7 harmonic,
June3, 2021	Release Rev C: updated orderable part for TR13, added PFOS Free, updated plating
JUN28, 2021	Release Rev D: update Min/Max Specs from Production Runs
OCT24, 2024	REV E, added Max Junction Temperature in AMR

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