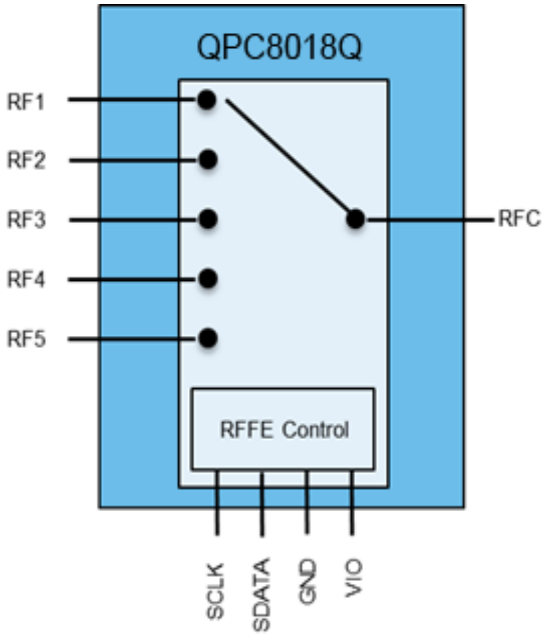
QPC8018Q

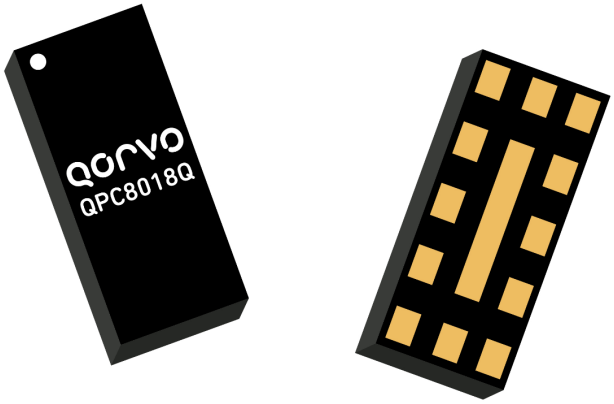
SP5T Switch For LTE Applications

Product Description

The QPC8018Q is a low loss, high isolation SP5T switch with performance optimized for LTE and diversity applications. The QPC8018Q is packaged in an ultra compact 1.1mm x 1.9mm x 0.44mm, 13-pin, Module package which allows for the smallest solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

Functional Block Diagram





13 Pin 1.1 x 1.9 x 0.44 mm Module Package

Feature Overview

- Qualified to AEC-Q100 Grade 3
- Excellent insertion loss and isolation performance
  - 0.32dB Typ IL, Band 5
  - 48dB Typ Isolation, Band 5
- Multi-Band operation from 600MHz to 6000MHz
- RFFE 2.0 compatible
- DC blocking capacitors are not required in typical applications

Applications

- Automotive Telematics Modules
- LTE and Diversity Applications

Ordering Information

PART NO.	DESCRIPTION
QPC8018QSB	5-pc Sample Bag
QPC8018QSR	100-pc, 7” Reel
QPC8018QTR13	10000-pc, 13” Reel
QPC8018QDK	Design Kit
QPC8018QPCK	Fully Assembled EVB and 5-pc Sample Bag

Absolute Maximum Ratings

PARAMETER	RATING
Storage Temperature	-45 to +125 °C
V_{IO}	2.5 V
SDATA, SCLK	2.5 V
Maximum Input Power (Electrical Limitation)	37 dBm, 100% Duty Cycle, CW tone, 1:1 VSWR. +85°C 34 dBm, 100% Duty Cycle, CW tone, 3:1 VSWR, +85°C
Maximum Input Power (Thermal Limitation)	35 dBm, 100% Duty Cycle, CW tone, 1:1 VSWR. +85°C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

PARAMETER	MIN.	TYP.	MAX.	UNITS
Operating Ambient Temperature [1]	-40	+25	+85	˚C
V_{IO} Supply Voltage	1.65	1.8	1.95	V
V_{IO} Supply Current (Active Mode)		27	35	µA
V_{IO} Supply Current (Low Power Mode)		0.4	6	µA
SDATA, SCLK Logic Low (Input)	0.00	0.00	0.3 x VIO	V
SDATA, SCLK Logic High (Input)	0.7 x VIO	1.8	VIO	V
SDATA Logic Low (Output)	0.00	0.00	0.2 x VIO	V
SDATA Logic High (Output)	0.8 x VIO	1.8	VIO	V
SDATA, SCLK Logic High Current		0.1	5	µA
Turn-On Time			20	µs
Switching Speed		3.2		µs
Junction Temperature			125	˚C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

[1] Case Temperature allows 10˚C max rise over Ambient.

Electrical Specifications(1)

Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, Input and Output = 50Ω, T = 25°C, V_{IO} = 1.8V

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Insertion Loss					
RFx to RFC	617MHz to 960MHz		0.32	0.5	dB
RFx to RFC	1710MHz to 2170MHz		0.45	0.65	dB
RFx to RFC	2300MHz to 2690MHz		0.54	0.8	dB
RFx to RFC	3300MHz to 4200MHz		1.05		dB
RFx to RFC	4400MHz to 5000MHz		1.25		dB
RFx to RFC	5100MHz to 6000MHz		1.33		dB
RFx to RFC*	5100MHz to 6000MHz		0.90		dB
Isolation					
RFx to RFx	See Isolation Matrix				
RFx to RFC	617MHz to 960MHz	34.5	48		dB
RFx to RFC	1710MHz to 2170MHz	29.5	37		dB
RFx to RFC	2300MHz to 2690MHz	27.5	33		dB
RFx to RFC	3300MHz to 4200MHz		28		dB
RFx to RFC	4400MHz to 5000MHz		25		dB
RFx to RFC	5100MHz to 6000MHz		23		dB
Harmonics					
Low Band, 2fo	Pin = +26dBm, 50Ω, f_0= 824MHz		-78	-70	dBm
Low Band, 3fo	Pin = +26dBm, 50Ω, f_0= 824MHz		-69	-60	dBm
Mid Band, 2fo	Pin = +26dBm, 50Ω, f_0= 1980MHz		-73	-57	dBm
Mid Band, 3fo	Pin = +26dBm, 50Ω, f_0= 1980MHz		-67	-60	dBm
High Band, 2fo	Pin = +26dBm, 50Ω, f_0= 2570MHz		-74	-65	dBm
High Band, 3fo	Pin = +26dBm, 50Ω, f_0= 2570MHz		-68	-65	dBm
IMD2					
Low Band	TX Carrier @ 897.5MHz at +21dBm CW Blocker @ 1840 MHz at -15dBm Measured RX frequency @ 942.5MHz		-116		dBm
High Band	TX Carrier @ 1880MHz at +21dBm CW Blocker @ 3840 MHz at -15dBm Measured RX frequency @ 1960MHz		-116		dBm
IMD3					
Low Band	TX Carrier @ 897.5MHz at +21dBm CW Blocker @ 852.5MHz at -15dBm Measured RX frequency @ 942.5MHz		-113		dBm
High Band	TX Carrier @ 1880MHz at +21dBm CW Blocker @ 1800MHz at -15dBm Measured RX frequency @ 1960MHz		-118		dBm

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VSWR					
	617 MHz to 960 MHz		1.06		:1
	1710 MHz to 2170 MHz		1.24		:1
	2300 MHz to 2690 MHz		1.44		:1
	3300 MHz to 4200 MHz		2.08		:1
	4400 MHz to 5000 MHz		2.24		:1
	5100 MHz to 6000 MHz		2.22		:1

* See tuning schematic for 5000MHz to 6000MHz insertion loss
[1)] Recommended EVB schematic / layout / BOM / PCB should be followed in order to achieve specified performance.

Isolation Matrix Low Band (617MHz – 960MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)				
		RF1	RF2	RF3	RF4	RF5
RF1	RF1		45	36	53	46
RF2	RF2	45		54	36	54
RF3	RF3	35	50		55	37
RF4	RF4	50	35	55		54
RF5	RF5	43	52	36	54	
RF1	RFC		53	39	52	51
RF2	RFC	53		52	39	44
RF3	RFC	39	55		51	42
RF4	RFC	55	38	51		44
RF5	RFC	49	54	40	52	

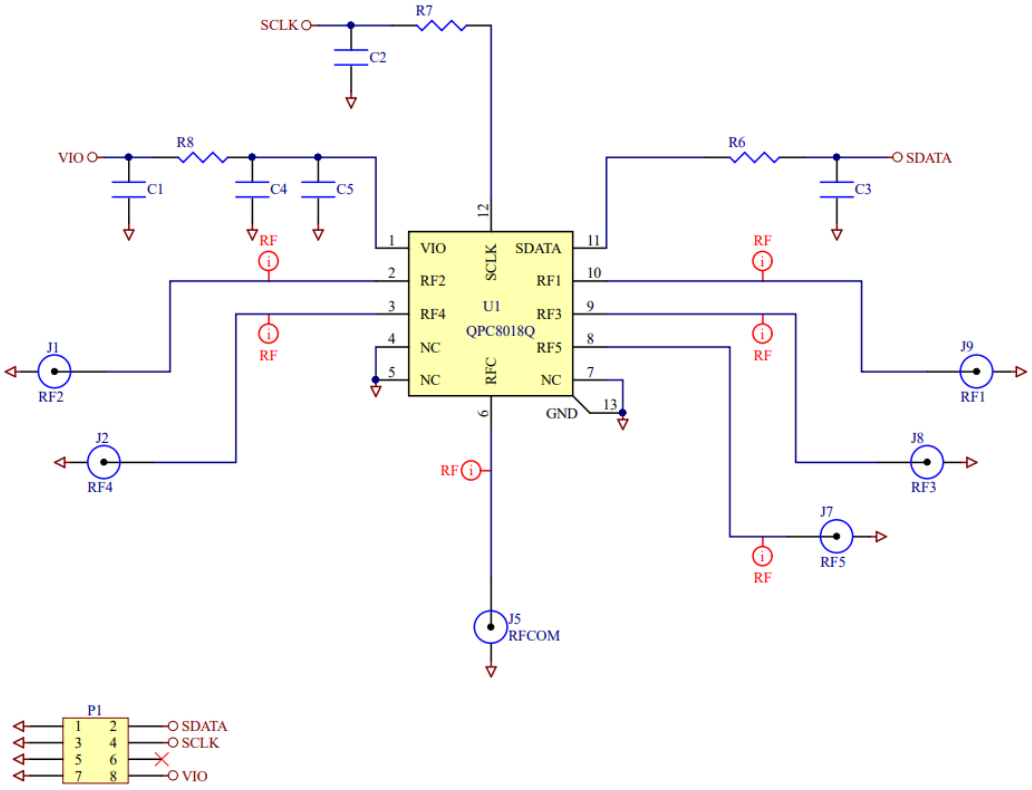
Isolation Matrix Mid Band (1710MHz – 2170MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)				
		RF1	RF2	RF3	RF4	RF5
RF1	RF1		36	28	42	36
RF2	RF2	36		42	28	43
RF3	RF3	27	40		43	28
RF4	RF4	39	27	42		42
RF5	RF5	34	41	28	42	
RF1	RFC		40	31	40	37
RF2	RFC	41		40	31	35
RF3	RFC	31	41		39	32
RF4	RFC	41	31	40		35
RF5	RFC	38	41	32	40	

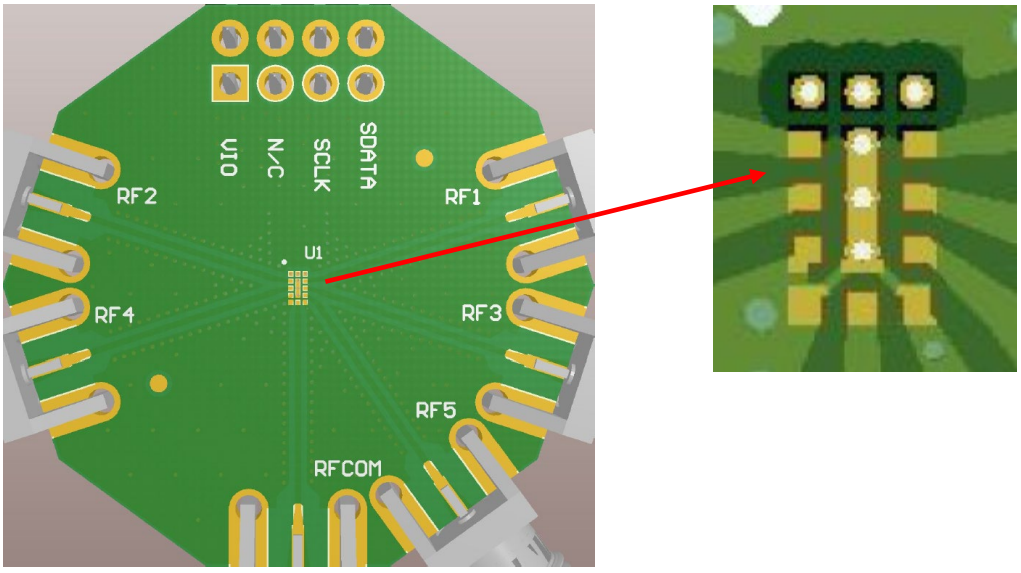
Isolation Matrix High Band (2300MHz – 2690MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)				
		RF1	RF2	RF3	RF4	RF5
RF1	RF1		34	25	38	33
RF2	RF2	33		38	25	39
RF3	RF3	24	36		39	25
RF4	RF4	36	24	38		38
RF5	RF5	31	37	25	38	
RF1	RFC		36	29	35	32
RF2	RFC	37		36	29	32
RF3	RFC	28	37		36	29
RF4	RFC	37	28	36		32
RF5	RFC	34	37	29	36	

Application Circuit Schematic

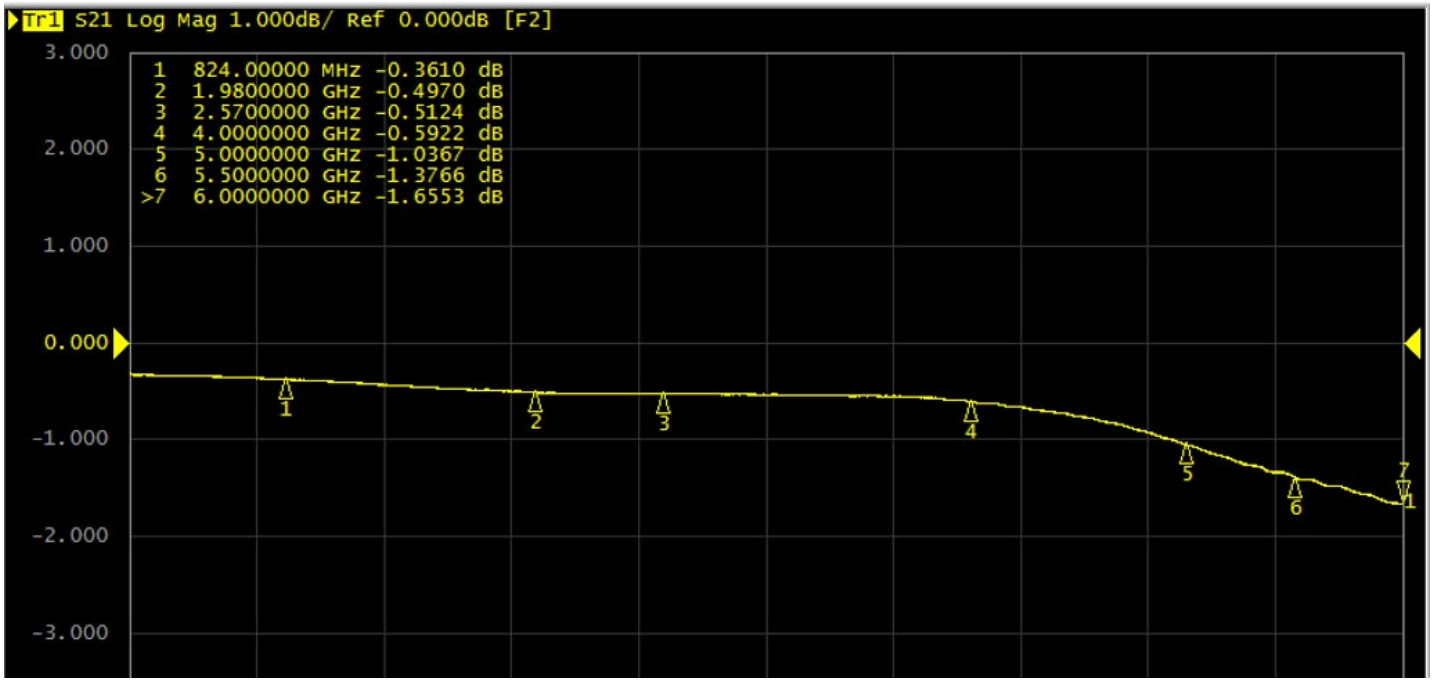


Evaluation Board PCB



Evaluation Board

Qty	Ref Des	Description	Mfg Part #	Mfg Name
1	PCB	PCB, QPC8018Q	QPC8018Q-4000(A)	Performance Micro International Pte
1	C4	CAP, 100pF, 5%, 25V, C0G, 0201	GRM0335C1E101JA01D	MURATA ELECTRONICS SINGAPORE PTE LT
3	R6,R7,R8	RES, 0 OHM, 5%, 1/20W, 0201	RMC1/20JPPA15	Kamaya, Inc
1	U1	P2P RFFE SP5T		
6	RF1,RF2,RF3,RF4,RF5,RFCOM	CONN, SMA, EL MINI FLT 0.068" SPE-000303	20-001CF-T	Aliner Industries, Inc.
1	P1	CONN, HDR, SHRD, RT-ANG, 2x4, 0.100"	75867-132LF	FCI Electronics
4	C1,C2,C3,C5	NOT POPULATED ITEM-1	DUMMY PART	

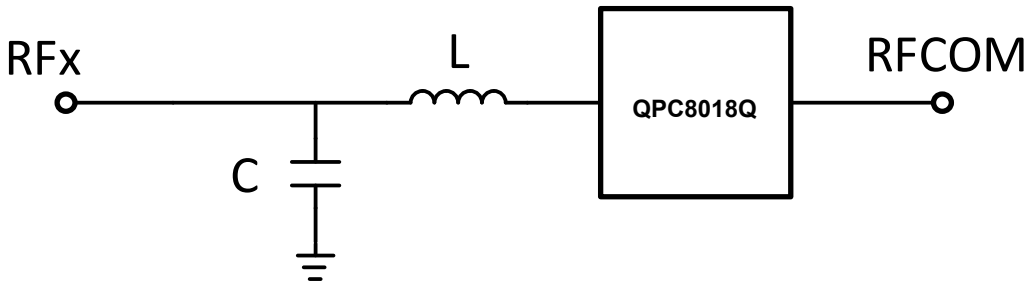


Evaluation Board PCB Information

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1	Copper	0.70mil		
4	Dielectric1	Rogers 4003	8.00mil	3.55	
5	L2	Copper	0.70mil		
6	Dielectric 3	FR4	8.00mil	4.2	
7	L3	Copper	0.70mil		
8	Dielectric 4	FR4	24.00mil	4.2	
9	L4	Copper	0.70mil		
10	Dielectric 5	FR4	8.00mil	4.2	
11	L5	Copper	0.70mil		
12	Dielectric 2	FR4	8.00mil	4.2	
13	L6	Copper	0.70mil		
14	Bottom Solder	Solder Resist	0.40mil	3.5	
15	Bottom Overlay				

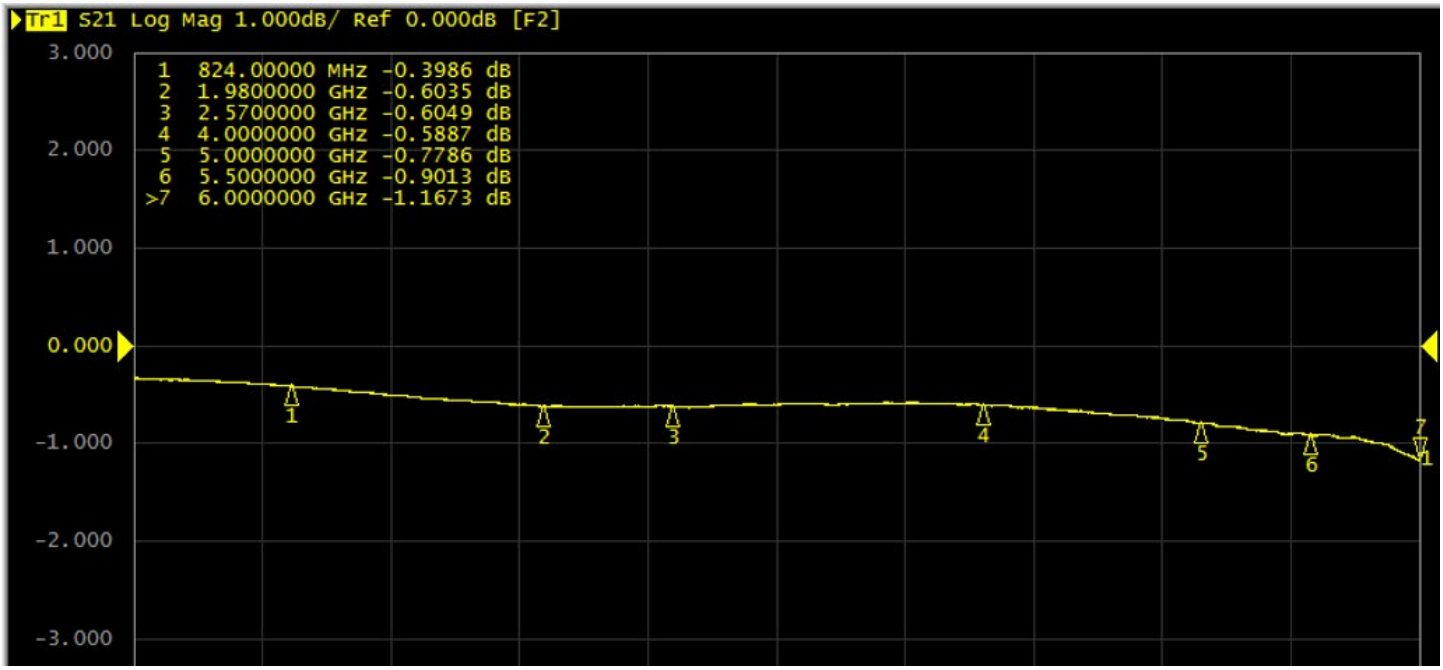
Total Thickness: 62mil +/-10%

Tuning Schematic for 5000MHz – 6000MHz

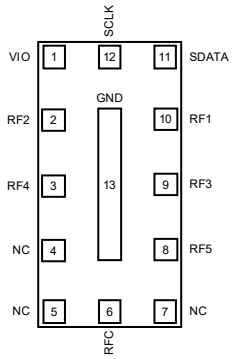


NAME	VALUE	PACKAGE	DESCRIPTION
C	0.4pF	0201	Matching for optimized RF performance*
L	1.0nH	0201	Matching for optimized RF performance*

* Matching elements are subject to change based on specific system application



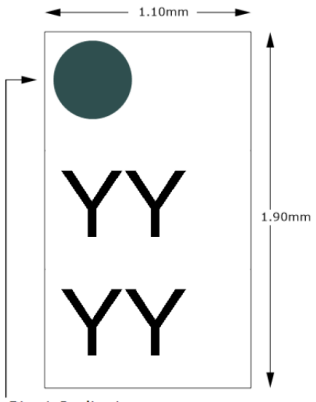
Pin Configuration and Description



Top View

PIN NO.	LABEL	DESCRIPTION
1	VIO	Voltage Supply
2	RF2	RF Port
3	RF4	RF Port
4	NC	No Connect
5	NC	No Connect
6	RFC	RF Common Port
7	NC	No Connect
8	RF5	RF Port
9	RF3	RF Port
10	RF1	RF Port
11	SDATA	RFFE Data Signal
12	SCLK	RFFE Clock Signal
13	GND	Ground

Part Marking



Pin 1 Indicator
Trace Code to be assigned by SubCon
(where YYYY indicates the Trace Code)

RFFE Register Map

Register 0x0000 – SW_CTRL0

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:5	SPARE	Reserved for future use	0x0	No	0 - 2	R/W
4:0	SW_CTRL	0x00: Isolation 0x01: RF1 - RFC 0x02: RF2 - RFC 0x04: RF3 - RFC 0x08: RF4 - RFC 0x10: RF5 - RFC	0x00	No	0 - 2	R/W

Register 0x0001 – SPARE

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	SPARE	Reserved for future use	0x00	No	0 - 2	R/W

Register 0x001C – PM_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	PWR_MODE[1:0]	00: ACTIVE - Normal Operation 01: STARTUP - Reset all registers to default settings 10: ACTIVE - Low Power - Antenna in isolation 11: STARTUP - Reset all registers to default settings *Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.*	0b10	B/G	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register.* *If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0b000	No	No	R/W
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.*	0b000	B/G	No	W

Register 0x001D — PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[7:0]	Lower eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x18	No	No	R

Register 0x001E — MANUFACTURER_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	MFG_ID[7:0]	Lower eight bits of MIPI Manufacturer ID *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x34	No	No	R

Register 0x001F — MAN_USID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	RESERVED	Reserved for future use	0b00	No	No	R
5:4	MFG_ID[9:8]	Upper two bits of MIPI Manufacturer ID *Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.*	0b01	No	No	R
3:0	USID[3:0]	Programmable Unique Slave ID *Note: USID is only writeable using a special programming sequence. See MIPI 6.6.2 for details.*	0x8	No	No	R/W

Register 0x0020 — EXT_PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[15:8]	Upper eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x00	No	No	R

Register 0x0021 — REVISION_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	MAJOR_REV[1:0]	Major Revisions - all layer	0b00	No	No	R

5:4	MINOR_REV[1:0]	Minor Revisions - metal only	0b00	No	No	R
3:0	MISC_REV[3:0]	Misc Revisions - mask variants	0b0001	No	No	R
		Note: The REVISION_ID register contains this product's revision number which is set by Qorvo according to manufacture date. The value may change throughout the product life cycle.				

Register 0x0022 – GSID0-1

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x0023 – UDR_RST

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	No	No	W
6:0	RESERVED		0x00	No	No	R

Register 0x0024 – ERR_SUM

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	SPARE	Reserved for future use	0	No	No	R/W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x002C – TEST_PATT

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TEST_PATT[7:0]	Test Pattern	0xD2	No	No	R

Power On and Off Sequence

It is very important that the user adheres to the correct timing sequences in order to avoid damaging the device. Figures are NOT drawn to scale.

1. Once VIO is powered down to 0V, wait a minimum of 10 µs to reapply power to VIO. (see figure 1)

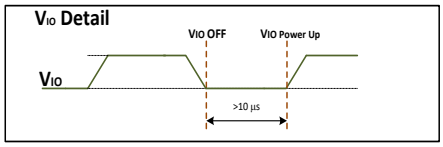


Figure 1 Digital Supply Detail

2. VIO must be applied for a minimum of 120 ns before sending SDATA/SCLK to ensure correct data transmission. (see figure 2)
3. VIO must be applied for a minimum of 15 µs before applying RF power. (see figure 2)
4. Wait a minimum of 5 µs after RFFE bus is idle to apply an RF signal. (see figure 2)

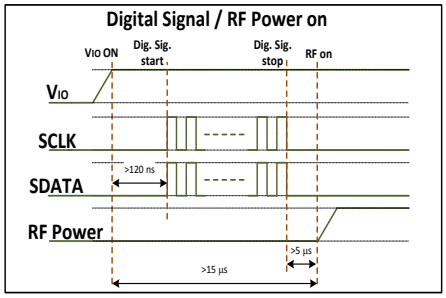


Figure 2 Digtial Signal / RF Power-On Detail

5. RF power must not be applied during switching events. To ensure this, remove RF power before completing a register write that will change the switch mode. (see figure 3)

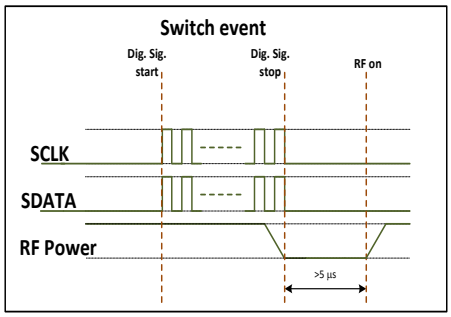


Figure 3 Switch Event Timing

6. If “Low Power Mode” is utilized, there must be a delay of 10 µs before exiting “Low Power Mode”. (see figure 4)

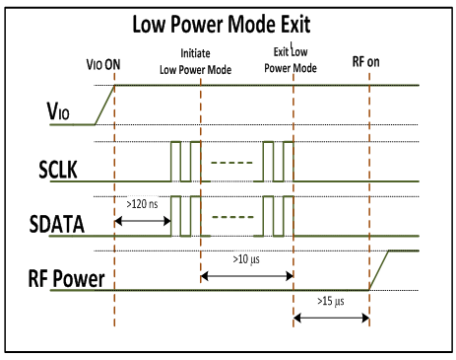
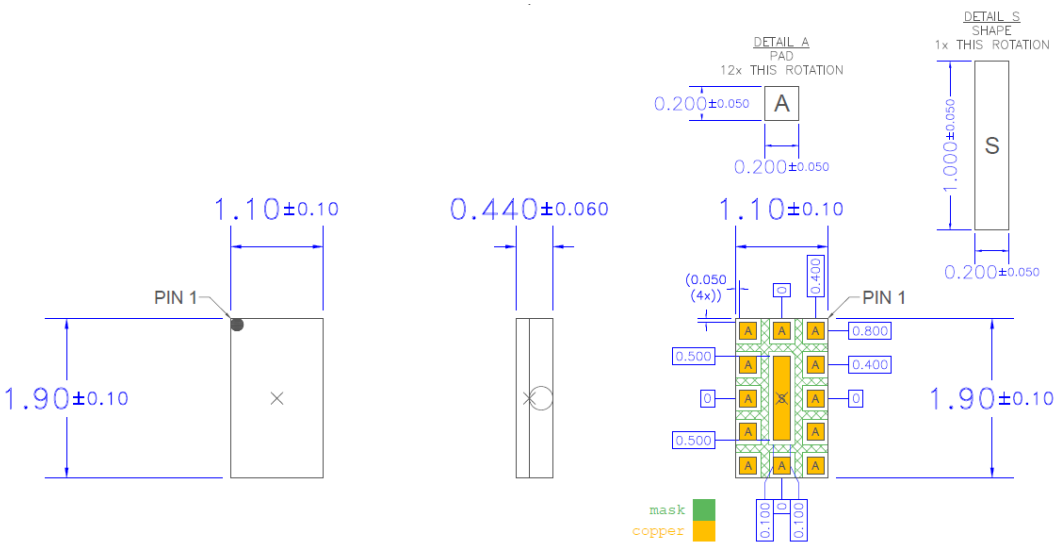
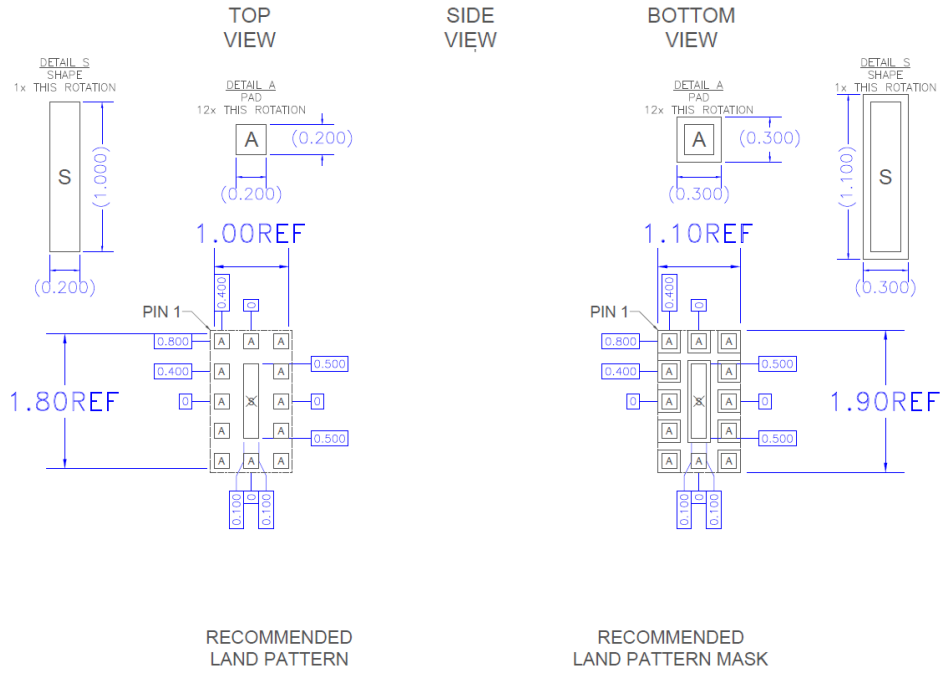


Figure 4 Low Power Mode Exit Timing

Mechanical Information





RECOMMENDED
LAND PATTERN

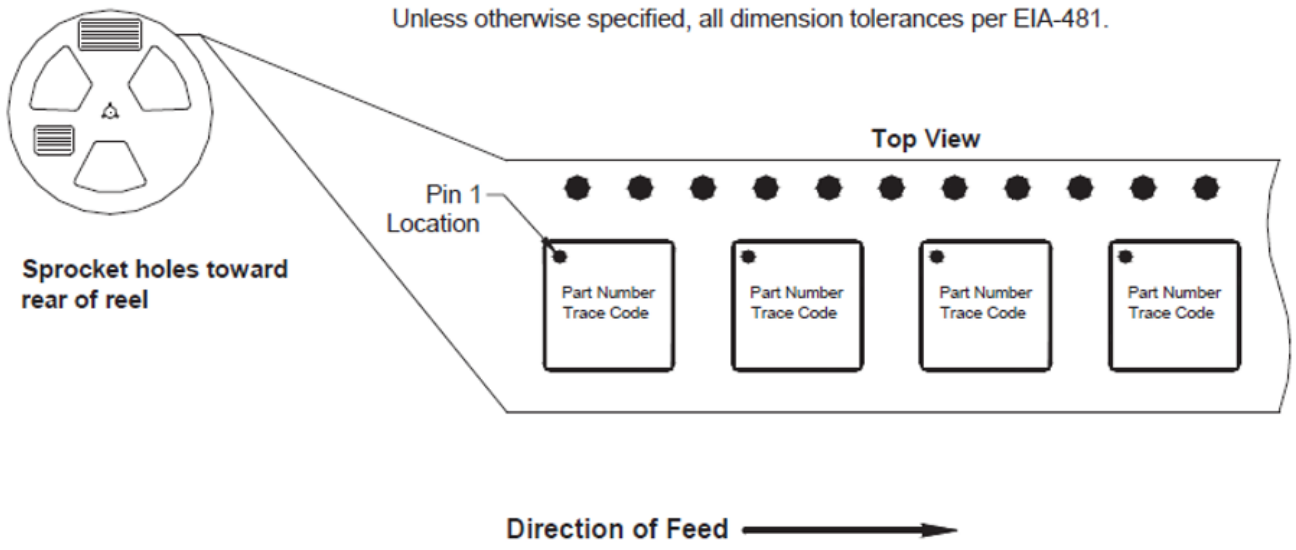
RECOMMENDED
LAND PATTERN MASK

Notes:

1. All dimensions are in milimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Tape and Reel Information

Qorvo Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units Per Reel
QPC8018QTR13	13 (330)	4 (102)	8	4	Single	10000
QPC8018QSR	7 (178)	2.5 (63)	8	4	Single	100



1.10 mm x 1.90 mm (Carrier Tape Drawing with Part Orientation).

Handling Precautions

PARAMETER	RATING	STANDARD
ESD – Human Body Model (HBM)	Class 2 2000V	ESDA/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C3 1000V	ESDA/JEDEC JS-001-2012
MSL – Moisture Senstivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: ENEPIG

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free
- PFOS Free

Revision History

Revision Code	Date	Comments
1.0	10-19-2018	Initial Datasheet Release
1.1	7-26-2019	Correct various datasheet errors
1.2	8/6/19	Update min/max limits and Auto DS updates
1.3	10/15/19	Added TBD for 2.7GHz testing; broke out NR77-79 bands; added Band71
1.4	1/15/20	Updated image, IM2/IM3 specs changed from IP2/IP3; added isolation charts for 4.4 to 6 GHz
A	7/29/20	Updated plating
B	7/29/21	Updated orderable TR13 part number; added PFOS Free; Added ESD ratings; Added EVB BOM; Updated EVB schematic; Added Tj max; Updated AMR specs from RVTM
C	11/11/21	Added min/max specs from PRD and test runs; Added screen shots for S21.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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