



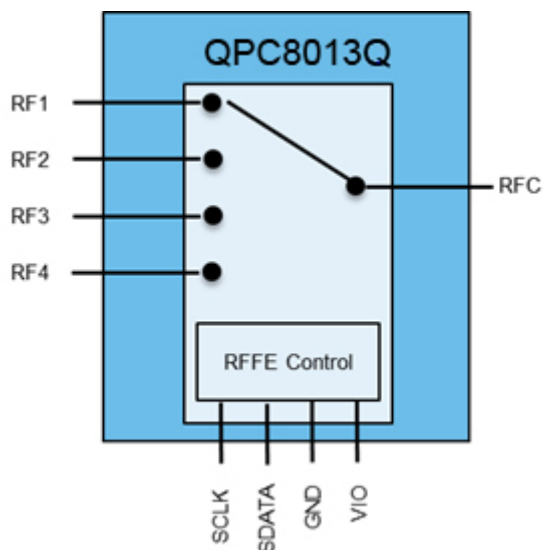
QPC8013Q

SP4T Switch For LTE Applications

Product Description

The QPC8013Q is a low loss, high isolation SP4T switch with performance optimized for LTE and diversity applications. The QPC8013Q is packaged in an ultra compact 1.1mm x 1.9mm x 0.44mm, 13-pin, Module package which allows for the smallest solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

Functional Block Diagram



13 Pin 1.1 x 1.9 x 0.44 mm Module Package

Feature Overview

- Qualified to AEC-Q100 Grade 3
- Excellent insertion loss and isolation performance
 - 0.55dB Typ IL, Band 7
 - 34dB Typ Isolation, Band 7
- Multi-Band operation from 617MHz to 6GHz
- RFFE 2.0 compatible
- Compact 1.1mm x 1.9mm x 0.44mm, Module package
- DC blocking capacitors are not required in typical applications

Applications

- Automotive Telematics Modules
- LTE and Diversity Applications

Ordering Information

| PART NO. | DESCRIPTION |
|--------------|--------------------------------|
| QPC8013QSB | 5-pc Sample Bag |
| QPC8013QSR | 100-pc, 7" Reel |
| QPC8013QTR13 | 10000-pc, 13" Reel |
| QPC8013QDK | Fully Assembled Evaluation Kit |

Absolute Maximum Ratings

| PARAMETER | RATING | CONDITIONS |
|--|----------------|--|
| Storage Temperature | -45 to +125 °C | |
| V _{IO} | 2.5 V | |
| SDATA, SCLK | 2.5 V | |
| Maximum Input Power (Max power point of view) | 37 dBm | 1:1 VSWR, 100% Duty Cycle, CW, +85°C |
| | 34 dBm | 3:1 VSWR, 100% Duty Cycle, CW, +85°C |
| Maximum Input Power (Thermal point of view) | 35 dBm | 1:1 VSWR, 100% Duty Cycle, CW, +85°C (T _J =125°C) |

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

| PARAMETER | MIN. | TYP. | MAX. | UNITS |
|---|-----------------------|------|-----------------------|-------|
| Operating Ambient Temperature ⁽¹⁾ | -40 | +25 | +85 | °C |
| V _{IO} Supply Voltage | 1.65 | 1.8 | 1.95 | V |
| V _{IO} Supply Current (Active Mode) | | 27 | | μA |
| V _{IO} Supply Current (Low Power Mode) | | 0.4 | | μA |
| SDATA, SCLK Logic Low (Input) | 0.00 | 0.00 | 0.3 x V _{IO} | V |
| SDATA, SCLK Logic High (Input) | 0.7 x V _{IO} | 1.8 | V _{IO} | V |
| SDATA Logic Low (Output) | 0.00 | 0.00 | 0.2 x V _{IO} | V |
| SDATA Logic High (Output) | 0.8 x V _{IO} | 1.8 | V _{IO} | V |
| SDATA, SCLK Logic High Current | | 0.1 | 5 | μA |
| Switching Speed (90% of RF) | | 3.5 | 5.5 | μs |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

⁽¹⁾ Case Temperature allows 10°C max rise over Ambient.

Electrical Specifications⁽¹⁾

Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, Input and Output = 50Ω, T = 25°C, V_{IO} = 1.8V

| PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|-----------------------|--|------|------|------|-------|
| Insertion Loss | | | | | |
| RFx to RFC | 617MHz to 960MHz | | 0.35 | 0.48 | dB |
| RFx to RFC | 1710MHz to 2170MHz | | 0.43 | 0.69 | dB |
| RFx to RFC | 2300MHz to 2700MHz | | 0.57 | 0.82 | dB |
| RFx to RFC | 3300MHz to 4200MHz | | 0.75 | | dB |
| RFx to RFC | 4400MHz to 5000MHz | | 0.82 | | dB |
| RFx to RFC | 5100MHz to 6000MHz | | 0.9 | | dB |
| RFx to RFC | 5100MHz to 6000MHz* | | 0.65 | | dB |
| Isolation | | | | | |
| RFx to RFx | Refer to Isolation Matrix | | | | |
| RFx to RFC | 617MHz to 960MHz | 34.5 | 48 | | dB |
| RFx to RFC | 1710MHz to 2170MHz | 27.5 | 37 | | dB |
| RFx to RFC | 2300MHz to 2700MHz | 25 | 34 | | dB |
| RFx to RFC | 3300MHz to 3800MHz | | 29 | | dB |
| RFx to RFC | 4200MHz to 5000MHz | | 26 | | dB |
| RFx to RFC | 5100MHz to 6000MHz | | 24 | | dB |
| Harmonics | | | | | |
| Low Band, 2fo | Pin = +25dBm, 50Ω, fo= 824MHz | | -88 | -74 | dBm |
| Low Band, 3fo | Pin = +25dBm, 50Ω, fo= 824MHz | | -82 | -64 | dBm |
| Mid Band, 2fo | Pin = +25dBm, 50Ω, fo= 1980MHz | | -81 | -65 | dBm |
| Mid Band, 3fo | Pin = +25dBm, 50Ω, fo= 1980MHz | | -80 | -60 | dBm |
| High Band, 2fo | Pin = +25dBm, 50Ω, fo= 2700MHz | | -77 | -68 | dBm |
| IMD2 | | | | | |
| Low Band | TX Carrier @ 897.5MHz at +21dBm CW Blocker @ 1840 MHz at -15dBm Measured RX frequency @ 942.5MHz | | -124 | | dBm |
| High Band | TX Carrier @ 1880MHz at +21dBm CW Blocker @ 3840 MHz at -15dBm Measured RX frequency @ 1960MHz | | -123 | | dBm |
| IMD3 | | | | | |
| Low Band | TX Carrier @ 897.5MHz at +21dBm CW Blocker @ 852.5MHz at -15dBm Measured RX frequency @ 942.5MHz | | -122 | | dBm |
| High Band | TX Carrier @ 1880MHz at +21dBm CW Blocker @ 1800MHz at -15dBm Measured RX frequency @ 1960MHz | | -128 | | dBm |

| PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|-----------|--------------------|------|------|------|-------|
| VSWR | | | | | |
| | 617 MHz to 960 MHz | | 1.19 | | :1 |
| | 1710MHz to 2700MHz | | 1.27 | | :1 |
| | 3300MHz to 4200MHz | | 1.54 | | :1 |
| | 4400MHz to 5000MHz | | 1.68 | | :1 |
| | 5100MHz to 6000MHz | | 1.84 | | :1 |

* See tuning schematic for 5000MHz to 6000MHz insertion loss

⁽¹⁾ Recommended EVB schematic / layout / BOM / PCB should be followed in order to achieve specified performance.

Isolation Matrix Low Band (617MHz – 960MHz)

| STATE | INSERTION PORT | ISOLATION, TYPICAL (dB) | | | |
|-------|----------------|-------------------------|-----|-----|-----|
| | | RF1 | RF2 | RF3 | RF4 |
| RF1 | RF1 | | 45 | 40 | 58 |
| RF2 | RF2 | 46 | | 58 | 40 |
| RF3 | RF3 | 39 | 50 | | 58 |
| RF4 | RF4 | 51 | 39 | 58 | |
| RF1 | RFC | | 55 | 51 | 43 |
| RF2 | RFC | 54 | | 42 | 52 |
| RF3 | RFC | 48 | 49 | | 43 |
| RF4 | RFC | 48 | 48 | 42 | |

Isolation Matrix Mid Band (1710MHz – 2170MHz)

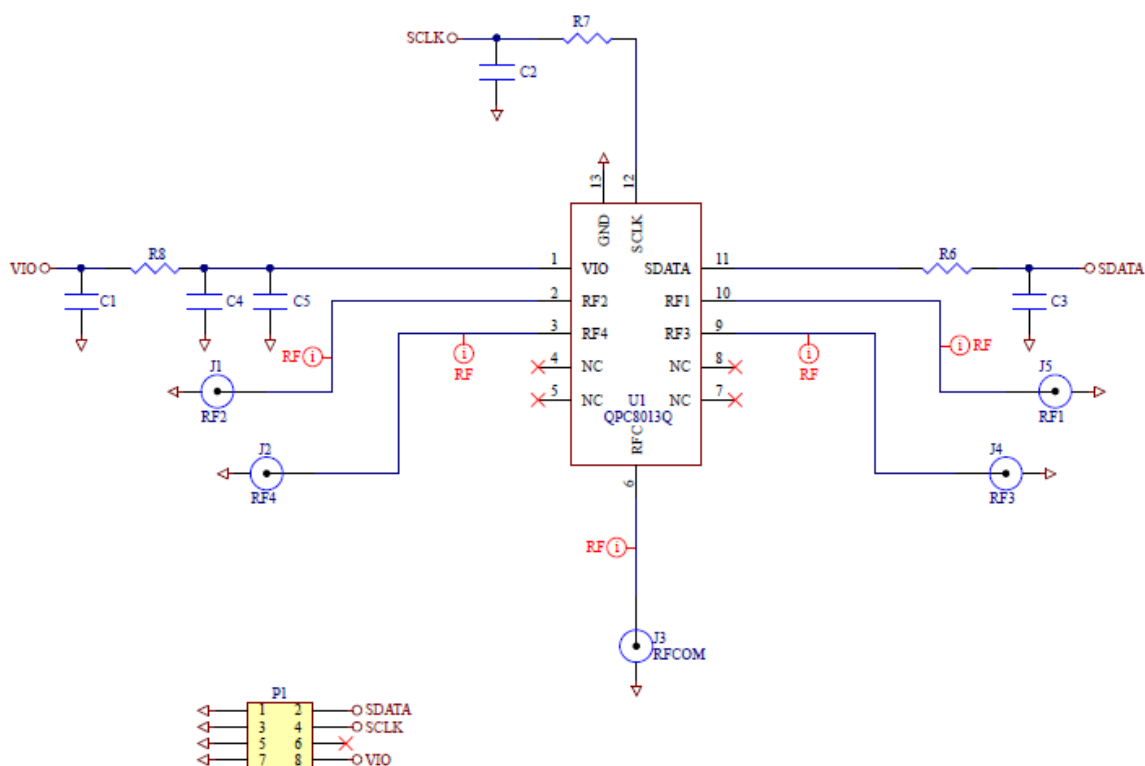
| STATE | INSERTION PORT | ISOLATION, TYPICAL (dB) | | | |
|-------|----------------|-------------------------|-----|-----|-----|
| | | RF1 | RF2 | RF3 | RF4 |
| RF1 | RF1 | | 37 | 31 | 44 |
| RF2 | RF2 | 37 | | 44 | 32 |
| RF3 | RF3 | 31 | 41 | | 44 |
| RF4 | RF4 | 41 | 31 | 44 | |
| RF1 | RFC | | 43 | 38 | 34 |
| RF2 | RFC | 42 | | 34 | 39 |
| RF3 | RFC | 40 | 40 | | 34 |
| RF4 | RFC | 39 | 41 | 34 | |

Isolation Matrix High Band (2300MHz – 2690MHz)

| STATE | INSERTION PORT | ISOLATION, TYPICAL (dB) | | | |
|-------|----------------|-------------------------|-----|-----|-----|
| | | RF1 | RF2 | RF3 | RF4 |
| RF1 | RF1 | | 34 | 28 | 40 |
| RF2 | RF2 | 34 | | 40 | 29 |
| RF3 | RF3 | 28 | 38 | | 40 |
| RF4 | RF4 | 38 | 28 | 40 | |
| RF1 | RFC | | 39 | 34 | 31 |
| RF2 | RFC | 38 | | 31 | 35 |
| RF3 | RFC | 37 | 37 | | 32 |
| RF4 | RFC | 36 | 38 | 31 | |

Application Circuit Schematic

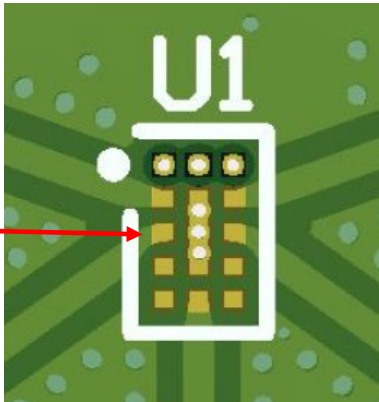
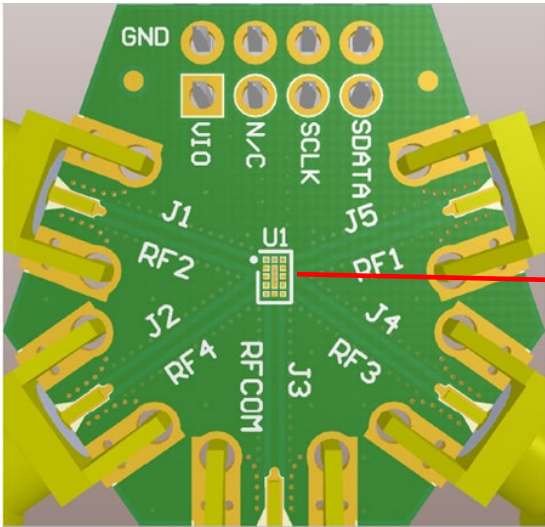
It is recommended to GND the NC pins. All RF ports should be terminated in 50 ohms.



Application EVB BOM

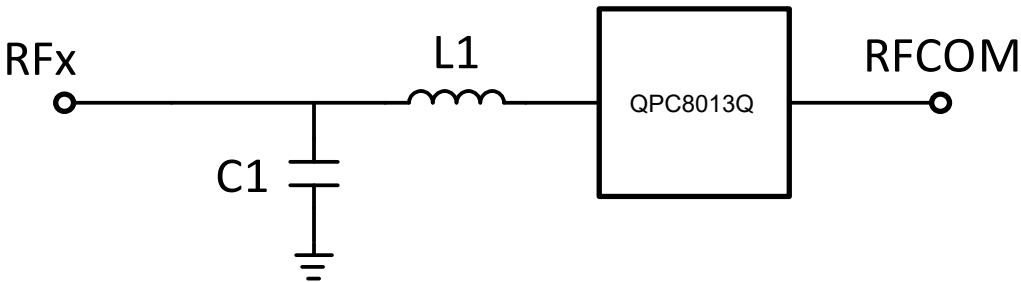
| Qty | Ref Des | Description |
|-----|-----------------------|--|
| 1 | U1 | SP4T, LTE, RFFE |
| 1 | PCB | PCB, QPC8013Q-4000(A) |
| 3 | C1,C2,C3 | CAP, 100pF, 5%, 25V, C0G, 0201 |
| 3 | R6,R7,R8 | RES, 0 OHM, 5%, 1/20W, 0201 |
| 5 | RF1,RF2,RF3,RF4,RFCOM | CONN, SMA, EL MINI FLT 0.068" SPE-000303 |
| 1 | P1 | CONN, HDR, SHRD, RT-ANG, 2x4, 0.100" |
| 1 | C4*,C5* | NOT POPULATED ITEM-1 |

Application EVB



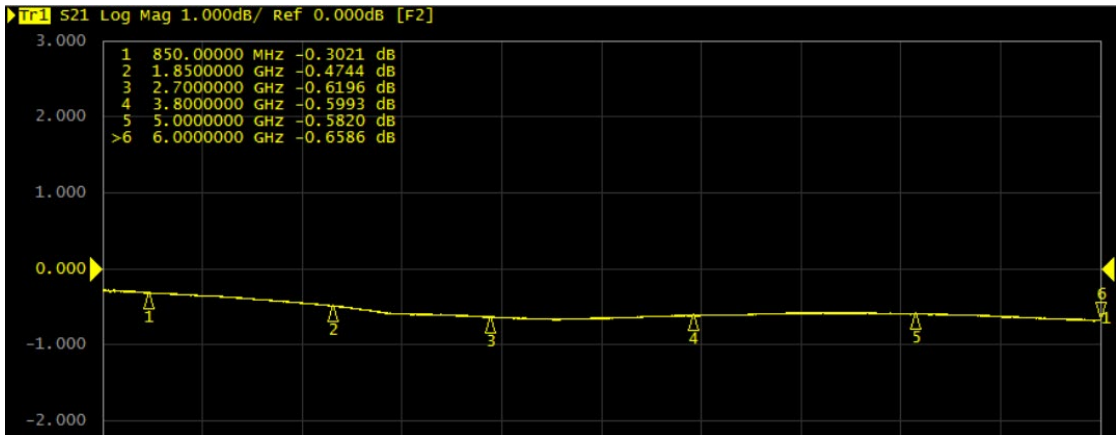
3 vias on center GND pad for thermal conductivity

Tuning Schematic for 5000MHz – 6000MHz

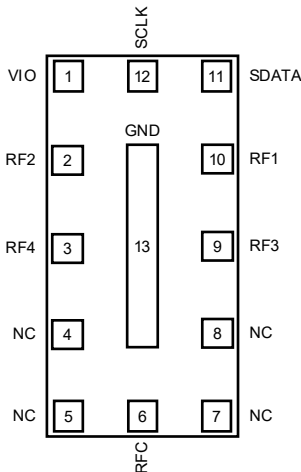


| NAME | VALUE | PACKAGE | DESCRIPTION |
|------|-------|---------|--|
| C1 | 0.3pF | 0201 | Matching for optimized RF performance* |
| L1 | 1.0nH | 0201 | Matching for optimized RF performance* |

* Matching elements are subject to change based on specific system application



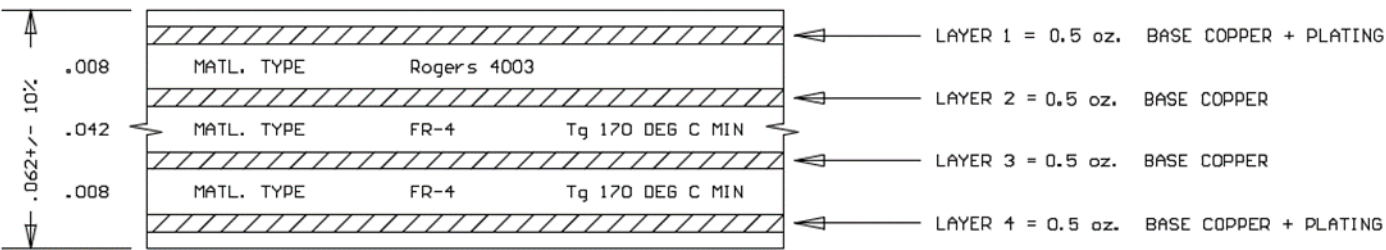
Pin Configuration and Description



Top View

| PIN NO. | LABEL | DESCRIPTION |
|---------|-------|-------------------|
| 1 | VIO | Voltage Supply |
| 2 | RF2 | RF Port |
| 3 | RF4 | RF Port |
| 4 | NC | No Connect |
| 5 | NC | No Connect |
| 6 | RFC | RF Common Port |
| 7 | NC | No Connect |
| 8 | NC | No Connect |
| 9 | RF3 | RF Port |
| 10 | RF1 | RF Port |
| 11 | SDATA | RFFE Data Signal |
| 12 | SCLK | RFFE Clock Signal |
| 13 | GND | Ground |

Evaluation Board PCB Information



RFFE Register Map

Register 0x0000 — SW_CTRL0

| Bit(s) | Field Name | Description | Reset | B/G | Trig | R/W |
|--------|------------|---|-------|-----|-------|-----|
| 7:4 | SPARE | Reserved for future use | 0x0 | No | 0 - 2 | R/W |
| 3:0 | SW_CTRL | 0x00: Isolation 0x01: RF1 - RFC 0x02: RF2 - RFC 0x04: RF3 - RFC 0x08: RF4 - RFC | 0x0 | No | 0 - 2 | R/W |

Register 0x0001 — SPARE

| Bit(s) | Field Name | Description | Reset | B/G | Trig | R/W |
|--------|------------|-------------------------|-------|-----|-------|-----|
| 7:0 | SPARE | Reserved for future use | 0x00 | No | 0 - 2 | R/W |

Register 0x001C — PM_TRIG

| Bit(s) | Field Name | Description | Reset | B/G | Trig | R/W |
|--------|------------------|---|-------|-----|------|-----|
| 7:6 | PWR_MODE[1:0] | 00: ACTIVE - Normal Operation 01: STARTUP - Reset all registers to default settings 10: ACTIVE - Low Power - Antenna in isolation 11: STARTUP - Reset all registers to default settings <i>Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.</i> | 0b10 | B/G | No | R/W |
| 5:3 | TriggerMask[2:0] | Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates <u>before</u> Trigger[N] is processed <i>Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register. If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.</i> | 0b000 | No | No | R/W |
| 2:0 | Trigger[2:0] | Setting bit Trigger[N] loads Trigger[N]'s associated registers <i>Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.</i> | 0b000 | B/G | No | W |

Register 0x001D — PRODUCT_ID

| Bit(s) | Field Name | Description | Reset | B/G | Trig | R/W |
|--------|--------------|--|-------|-----|------|-----|
| | | Lower eight bits of Product Number | | | | |
| 7:0 | PROD_ID[7:0] | <i>Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.</i> | 0x17 | No | No | R |

Register 0x001E — MANUFACTURER_ID

| Bit(s) | Field Name | Description | Reset | B/G | Trig | R/W |
|--------|-------------|--|-------|-----|------|-----|
| | | Lower eight bits of MIPI Manufacturer ID | | | | |
| 7:0 | MFG_ID[7:0] | <i>Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.</i> | 0x34 | No | No | R |

Register 0x001F — MAN_USID

| Bit(s) | Field Name | Description | Reset | B/G | Trig | R/W |
|--------|-------------|---|-------|-----|------|-----|
| 7:6 | RESERVED | Reserved for future use | 0b00 | No | No | R |
| | | Upper two bits of MIPI Manufacturer ID | | | | |
| 5:4 | MFG_ID[9:8] | <i>Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.</i> | 0b01 | No | No | R |
| | | Programmable Unique Slave ID | | | | |
| 3:0 | USID[3:0] | <i>Note: USID is only writeable using a special programming sequence. See MIPI 6.6.2 for details.</i> | 0x8 | No | No | R/W |

Register 0x0020 — EXT_PRODUCT_ID

| Bit(s) | Field Name | Description | Reset | B/G | Trig | R/W |
|--------|---------------|--|-------|-----|------|-----|
| | | Upper eight bits of Product Number | | | | |
| 7:0 | PROD_ID[15:8] | <i>Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.</i> | 0x00 | No | No | R |

Register 0x0021 — REVISION_ID

| Bit(s) | Field Name | Description | Reset | B/G | Trig | R/W |
|--------|----------------|--------------------------------|--------|-----|------|-----|
| 7:6 | MAJOR_REV[1:0] | Major Revisions - all layer | 0b00 | No | No | R |
| 5:4 | MINOR_REV[1:0] | Minor Revisions - metal only | 0b00 | No | No | R |
| 3:0 | MISC_REV[3:0] | Misc Revisions - mask variants | 0b0001 | No | No | R |

Note: The REVISION_ID register contains this product's revision number which is set by Qorvo according to manufacture date. The value may change throughout the product life cycle.

Register 0x0022 — GSID0-1

| Bit(s) | Field Name | Description | Reset | B/G | Trig | R/W |
|--------|------------|-----------------|-------|-----|------|-----|
| 7:4 | GSID0[3:0] | Group Slave ID0 | 0x0 | No | No | R/W |
| 3:0 | GSID1[3:0] | Group Slave ID1 | 0x0 | No | No | R/W |

Register 0x0023 — UDR_RST

| Bit(s) | Field Name | Description | Reset | B/G | Trig | R/W |
|--------|------------|---|-------|-----|------|-----|
| 7 | UDR_RST | Setting this bit initiates a software reset <i>Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.</i> | 0 | No | No | W |
| 6:0 | RESERVED | | 0x00 | No | No | R |

Register 0x0024 — ERR_SUM

| Bit(s) | Field Name | Description | Reset | B/G | Trig | R/W |
|--------|---------------|---|-------|-----|------|-----|
| 7 | SPARE | Reserved for future use | 0 | No | No | R/W |
| 6 | CMD_FR_P_ERR | Command Frame received with a parity error | 0 | No | No | R/W |
| 5 | CMD_LEN_ERR | Command Sequence received with an incorrect length | 0 | No | No | R/W |
| 4 | ADDR_FR_P_ERR | Address Frame received with a parity error | 0 | No | No | R/W |
| 3 | DATA_FR_P_ERR | Data Frame received with a parity error | 0 | No | No | R/W |
| 2 | RD_INVLD_ADDR | Read Command Sequence received with an invalid address | 0 | No | No | R/W |
| 1 | WR_INVLD_ADDR | Write Command Sequence received with an invalid address | 0 | No | No | R/W |
| 0 | BID_GID_ERR | Read Command Sequence received with a BSID or GSID | 0 | No | No | R/W |

Note: Reading this register resets this register.

Register 0x002C — TEST_PATT

| Bit(s) | Field Name | Description | Reset | B/G | Trig | R/W |
|--------|----------------|--------------|-------|-----|------|-----|
| 7:0 | TEST_PATT[7:0] | Test Pattern | 0xD2 | No | No | R |

Power On and Off Sequence

It is very important that the user adheres to the correct timing sequences in order to avoid damaging the device. Figures are NOT drawn to scale.

1. Once VIO is powered down to 0V, wait a minimum of 10 μ s to reapply power to VIO. (see figure 3)

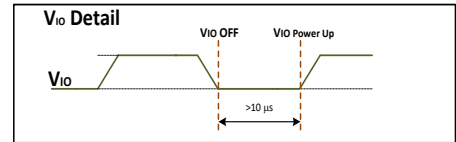


Figure 1 Digital Supply Detail

2. VIO must be applied for a minimum of 120 ns before sending SDATA/SCLK to ensure correct data transmission. (see figure 5)
3. VIO must be applied for a minimum of 15 μ s before applying RF power. (see figure 5)
4. Wait a minimum of 5 μ s after RFFE bus is idle to apply an RF signal. (see figure 5)

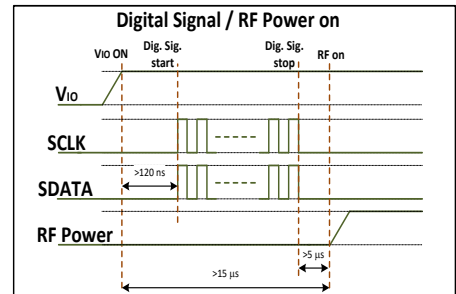


Figure 2 Digital Signal / RF Power-On Detail

5. RF power must not be applied during switching events. To ensure this, remove RF power before completing a register write that will change the switch mode. (see figure 6)

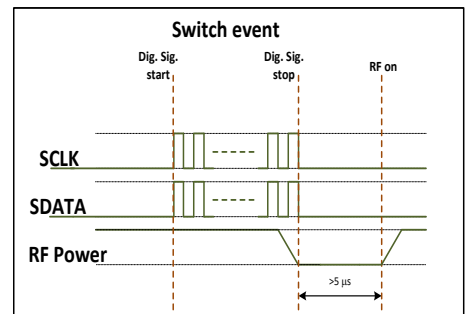


Figure 3 Switch Event Timing

6. If "Low Power Mode" is utilized, there must be a delay of 10 μ s before exiting "Low Power Mode". (see figure 7)

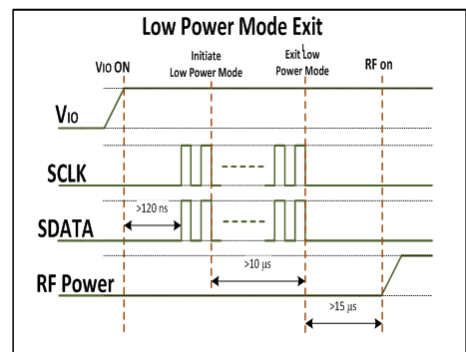
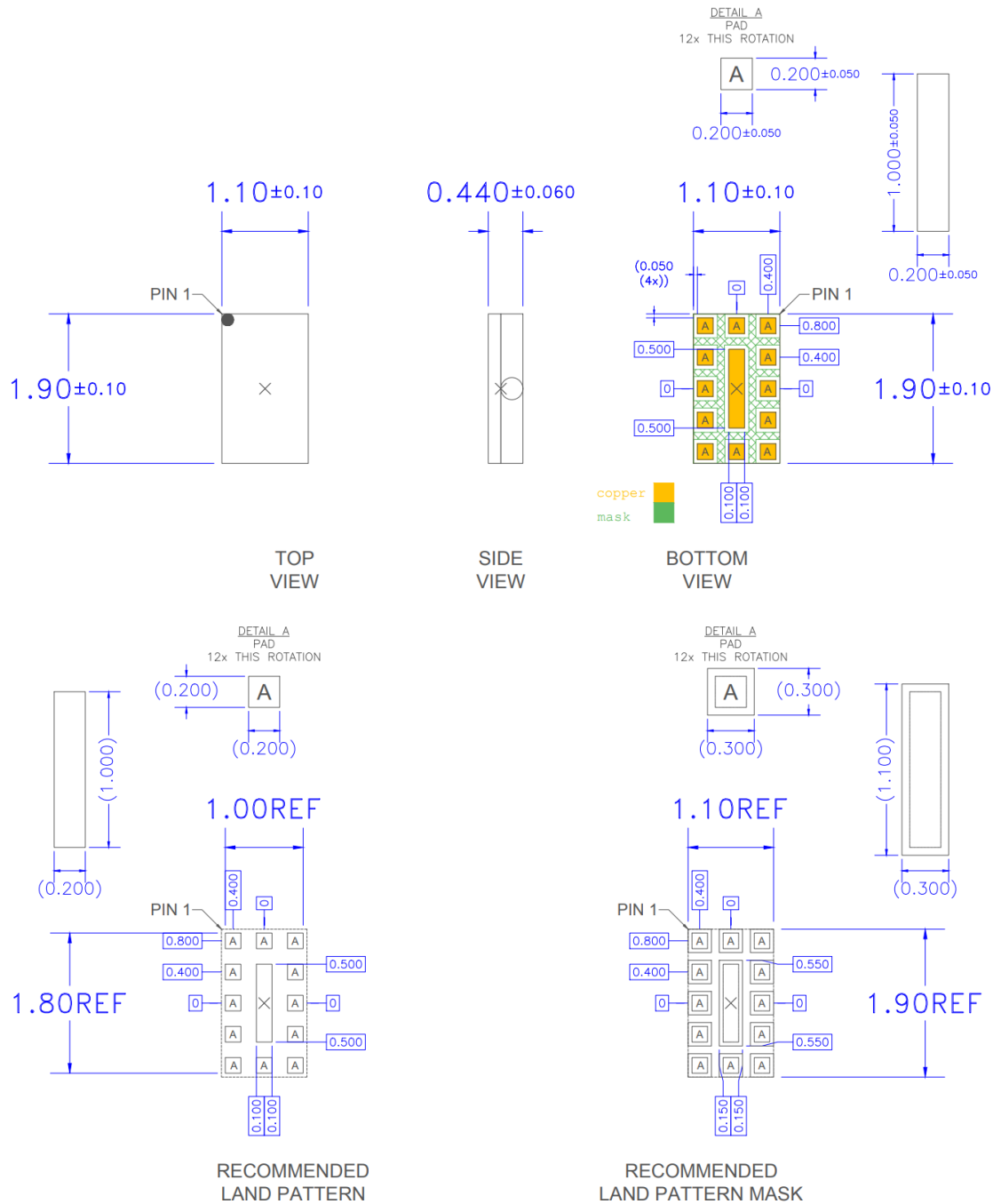


Figure 4 Low Power Mode Exit Timing

Mechanical Information

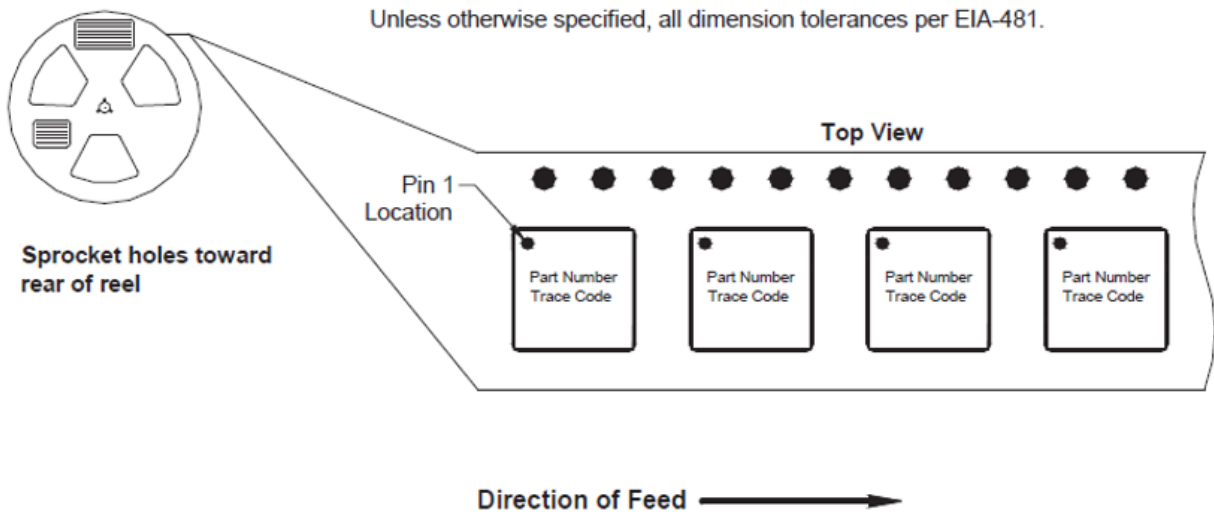


Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Tape and Reel Information

| Qorvo Part Number | Reel Diameter Inch (mm) | Hub Diameter Inch (mm) | Width (mm) | Pocket Pitch (mm) | Feed | Units Per Reel |
|-------------------|-------------------------|------------------------|------------|-------------------|--------|----------------|
| QPC8013QTR13-10K | 13 (330) | 4 (102) | 8 | 4 | Single | 10000 |
| QPC8013QSR | 7 (178) | 2.5 (63) | 8 | 4 | Single | 100 |



1.10 mm x 1.90 mm (Carrier Tape Drawing with Part Orientation).

Handling Precautions

| PARAMETER | RATING | STANDARD |
|----------------------------------|---------------------|------------------------|
| ESD – Human Body Model (HBM) | Class 2 (2000V) | ESDA/JEDEC JS-001-2012 |
| ESD – Charge Device Model (CDM) | Class C3 (1000V) | ESDA/JEDEC JS-002-2012 |
| MSL – Moisture Sensitivity Level | Level 3 | IPC/JEDEC J-STD-020 |



Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: ENEPIG

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- SVHC Free
- PFOS Free



Revision History

| Revision Code | Date | Comments |
|---------------|------------|--|
| Rev 1.0 | 10-29-2018 | Initial Preliminary Datasheet |
| Rev 1.1 | 8/5/19 | Updated for TBD min/max values |
| Rev1.2 | 10/11/19 | Updated image |
| 1.3 | 11/29/19 | Updated matching for 6GHz |
| A | 11/16/20 | Updated TBDs for ESD, updated format |
| B | 10/11/21 | Prepared for PR: added EDS/MSL data, Updated specs per PR Run Test Data and CHAR data including AMR specs; Added EVB DUT shot. |

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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