



# QPB9337

## Dual-Channel Switch LNA Module

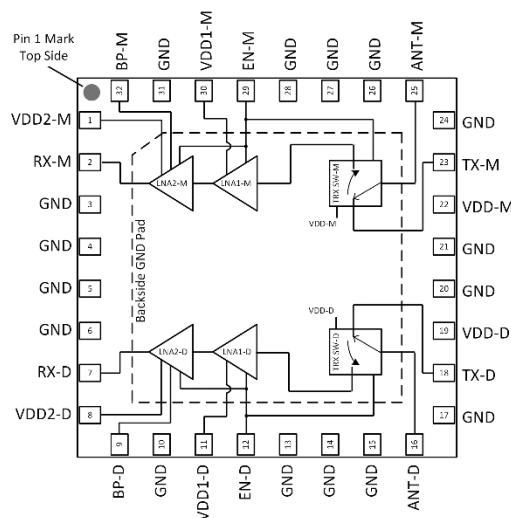
### Product Overview

The QPB9337 is a highly integrated front-end module targeted for TDD base stations. The switch LNA module integrates a two-stage LNA and a high power switch in a dual channel configuration. The second stage LNA has integrated bypass mode. Power down and bypass capability for the LNAs can be controlled with control pins on the module.

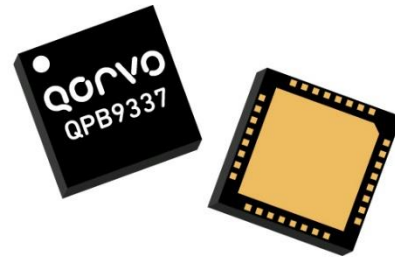
The QPB9337 can be utilized across the 2.3–3.8 GHz range to provide 1.3 dB noise figure for operation in the receive mode at 3.5 GHz and 0.8 dB insertion loss in the transmit mode. The LNAs utilize Qorvo's high performance E-pHEMT process while the SOI technology based switch supports input RF power signals of 8W average power. The product only needs a +5V supply to operate the high power switch and the LNAs.

The QPB9337 is packaged in a RoHS-compliant, compact 6 mm x 6 mm surface-mount leadless package. The switch LNA module is targeted for wireless infrastructure applications configured for TDD-based MIMO architectures. The module can be used for next generation 5G or pre-5G solutions or small cell base-station applications.

### Functional Block Diagram



Top View



32 Pin 6 mm x 6 mm leadless SMT Package

### Key Features

- 2.3 - 3.8 GHz Frequency Range
- 1.3 dB Noise Figure
- Second LNA with Bypass mode
- Pin (Tx mode): 8W Pavg
- 35.6 dB Gain (Rx mode, High Gain state)
- 18 dB Gain (RX mode, Low Gain state)
- +31 dBm OIP3 (Rx mode, High Gain state)
- 1.8V Logic Compatibility
- 3 to 5V Operational for Switch and LNAs

### Applications

- Wireless Infrastructure
- Small Cell BTS
- Pre-5G / 5G Massive MIMO systems
- TDD-based architectures

### Ordering Information

Part No.	Description
QPB9337TR13	2500 pcs on a 13" reel
QPB9337EVB-01	Evaluation Board

## Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150 °C
Supply Voltage (Pins 1, 8, 11, 19, 22, 30)	+6 V
Pin at ANT, Rx mode, Average (8 dB PAR, 100% Duty Cycle, 105°C)	19 dBm
Pin at ANT, Tx mode, Average (8dB PAR, 88% Duty Cycle, 8.8ms max, 105°C)	39 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

## Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
LNA Voltage	+3	+5	+5.25	V
Switch V <sub>DD</sub>	+3	+5	+5.5	V
T <sub>CASE</sub>	-40		+105	°C
T <sub>j</sub> <sup>(1)</sup> Rx Mode			+190	°C
T <sub>j</sub> <sup>(1)</sup> Tx Mode Pin 5W at max T <sub>CASE</sub>			+125	°C

Notes:

1. MTTF > 1e6 hours

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

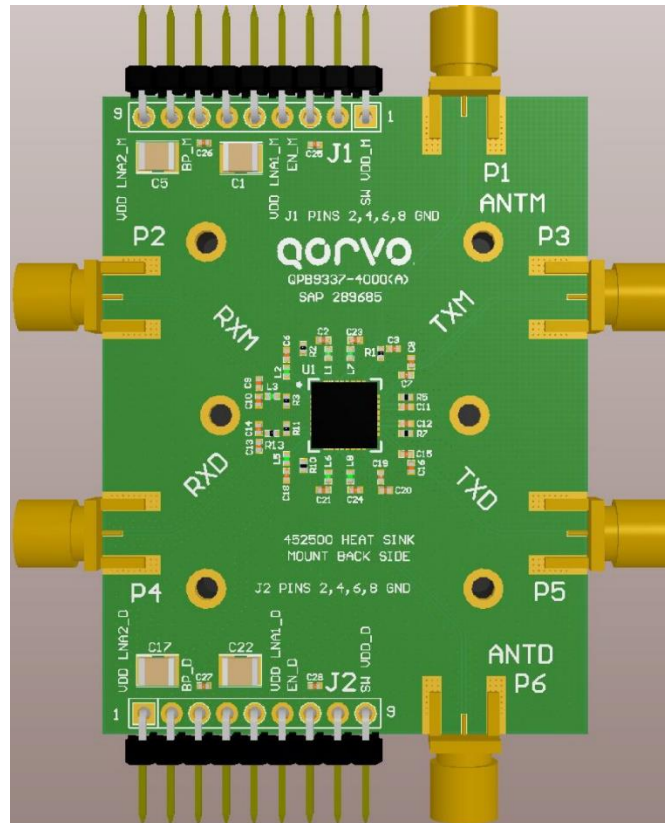
Parameter	Conditions <sup>(1)</sup>	Min	Typ	Max	Units
Operational Frequency Range		2300		3800	MHz
Test Frequency			3500		MHz
Gain <sup>(2)</sup>	Rx mode, High Gain state	34	35.6	39	dB
	Rx mode, Low Gain state	17	18	22	dB
Gain Flatness	Rx mode, Any 100 MHz BW within band		0.3		dB
Noise Figure <sup>(2)</sup>	Rx mode, High Gain state		1.3	1.55	dB
Output IP3 <sup>(3)</sup>	Rx mode, High Gain state	27	31		dBm
	Rx mode, Low Gain state	24	29		dBm
OP1dB <sup>(2)</sup>	Rx mode, High Gain state	18	19		dBm
	Rx mode, Low Gain state	10	12		dBm
Insertion Loss <sup>(2)</sup>	Tx mode		0.8	1.5	dB
VSWR	ANT Port, and TX Port		1.5:1	2.0:1	--
Switch Isolation	ANT to TX in Rx mode		25		dB
Switch Isolation	ANT to RX in Tx mode		40		dB
Channel Isolation	Rx mode, High Gain state		39		dB
	Tx mode		40		dB
LNA Supply Voltage			+5		V
LNA Current	Rx mode, High gain state, Per channel		113	150	mA
	Rx mode, Low gain state, Per channel		54	75	mA
LNA Shutdown Current	Per channel		9		mA
LNA and Switch Control Voltage (Pins 9, 12, 29 and 32)	V <sub>LOW</sub>	0		+0.63	V
	V <sub>HIGH</sub>	+1.17		V <sub>DD</sub> +0.3	V
Switch Current	Tx mode		0.50		mA
Switching Time	ANT-TX ON		0.90		μs
	ANT-TX OFF		0.50		μs
	ANT-RX ON		1.00		μs
	ANT-RX OFF		0.05		μs
Thermal Resistance	Tx Mode			22.7	°C/W
	Rx High Gain Mode			23.0	°C/W

Notes:

1. Test conditions unless otherwise noted: Temp = +25 °C, 50 Ω system.
2. Trace loss de-embedded.
3. Pout/tone = +3dBm, Δf = 1MHz



## Evaluation Board Assembly



Top View

## Typical Performance

Test conditions unless otherwise noted:  $V_{DD}=+5\text{ V}$ ,  $\text{Temp}=+25^{\circ}\text{C}$

Parameter	Conditions	Typical Values			Units
Frequency		3400	3600	3800	MHz
Gain	Rx High Gain Mode	37.0	35.7	33.5	dB
	Rx Low Gain Mode	19.4	18.8	18.1	dB
Input Return Loss	Rx High Gain Mode	18.8	23.0	20.2	dB
	Rx Low Gain Mode	19.3	23.5	20.5	dB
Output Return Loss	ANT-RX Path, High Gain Mode	9.2	9.2	7.0	dB
	ANT-RX Path, Low Gain Mode	25.0	12.6	9.6	dB
Output P1dB	Rx High Gain Mode	20.0	19.5	18.7	dBm
	Rx Low Gain Mode	12.4	12.0	12.0	dBm
OIP3 <sup>(2)</sup>	Rx High Gain Mode	33.2	33.8	33.5	dBm
	Rx Low Gain Mode	29.7	30.0	29.2	dBm
Noise figure <sup>(1)</sup>	Rx High Gain Mode	1.43	1.42	1.42	dB
Insertion Loss <sup>(3)</sup>	ANT-TX, Tx Mode	0.80	0.79	0.78	dB
Isolation	ANT-RX, Tx Mode, Rx High Gain	83	65	66	dB
	ANT-TX, Rx Mode	28	28	27	dB
	RX-RX, Rx High Gain Mode	43	45	50	dB
	TX-TX, Tx Mode	58	58	57	dB

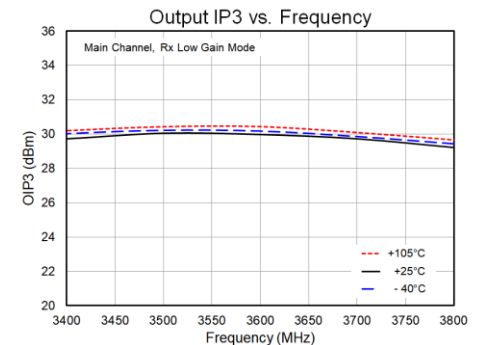
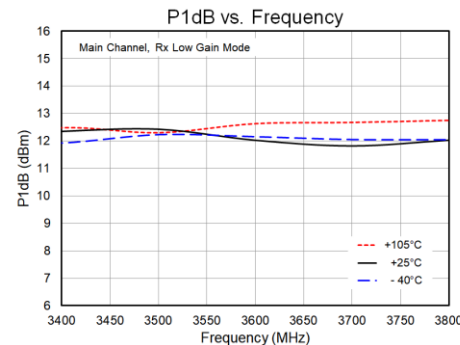
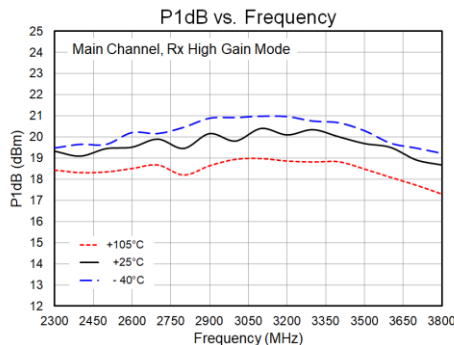
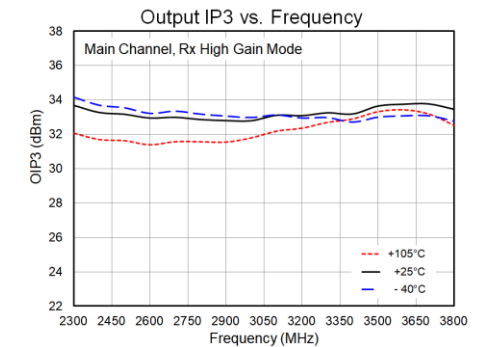
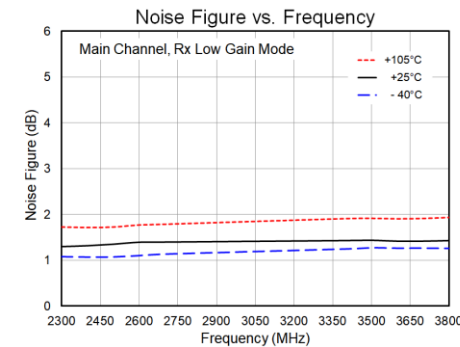
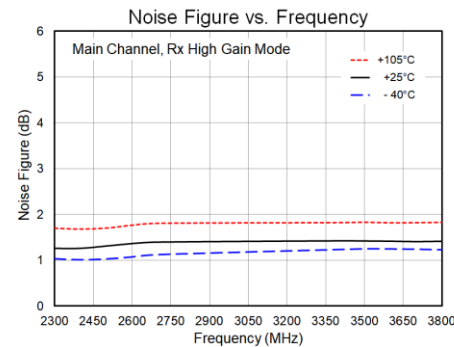
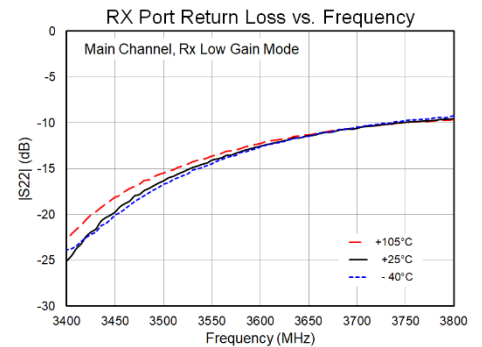
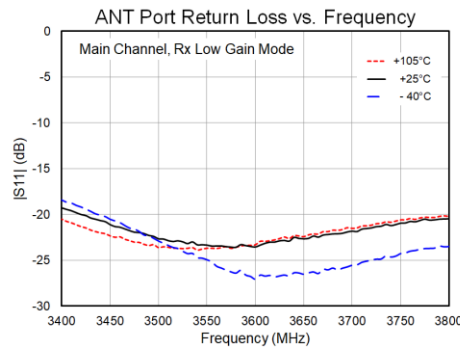
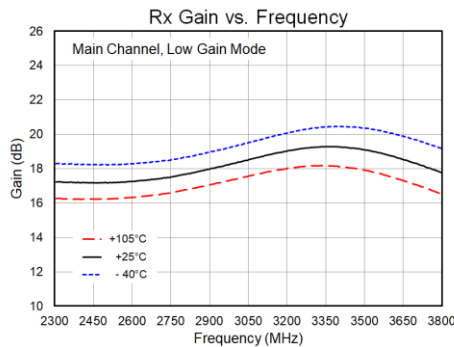
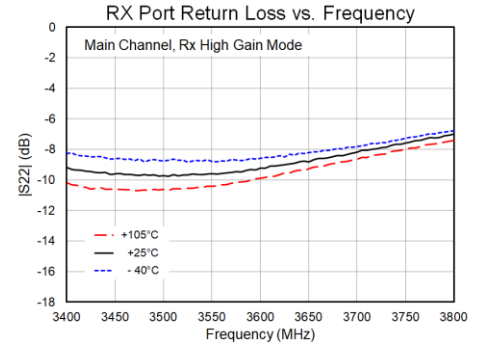
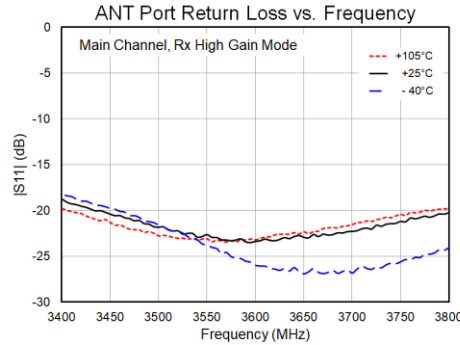
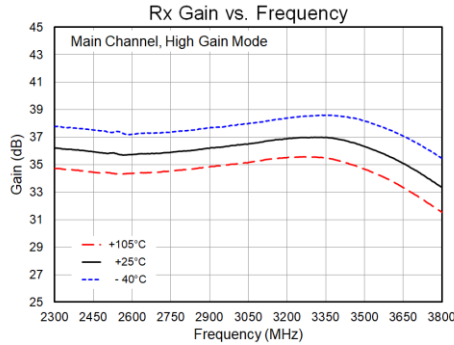
Note: 1) Noise figure data has input trace loss de-embedded. Insertion Loss has both Input and Output trace losses deducted.

2)  $P_{out}=+3\text{ dBm/tone}$ ,  $\Delta f=1\text{ MHz}$

3) De-embedded and mismatch losses removed

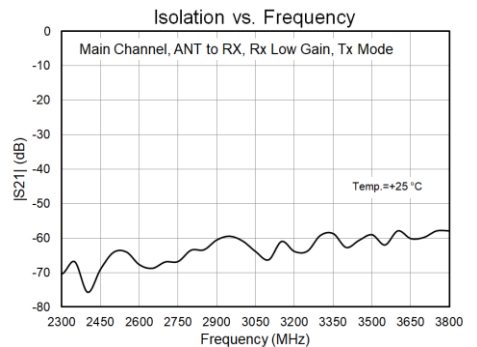
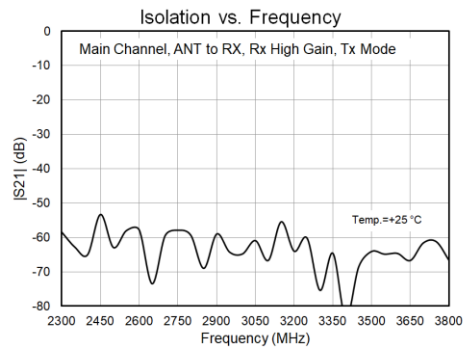
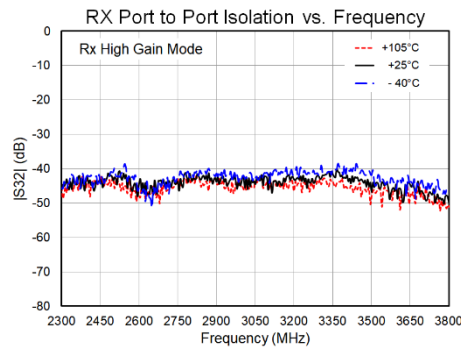
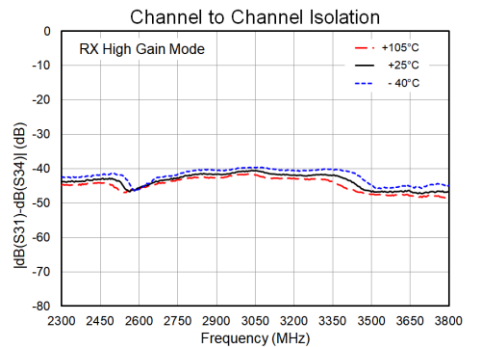
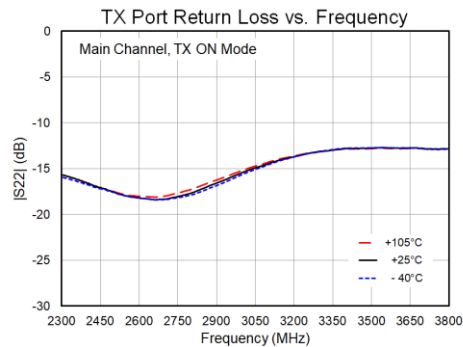
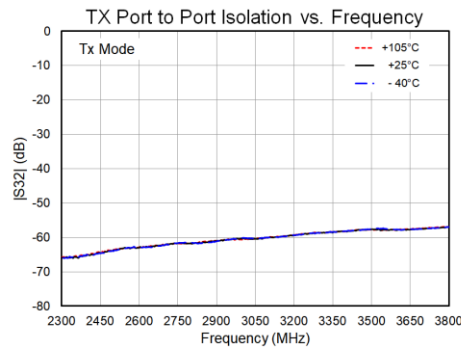
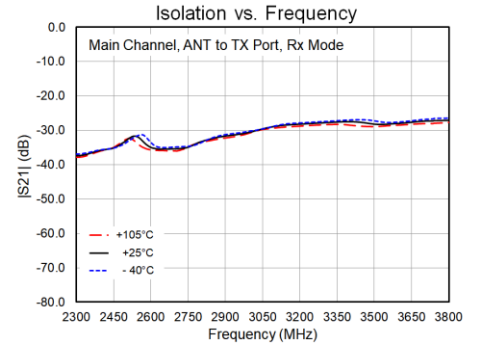
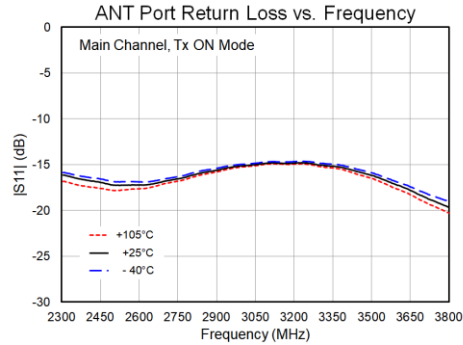
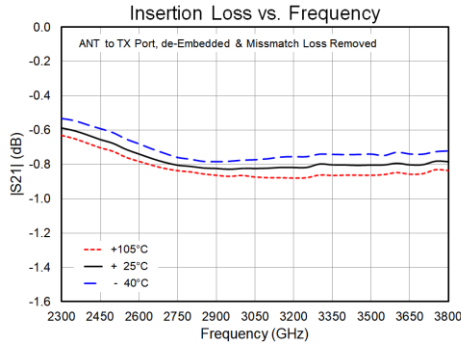
## Performance Plots

Test conditions unless otherwise noted:  $V_{DD} = +5\text{ V}$ , Temp. =  $+25^\circ\text{C}$

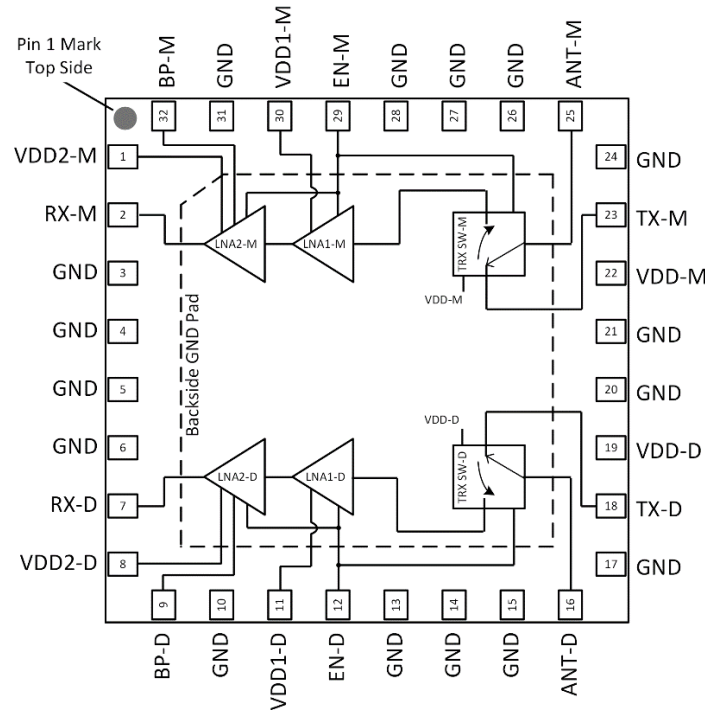


## Performance Plots Contd.

Test conditions unless otherwise noted:  $V_{DD} = +5$  V, Temp. = +25 °C



## Pin Configuration and Description



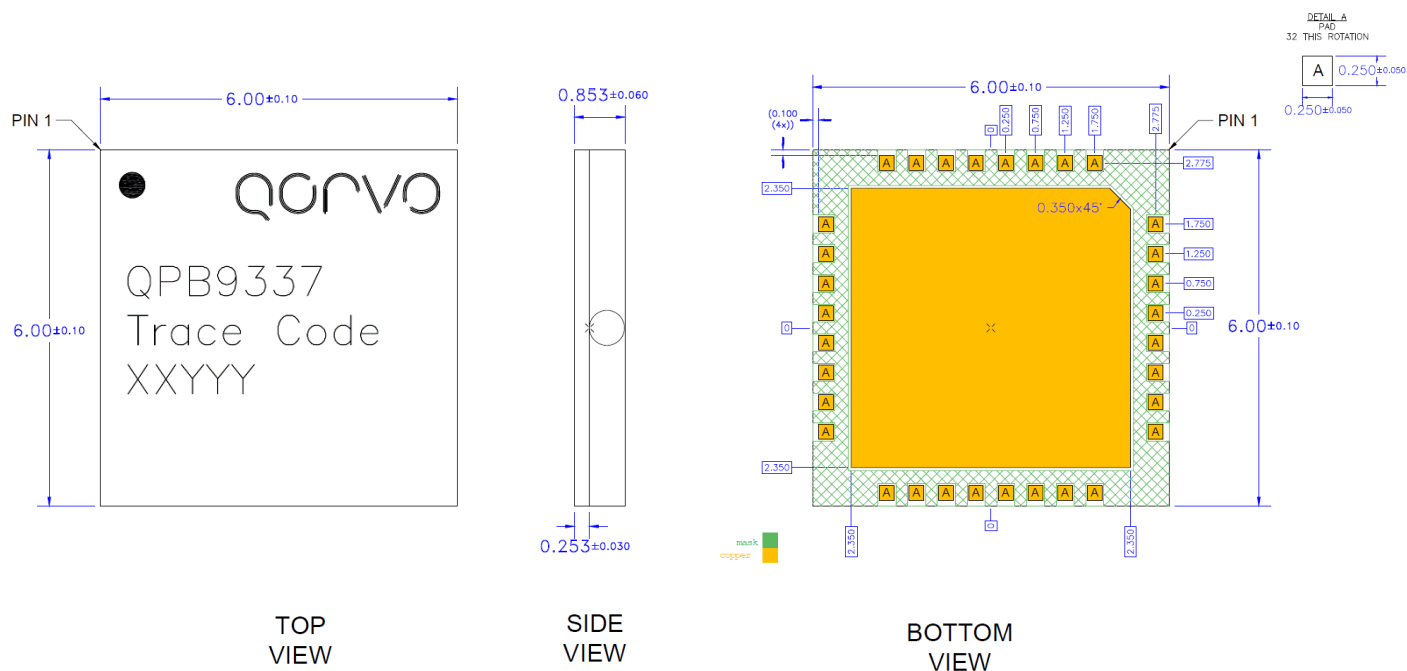
Top View

Pin No.	Label	Description
1	VDD2-M	The 2 <sup>nd</sup> stage LNA DC power supply input of the main channel
2	RX-M	Rx LNA RF output of the main channel
7	RX-D	Rx LNA RF output of the diversity channel
8	VDD2-D	The 2 <sup>nd</sup> stage LNA DC power supply input of the diversity channel
9	BP-D	The 2 <sup>nd</sup> stage LNA Bypass control input of the diversity channel. Enable (1) LNA low gain mode
11	VDD1-D	The 1 <sup>st</sup> stage LNA DC power supply input of the diversity channel
12	EN-D	Tx or Rx mode control input of the diversity channel. Enabled (1) Tx mode.
16	ANT-D	Antenna port of the diversity channel
18	TX-D	Tx or Termination port of the diversity channel
19	VDD-D	TRX switch DC power supply input of the diversity channel
22	VDD-M	TRX switch DC power supply input of the main channel
23	TX-M	Tx or Termination port of the main channel
25	ANT-M	Antenna port of the main channel
29	EN-M	Tx or Rx mode control input of the main channel. Enable (1) Tx mode.
30	VDD1-M	The 1 <sup>st</sup> stage LNA DC power supply input of the main channel
32	BP-M	The 2 <sup>nd</sup> stage LNA Bypass control input of the main channel. Enable (1) LNA low gain mode
3, 4, 5, 6, 10, 13, 14, 15, 17, 20, 21, 24, 26, 27, 28, 31, Package Base	GND	RF/DC ground connection. The back side of the package should be connected to the ground plan though multiple connections as short as possible. PCB via holes under the device are recommended.



### Package Marking and Dimensions

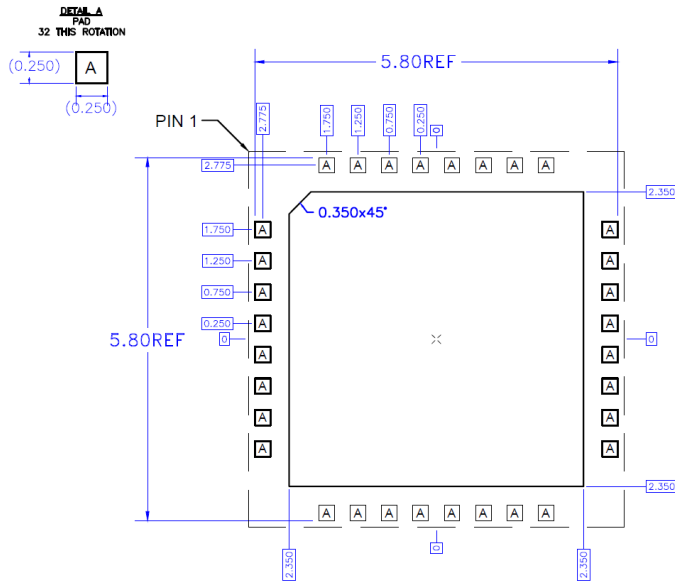
Marking: Part Number – QPB9337  
Trace Code – Assigned by Sub-Contractor  
XXYYY – Unit serialization



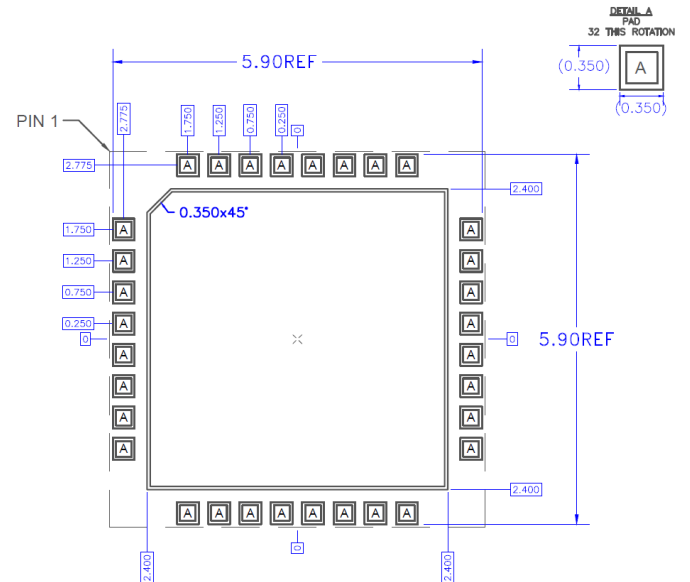
#### Notes:

1. All dimensions are in mm. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

## PCB Mounting Pattern



RECOMMENDED  
LAND PATTERN



RECOMMENDED  
LAND PATTERN MASK

### Notes:

1. All dimensions are in mm. Angles are in degrees.
2. A heat sink underneath the area of the PCB for the mounted device is recommended for proper thermal operation.
3. Ground / thermal via holes are critical for the proper performance of this device. Via holes should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
4. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Technical drawing of a mechanical part, showing a perspective view and a cross-section A-A.

**Perspective View:**

- Part is blue.
- Top surface features a row of 8 circular holes.
- Bottom surface features 5 rectangular slots.
- Blue arrow labeled "User Direction of Feed" points to the right.

**Cross-Section A-A:**

- Dimensions (from left to right):
  - 0.30 ± 0.05
  - R 0.3 MAX
  - K0
  - 2.00 ± 0.05 SEE NOTE 3
  - 4.00 SEE NOTE 1
  - Ø 1.5 +0.1/-0.0
  - 8.00
  - Ø 1.50 MIN
  - 1.75 ± 0.10
  - 5.50 ± 0.05 SEE NOTE 3
  - 12.0 ± 0.3
  - 12.0
  - .12
  - .12
  - R.25
- Section line A-A is indicated.

**Table:**

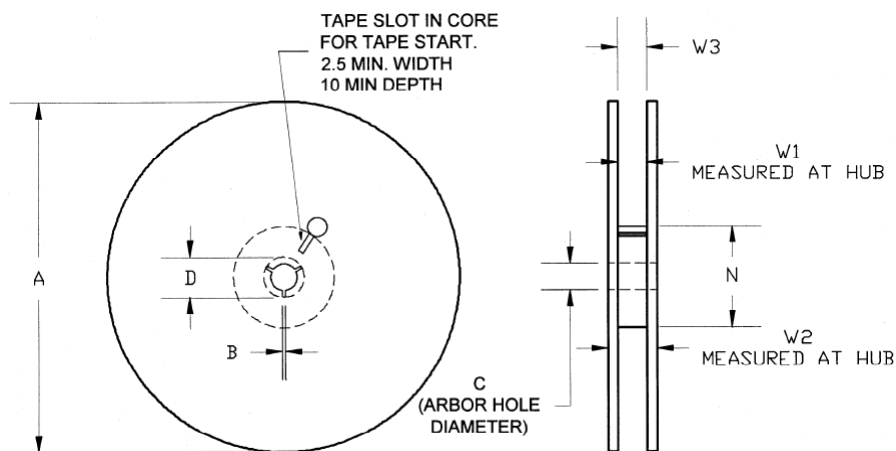
A0 =	6.40
B0 =	6.40
K0 =	1.50

**SECTION A - A**

Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.252	6.40
	Width	B0	0.252	6.40
	Depth	K0	0.059	1.50
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.00

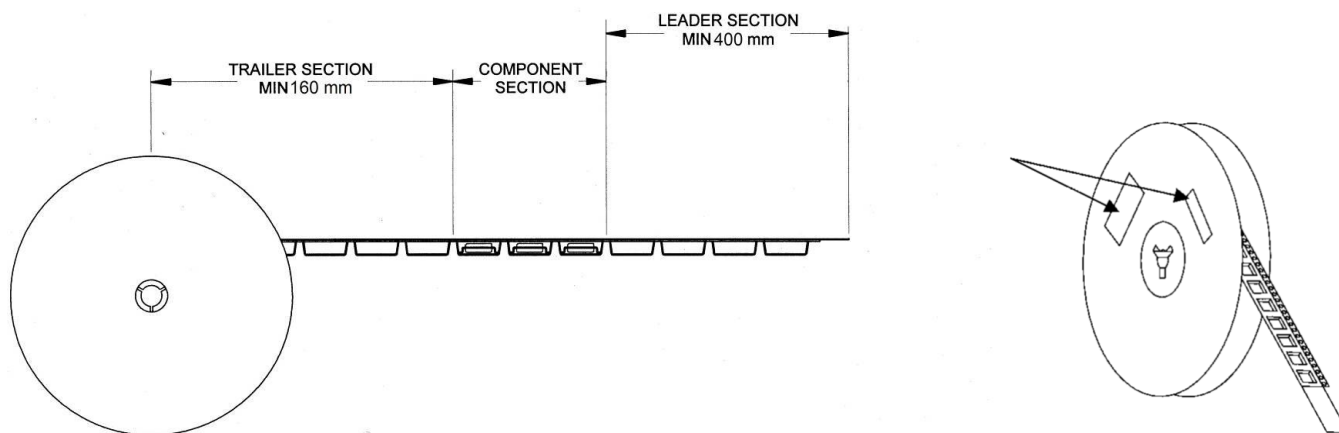
## Tape and Reel Information – Reel Dimensions (13")

Standard T/R size = 2,500 pieces on a 13" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

## Tape and Reel Information – Tape Length and Label Placement



### Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

## Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ANSI / ESDA / JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C2	ANSI / ESDA / JEDEC JS-002
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!  
ESD-Sensitive Device

## Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: NiPdAu (*Electroless Plating Thickness: Ni 3.5 ± 1.5 μm – Pd 0.145 ± 0.035 μm – Au 0.095 ± 0.025 μm*)

## RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: [www.qorvo.com](http://www.qorvo.com)

Tel: 1-844-890-8163

Email: [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

For technical questions and application information:

Email: [appsupport@qorvo.com](mailto:appsupport@qorvo.com)

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