



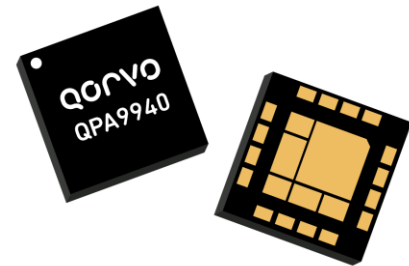
QPA9940

2300-2400MHz 4 W High-Efficiency Amplifier

Product Overview

The QPA9940 is a high-efficiency, linearizable power amplifier targeting Band 40 small-cell wireless infrastructure systems. Using InGaP/GaAs HBT technology, the product delivers high efficiency of 31% at +28dBm average output power while providing excellent DPD linearized ACPR of -50 dBc for signal bandwidths of up to 100MHz.

The QPA9940 is housed in a 5x5mm SMT package. It is pin-to-pin compatible to QPA9901, QPA9903 and QPA9908 (high-efficiency small cell PA).

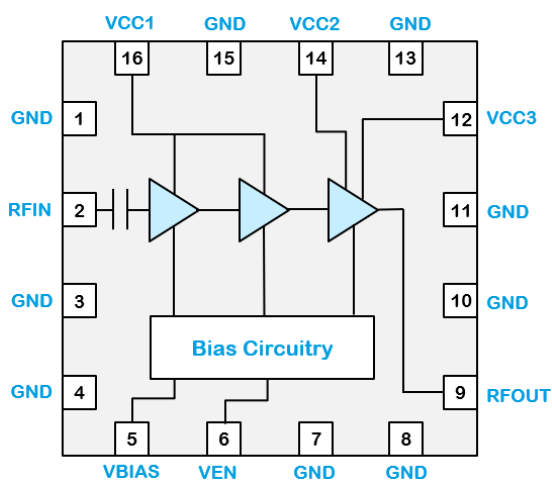


16 Pad 5 x 5 mm Package

Key Features

- 2300 – 2400 MHz
- 34.5 dB Gain
- Over 36 dBm P3dB
- 31% PAE at +28 dBm power output
- -50 dBc ACPR DPD Linearized at +28 dBm Power Output with 5-carrier signal
- 1.8V Logic Compatible PA ON/OFF Control
- On Chip ESD Protection
- 5 x 5 mm Package

Functional Block Diagram



Top View

Applications

- 4G/5G Small-cell BTS
- 5G M-MIMO
- Repeaters / DAS
- Mobile Infrastructure
- General Purpose Wireless

Ordering Information

Part No.	Description
QPA9940TR13	2500pcs on 13" reel
QPA9940EVB-01	2300-2400 MHz EVB

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to +125 °C
RF Input Power, Pulsed CW, 50 Ω ⁽¹⁾	+10 dBm
Device Voltage (V _{CC})	+5.5 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

1. 2300-2400 MHz, Pulsed CW, 10% duty cycle, 100us period

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V _{CC})	+4.75	+5	+5.25	V
T _{CASE}	-40		+105	°C
T _j for >10 ⁶ hours MTTF			+175	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Units
Operational Frequency Range		2300		2400	MHz
Test Frequency			2350		MHz
Gain ⁽²⁾	At +28dBm Pout and room temperature	32	34.5		dB
Input Return Loss			-17		dB
Output Return Loss			-15		dB
Output P3dB	10 μ s pulse width, 10% duty cycle	35.1	+36		dBm
Power Added Efficiency ⁽²⁾	Pout = +28 dBm	28.1	31		%
ACPR (Uncorrected) ⁽²⁾	Pout = +28 dBm		-31	-28.4	dBc
ACPR (Uncorrected) ⁽³⁾	Pout = +28 dBm		-29		dBc
ACPR (Corrected) ⁽³⁾	Pout = +28 dBm		-50		dBc
Quiescent Current, I _{CC}	Pins 12, 14 and 16		100		mA
Total Operating Current	Pin 5, 12, 14 and 16, Pout = +28 dBm		406		mA
Thermal Resistance, θ_{jc}	Junction to case		23.3		°C/W
V _{EN} High		1.17	1.8	V _{CC}	V
V _{EN} Low		0	0	0.63	V
2nd Harmonic	Pout = +28 dBm		-40		dBc
3rd Harmonic	Pout = +28 dBm		-54		dBc
Turn-on time	Measured from 50% PA enable voltage level to 90% of RF amplitude		0.5		us

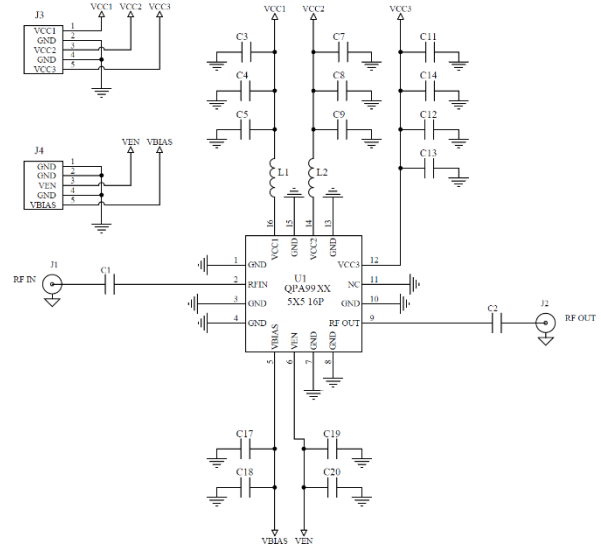
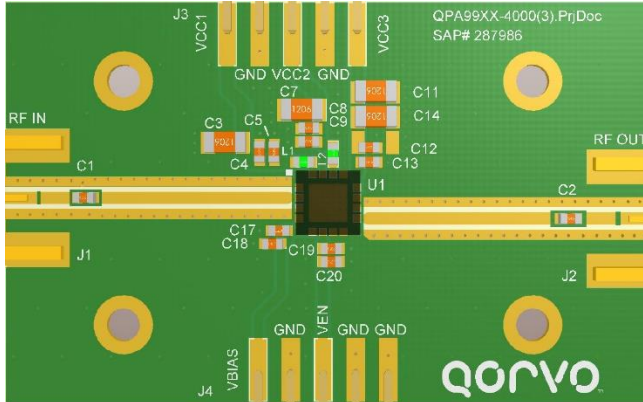
Notes:

1. Test conditions unless otherwise noted: All V_{CC} & V_{BIAS} = +5.0 V, V_{EN} = +1.8 V, Temp = +25 °C, 50 Ω system.
2. LTE, 20 MHz E-UTRA Test Mode 1.1 or 3.1, PAR = 8.5 dB at 0.01% probability.
3. LTE, 20 MHz x 5 E-UTRA Test Mode 1.1 or 3.1, PAR = 8.5 dB at 0.01% probability.

Power Amplifier Enable Logic Table

Parameter	High	Low
V _{EN}	Power Amplifier ON	Power Amplifier OFF

QPA9940 EVB Layout and Schematic



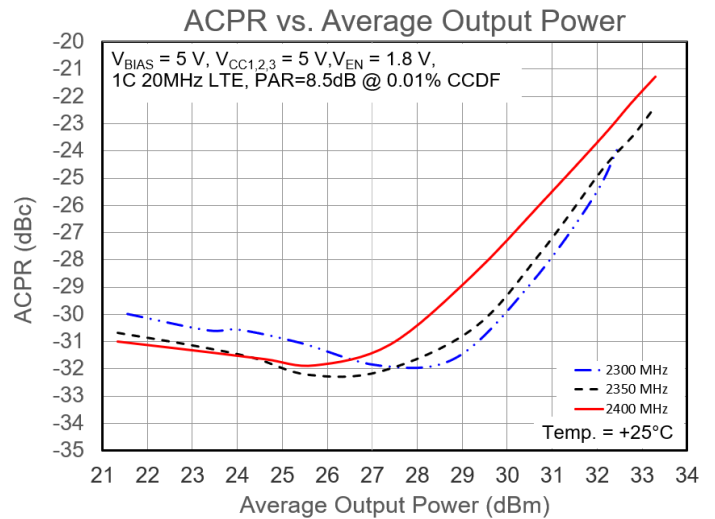
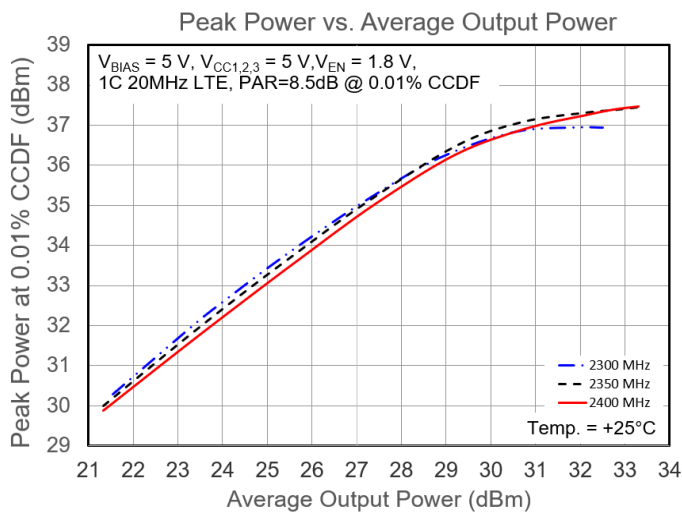
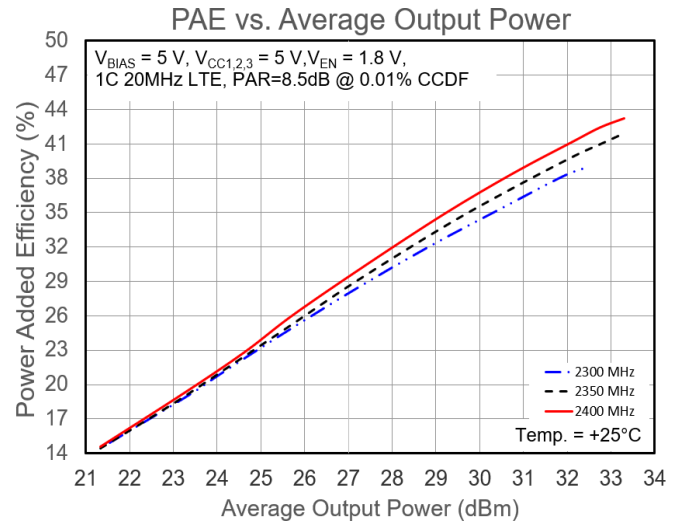
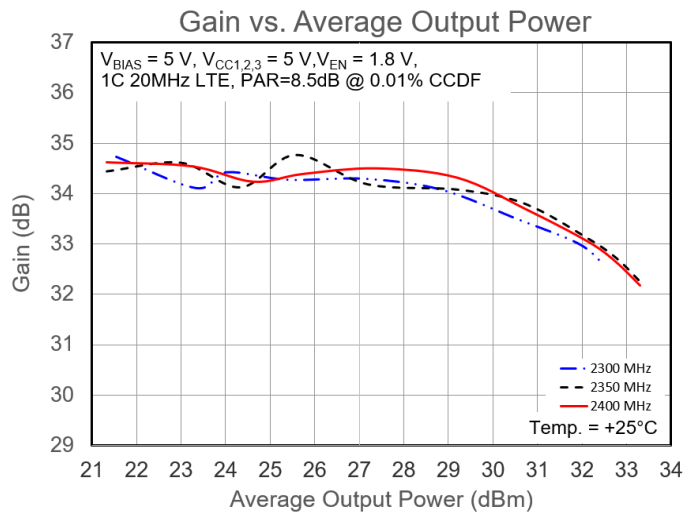
Notes:

1. See Evaluation Board PCB Information for material and stack up.

Bill of Materials – QPA9940EVB-01

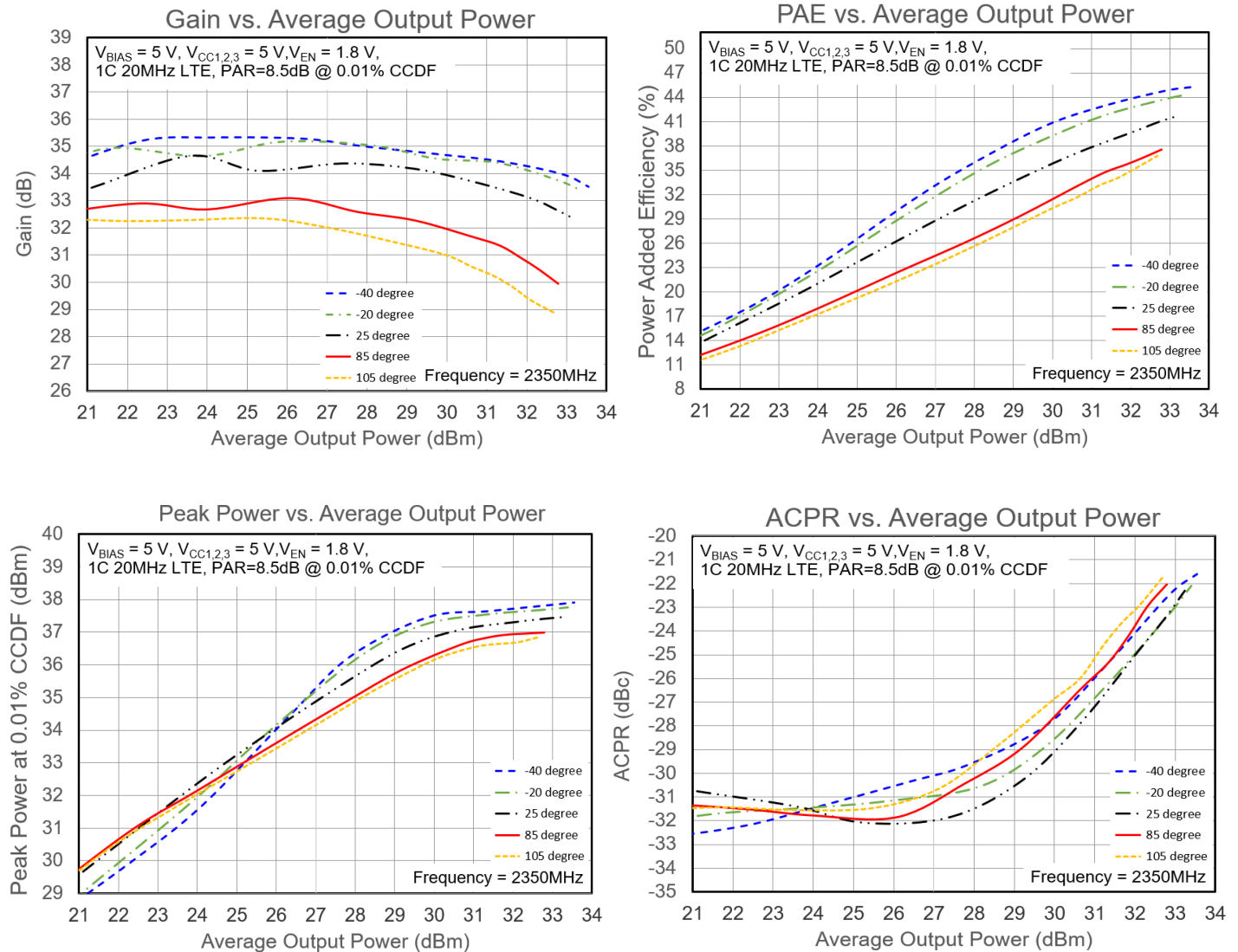
Reference Des.	Value	Description	Manuf.	Part Number
U1	-	Amplifier, QPA9940 2300-2400MHz, High-Efficiency	Qorvo	QPA9940
C1, C2	100 pF	CAP,100 pF, 0603, 5%, 50V, C0G	various	
C5, C9, C13, C17, C19	1000 pF	CAP,1000 pF, 0603, 5%, 50V, C0G	various	
C4, C8, C12, C18, C20	0.1 μ F	CAP,0.1 μ F, 0603, 10%, 50V, X7R	various	
C3, C7, C14	10 μ F	CAP, 10 μ F, 1206, 25V	various	
L1, L2	0 Ω	RES 0 Ω , 0603, 1/16W, Chip	various	
J1, J2	-	CONN. RF. SMA. F. STRT. Edge Mount	various	
J3, J4	-	Connector, 5 Pin	various	

Performance Plots - LTE



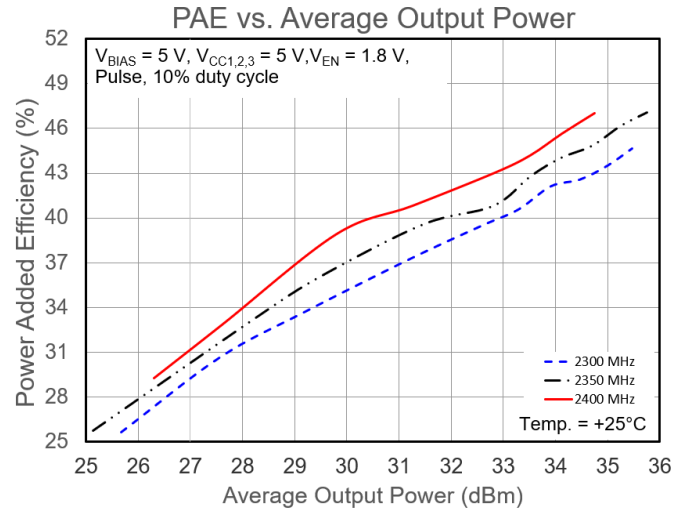
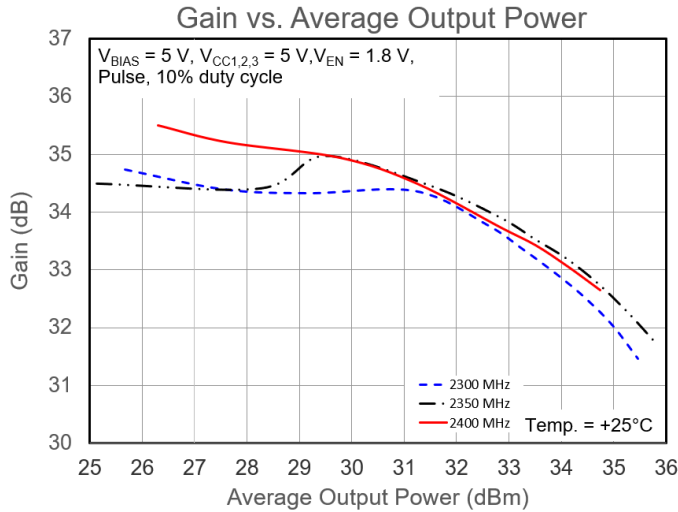
Test conditions unless otherwise noted: $V_{BIAS} = 5\text{ V}$, $V_{CC1,2,3} = 5\text{ V}$, $V_{EN} = 1.8\text{ V}$, $T = +25^\circ\text{C}$, tested using a single-carrier, 20 MHz LTE signal with 8.5 dB PAR at 0.01% CCDF on a reference design fixture.

Performance Plots - LTE

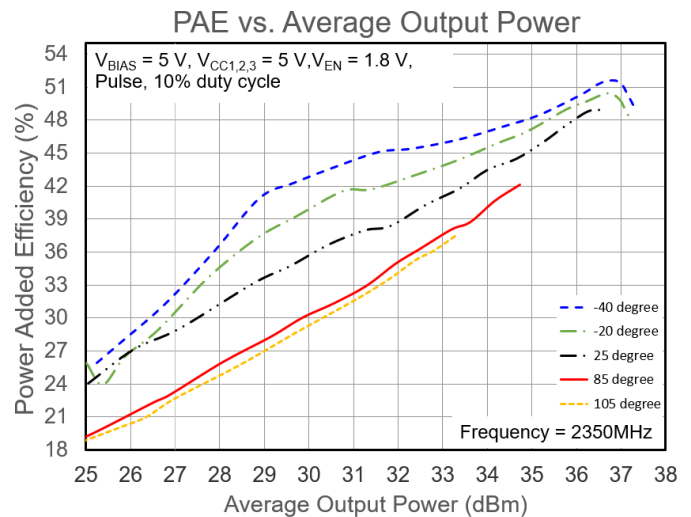
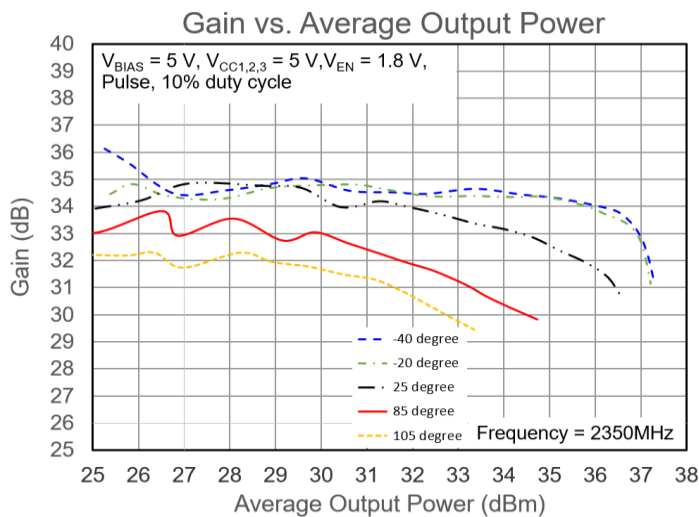


Test conditions unless otherwise noted: $V_{BIAS} = 5\text{ V}$, $V_{CC1,2,3} = 5\text{ V}$, $V_{EN} = 1.8\text{ V}$, tested at 2350 MHz using a single-carrier, 20 MHz LTE signal with 8.5 dB PAR at 0.01% CCDF on a reference design fixture.

Performance Plots - Pulse

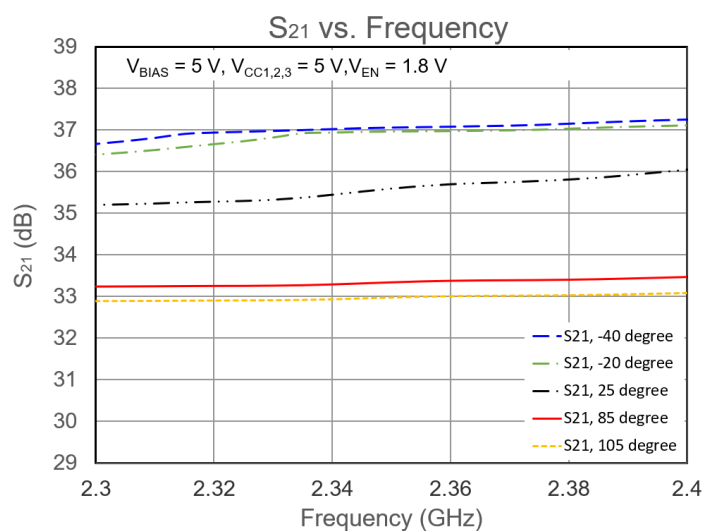
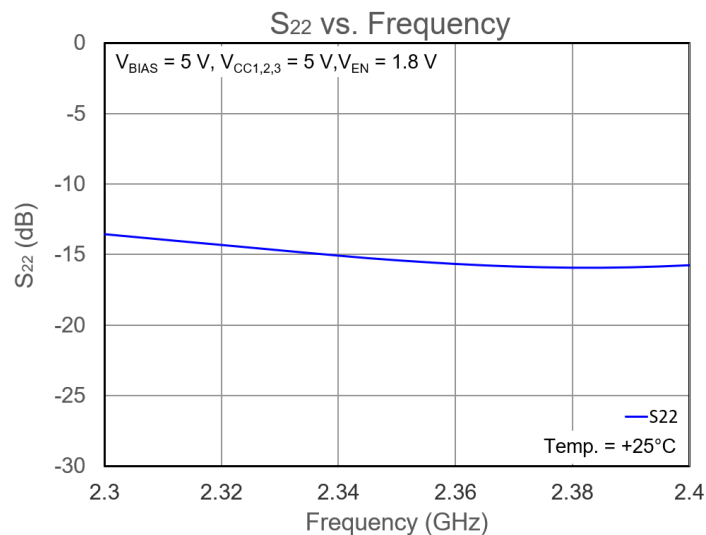
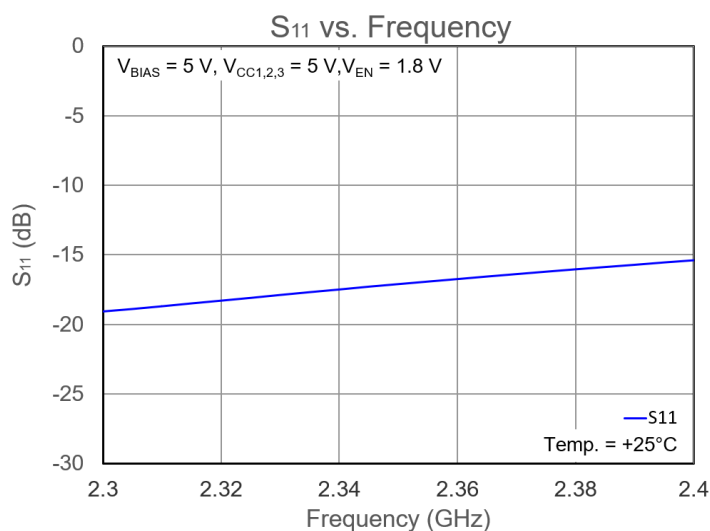


Test conditions unless otherwise noted: $V_{BIAS} = 5\text{ V}$, $V_{CC1,2,3} = 5\text{ V}$, $V_{EN} = 1.8\text{ V}$, $T = +25^\circ\text{C}$, tested using a pulse signal, 10% duty cycle.



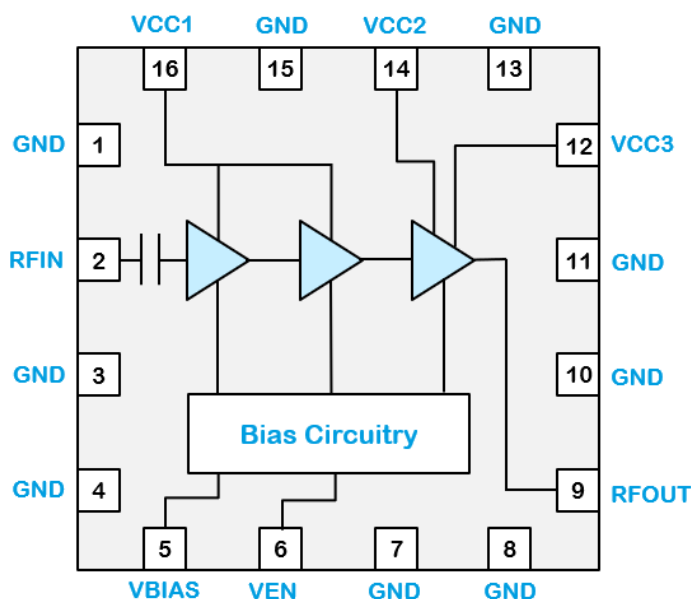
Test conditions unless otherwise noted: $V_{BIAS} = 5\text{ V}$, $V_{CC1,2,3} = 5\text{ V}$, $V_{EN} = 1.8\text{ V}$, tested at 2350 MHz using a pulse signal, 10% duty cycle.

Performance Plots – S-parameters



Test conditions unless otherwise noted: $V_{\text{BIAS}} = 5 \text{ V}, V_{\text{CC1,2,3}} = 5 \text{ V}, V_{\text{EN}} = 1.8 \text{ V}$.

Pad Configuration and Description



Top View

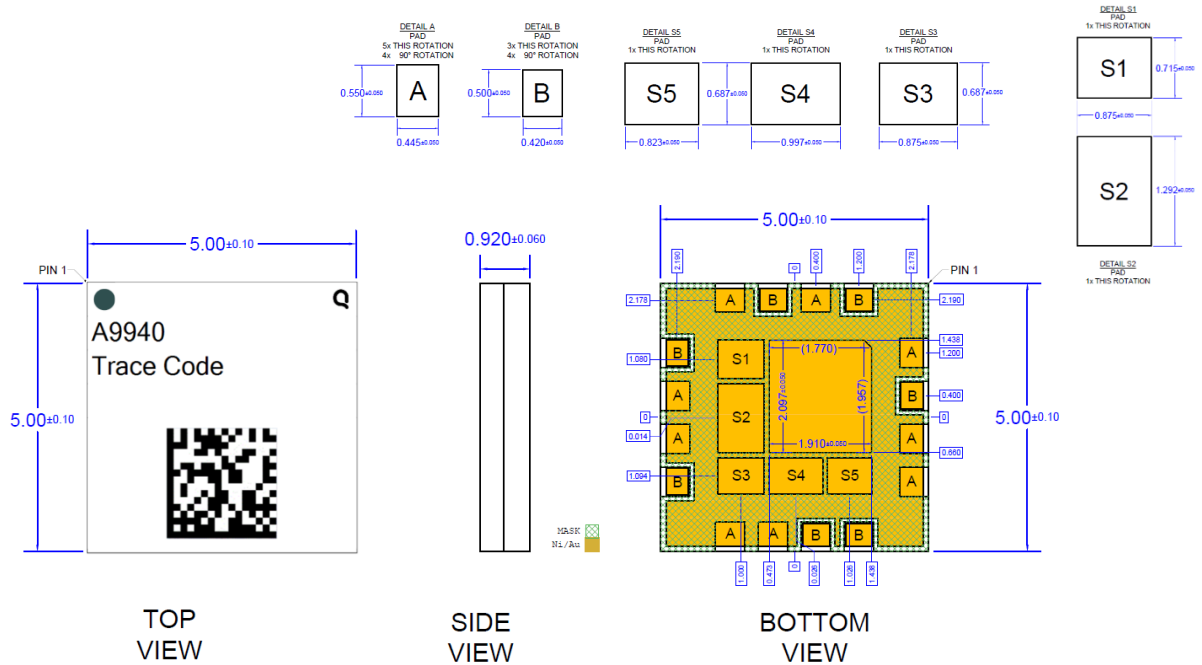
Pad No.	Label	Description
1, 3, 4, 7, 8, 10, 11, 13, 15	GND	Ground connection.
2	RF _{IN}	RF input, internally matched to 50Ω and DC blocked.
5	V _{BIAS}	Bias circuit supply voltage
6	V _{EN}	Amplifier enable voltage (regulated internally)
9	RF _{OUT}	RF output, internally matched to 50Ω and DC shorted. External DC blocking capacitor required
12	V _{CC3}	Supply voltage for the various amplifier stages
14	V _{CC2}	Supply voltage for the various amplifier stages
16	V _{CC1}	Driver stage supply voltage
Backside Paddle	GND	Ground connection. The back side of the package should be connected to the ground plane through as short of a connection as possible. PCB via holes under the device are recommended.

Package Marking and Dimensions

Marking: Pin 1 Indicator and Qorvo Logo

Part Number – QPA9940

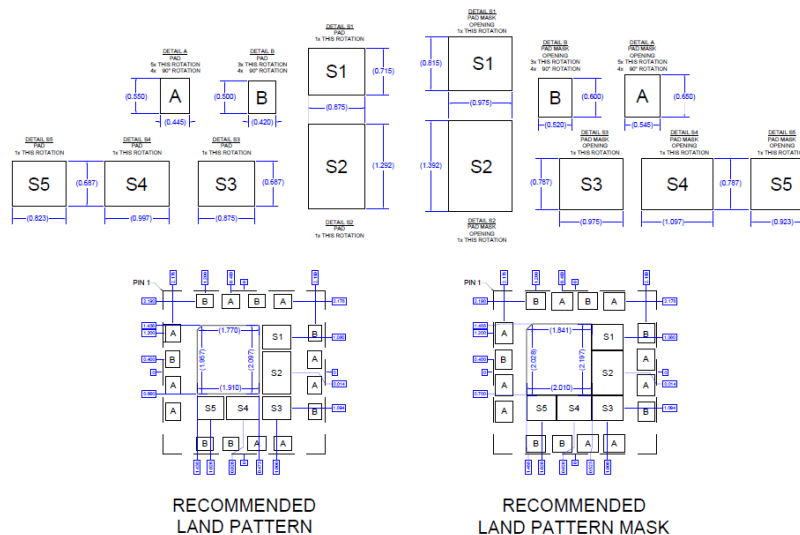
Trace Code – XXXXXX Up to 8 Characters to be Assigned by sub-Contractor



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Contact plating: ENEPIG

PCB Mounting Pattern

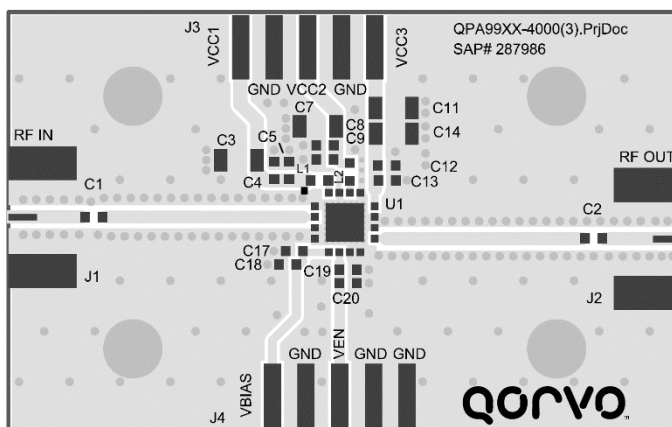


Evaluation Board PCB Information

PC Board Layout

Layer	Name	Material	Thickness	Constant
1	Top Overlay			
2	Top Solder	Solder Resist	0.40 mil	3.5
3	Top Layer	Copper	1.40 mil	
4	Dielectric1	RO4350	20.00 mil	3.48
5	Bottom Layer	Copper	1.40 mil	

Total thickness: 23.2mil

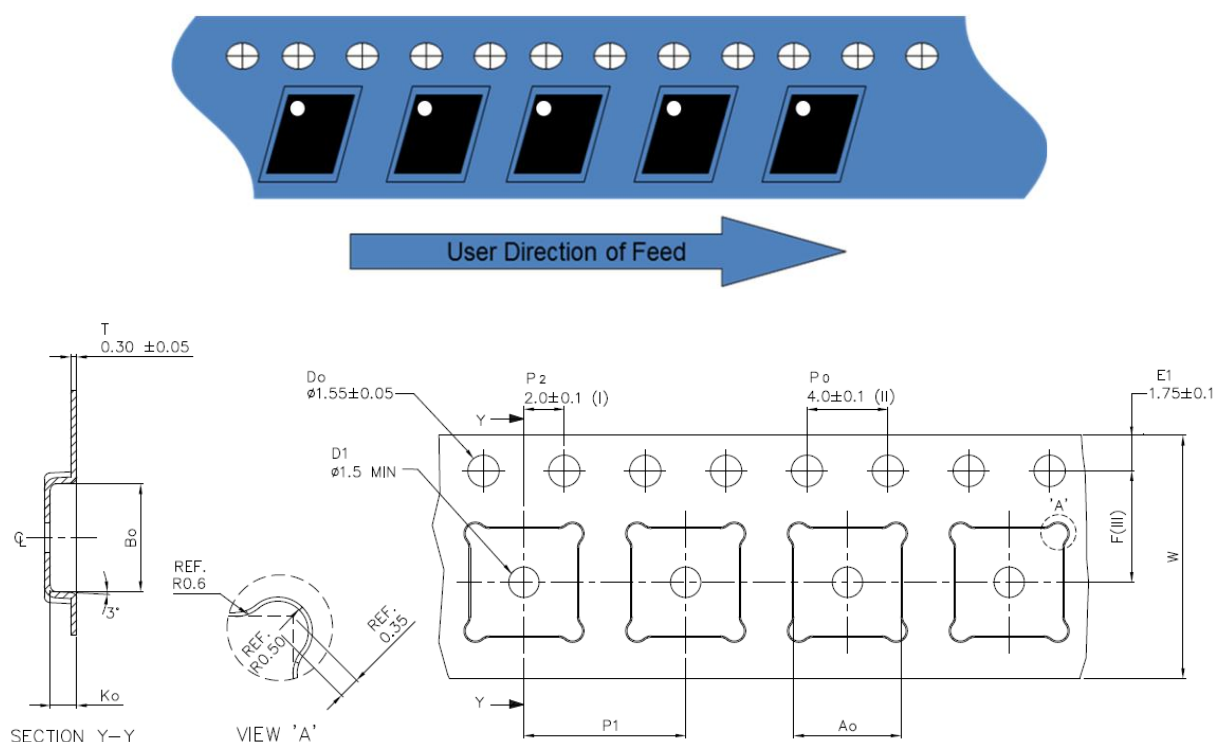


Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Tape and Reel Information – Carrier and Cover Tape Dimensions

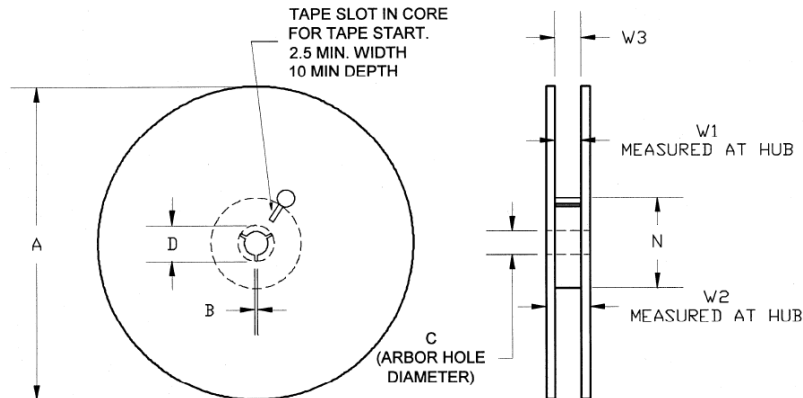
Tape and reel specifications for this part are also available on the Qorvo website.
 Standard T/R size = 2500 pieces on a 13" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.209	5.3
	Width	B0	0.209	5.3
	Depth	K0	0.051	1.3
	Pitch	P1	0.315	8.0
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.0
	Cavity to Perforation - Width Direction	F	0.217	5.5
Cover Tape	Width	C	0.362	9.2
Carrier Tape	Width	W	0.472	12

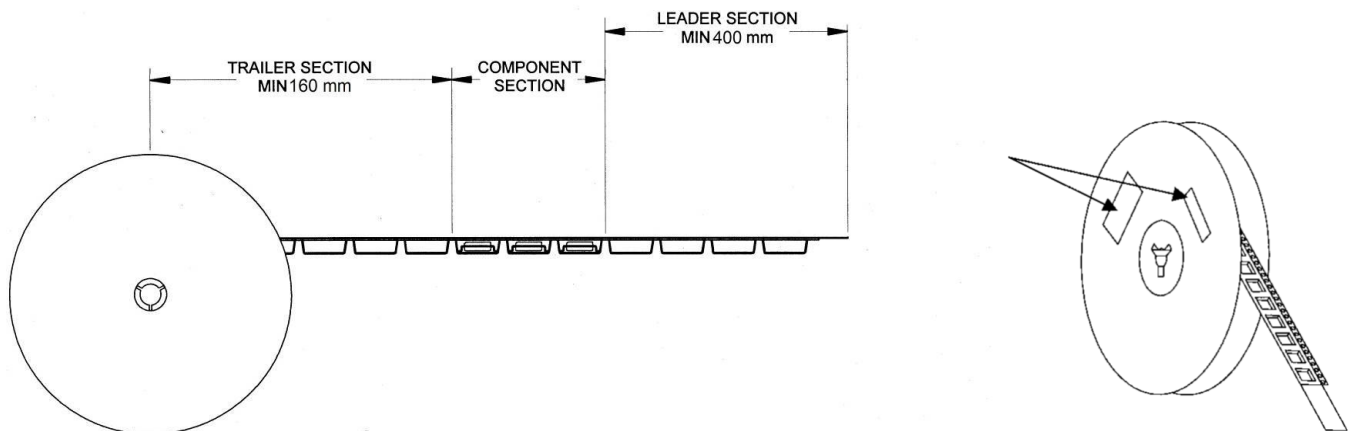
Tape and Reel Information – Reel Dimensions

Packaging reels are used to prevent damage to devices during shipping and storage, loaded carrier tape is typically wound onto a plastic take-up reel. The reel size is 13" diameter. The reels are made from high-impact injection-molded polystyrene (HIPS), which offers mechanical and ESD protection to packaged devices.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.00
	Thickness	W2	0.717	18.20
	Space Between Flange	W1	0.504	12.80
Hub	Outer Diameter	N	4.016	102.00
	Arbor Hole Diameter	C	0.512	13.00
	Key Slit Width	B	0.079	2.00
	Key Slit Diameter	D	0.795	20.2

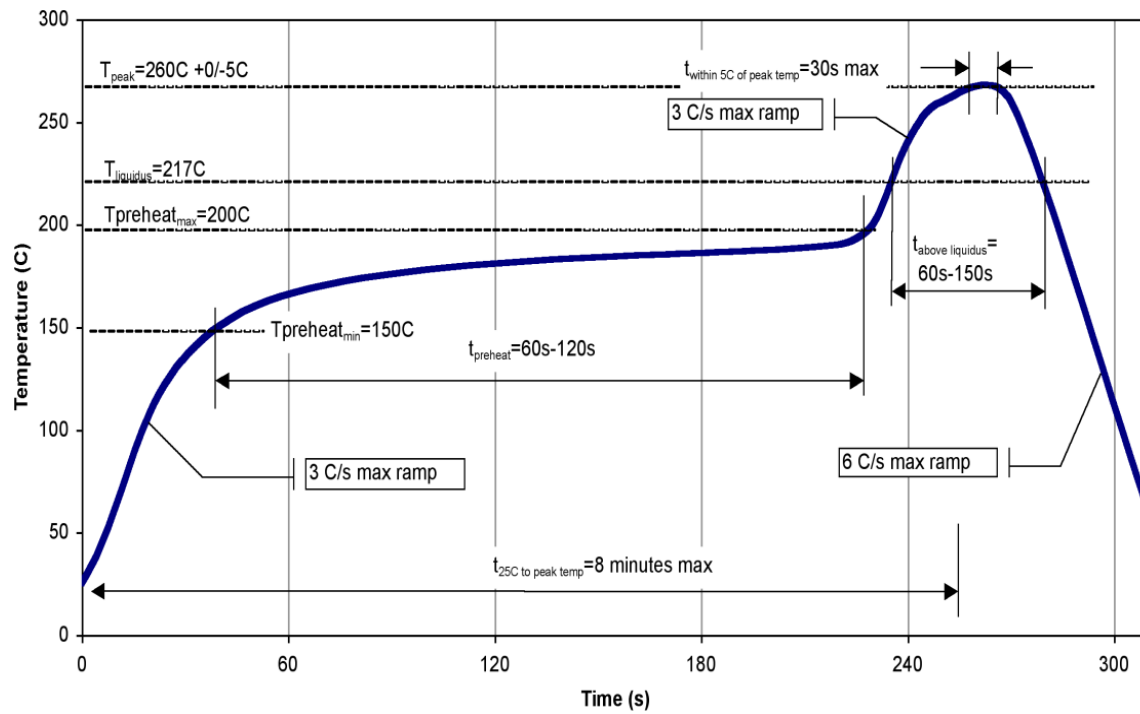
Tape and Reel Information – Tape Length and Label Placement



Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Recommended Solder Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: ENEPIG

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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