



QPA4536

24.2 – 26.5 GHz K-Band Power Amplifier

Product Overview

Qorvo QPA4536 is a K-Band Power Amplifier with integrated power detector. The QPA4536 operates from 24.2 – 26.5 GHz and is designed using Qorvo's power pHEMT production process.

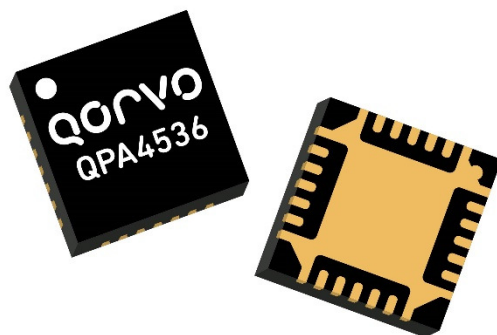
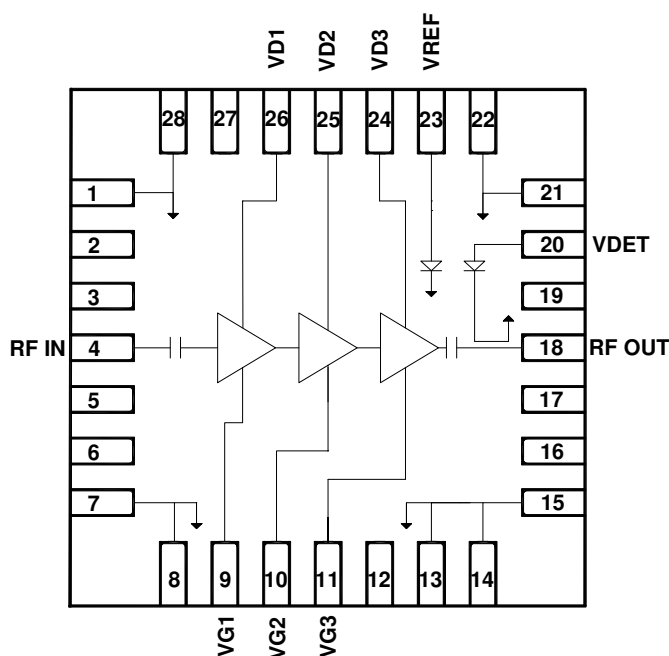
The QPA4536 typically provides 31.5 dBm output power at 1dB gain compression, and 33 dBm of saturated output power. The small signal gain is 18 dB, and Third Order Intercept is 43 dBm at 23 dBm SCL.

To simplify system integration, the QPA4536 is fully matched to 50 ohms with integrated DC clocking caps on both I/O ports.

The QPA4536 is available in a low-cost, surface mount 28 lead 5x5 mm QFN package. It is ideally suited for supporting communications and radar applications in both commercial and military markets.

Lead-free and RoHS compliant

Functional Block Diagram



Key Features

- Frequency Range: 24.2 – 26.5 GHz
- P_{1dB} ($P_{IN} \approx 14$ dBm): 31.5 dBm
- P_{SAT} ($P_{IN} = 18$ dBm): 32.5 dBm
- Small Signal Gain: 18 dB
- TOI ($P_{OUT}/Tone = 23$ dBm): 43 dBm
- Integrated Power Detector
- Bias: CW, $V_D = 6$ V, $I_{DQ} = 1430$ mA, $V_G = -0.6$ V typ.
- Package Dimensions: 5.0 x 5.0 x 1.3 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Applications

- Satellite Communications
- Point-to-Point Radio

Ordering Information

Part No.	Description
QPA4536TR7	250 pieces on a 7" reel (standard)
QPA4536EVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Rang
Drain to Gate Voltage, $V_D - V_G$	10 V
Drain Voltage (V_D)	6.5 V
Gate Voltage Range (V_G)	-3 V to 0 V
Drain Current (I_D)	3 A
Gate Current (I_G)	-14 to 110mA
Power Dissipation (P_{DISS}), $T_{BASE} = 85\text{ }^{\circ}\text{C}$	14 W
Input Power (P_{IN}), 50 Ω , CW, $V_D = 6\text{ V}$, $I_{DQ} = 1430\text{ mA}$, $T_{BASE} = 25\text{ }^{\circ}\text{C}$	25 dBm
Channel Temperature, T_{CH}	200 $^{\circ}\text{C}$
Mounting Temperature (30 seconds)	260 $^{\circ}\text{C}$
Storage Temperature	-55 to +150 $^{\circ}\text{C}$

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Drain Voltage (V_D)		6		V
Drain Current, Quiescent (I_D)		1430		mA
Drain Current, RF (I_{D_Drive})	See plot page 5, 6, 9			mA
Gate Voltage Typical Range (V_G)	-0.3	-0.9		V
Gate Current, RF (I_{G_Drive})	See plot page 5, 6			mA
Input Power ($P_{IN @ P_{1dB}}$)		14 ⁽¹⁾		
Operating Temp. Range T_{BASE} ⁽²⁾	-40		+85	$^{\circ}\text{C}$

- Limited by thermal; $P_{IN} > 14\text{ dBm}$ (where $P_{SAT} = 18\text{ dBm}$ P_{IN}) would degrade Median Lifetime, see p. 17
- T_{BASE} is back side of QPA4536

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

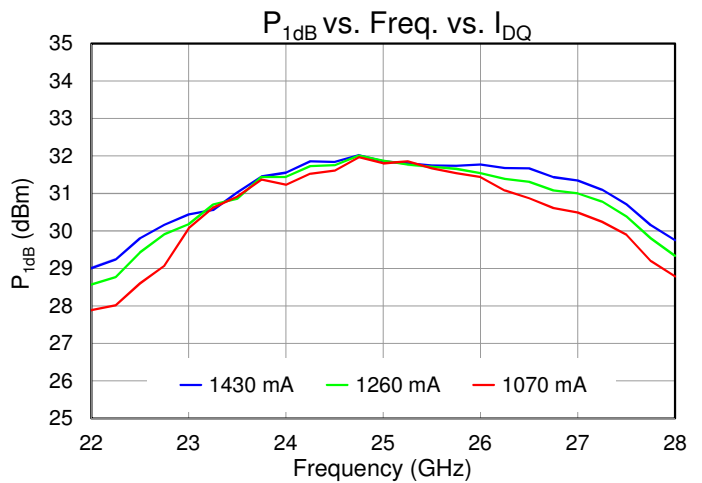
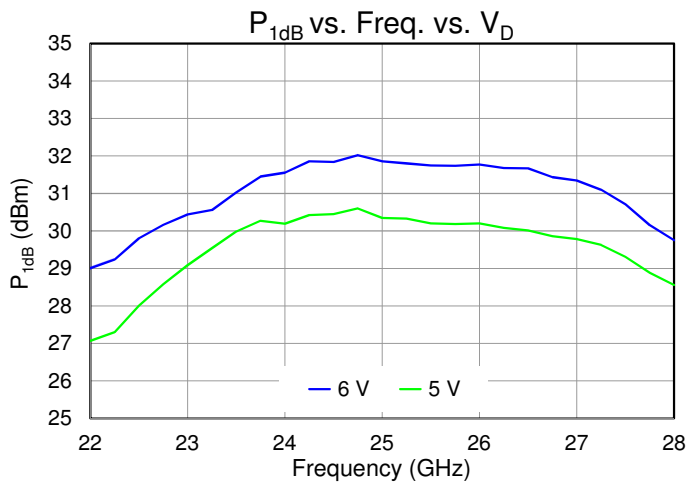
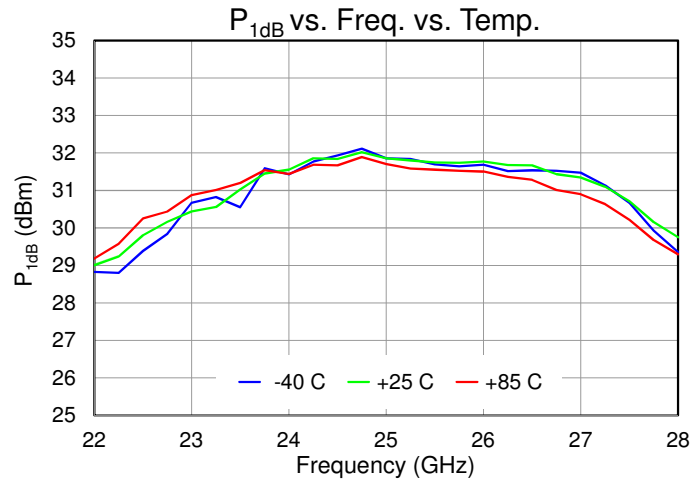
Parameter	Conditions ^{(1) (2)}	Freq. (GHz)	Min	Typ.	Max	Units
Operational Frequency Range			24.2		26.5	GHz
Output Power at 1dB Gain Compression, P_{1dB}	$P_{IN} \approx 14\text{ dBm}$			31.5		dBm
Output Power at Saturation, P_{SAT} ⁽³⁾	$P_{IN} = 18\text{ dBm} (\approx P_{5dB})$	24.2	32	33.0		dBm
		25.4	31	32.5		
		26.5	30	32.0		
Power Added Efficiency, PAE	$P_{IN} = 14\text{ dBm}$			12		%
Output TOI	$P_{OUT}/\text{Tone} = 23\text{ dBm}$, $\Delta F = 10\text{ MHz}$			43		dBm
Small Signal Gain, S21	$P_{IN} = -20\text{ dBm}$	24.2	18	19.5		dB
		25.4	16	18		
		26.5	14	16		
Input/Output Return Loss, IRL/ORL	$P_{IN} = -20\text{ dBm}$			7		dB
P_{1dB} Temperature Coefficient	$T_{DIFF} = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$			-0.005		dBm/ $^{\circ}\text{C}$
S21 Temperature Coefficient	$T_{DIFF} = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$			-0.02		dB/ $^{\circ}\text{C}$

Notes:

- Test conditions unless otherwise noted: CW, $V_D = 6\text{ V}$, $I_D = 1430\text{ mA}$, $V_G = -0.6\text{ V}$ +/- typical range, $T_{BASE} = 25^{\circ}\text{C}$, $Z_0 = 50\text{ }\Omega$
- T_{BASE} is back side of QPA4536
- Limited by thermal; operating at P_{SAT} would degrade Median Lifetime (T_M) for $T_{BASE} = 85^{\circ}\text{C}$; see page 17. Recommended reducing T_{BASE} to improve T_M .

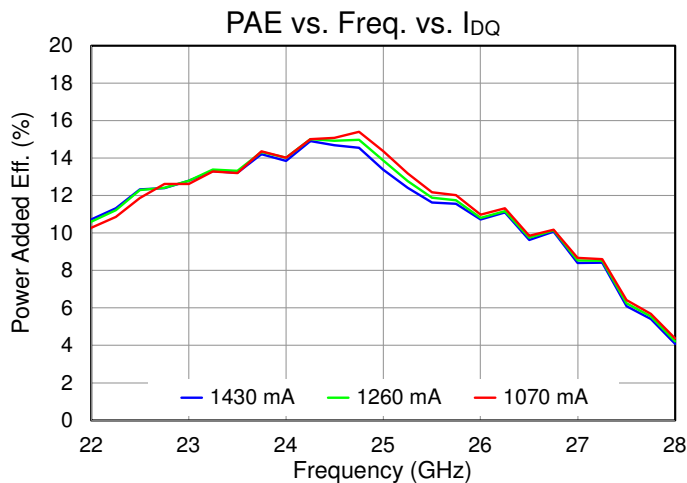
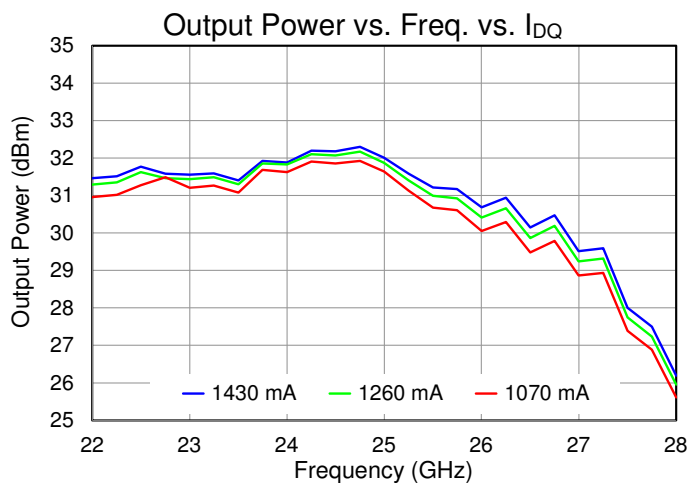
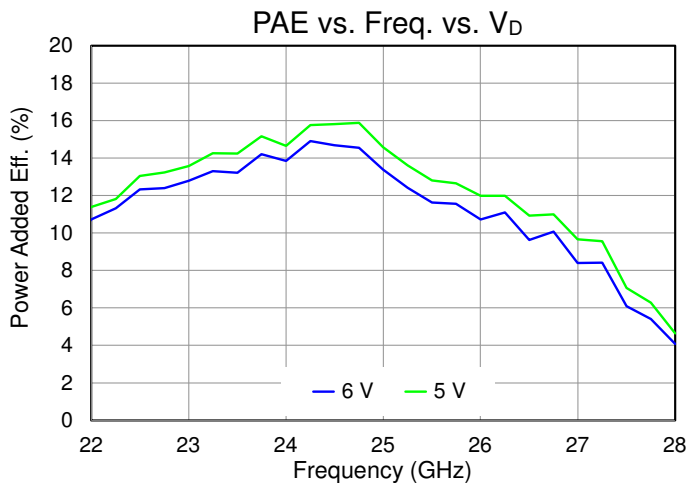
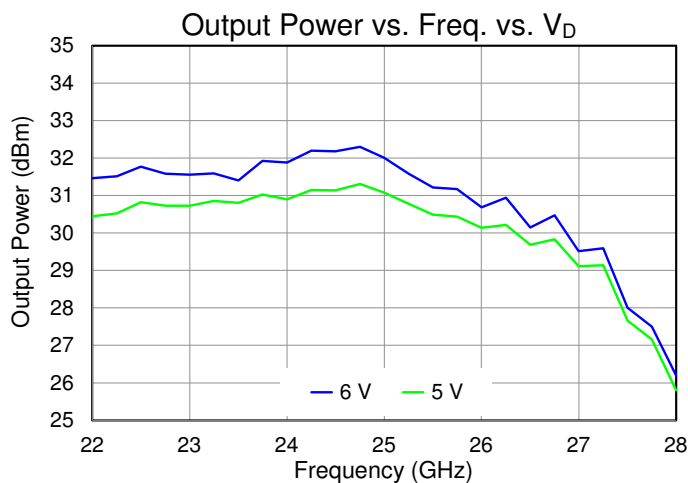
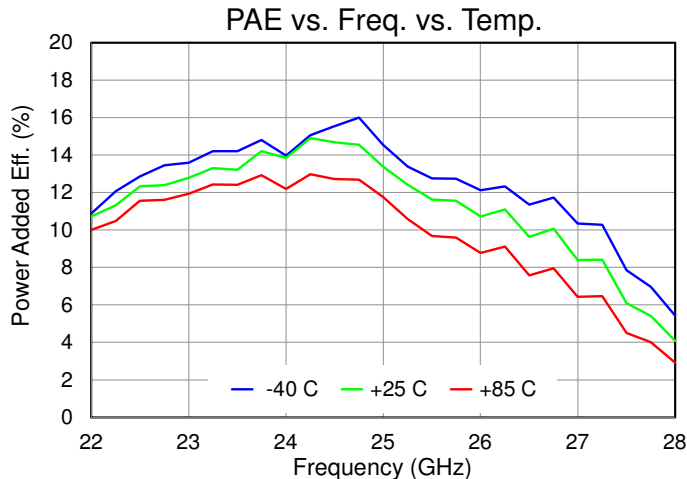
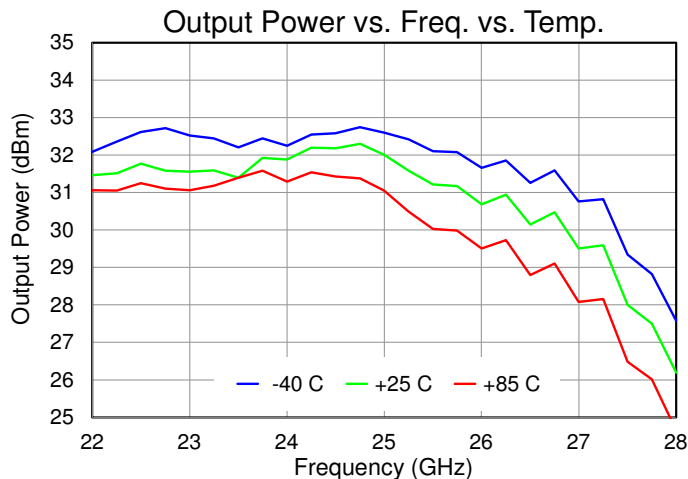
Performance Plots – Large Signal

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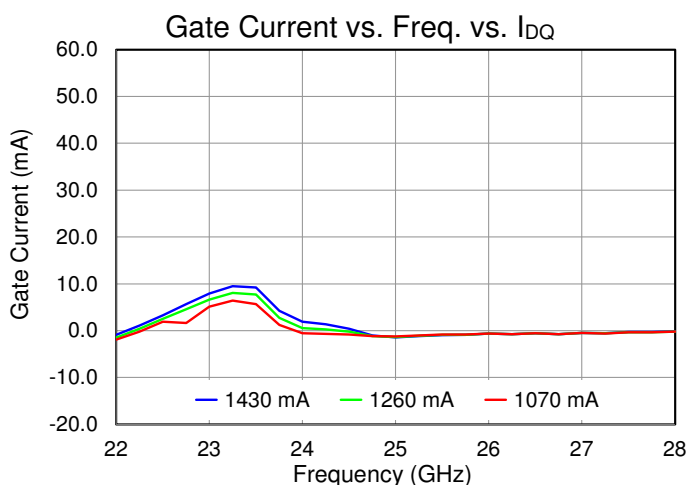
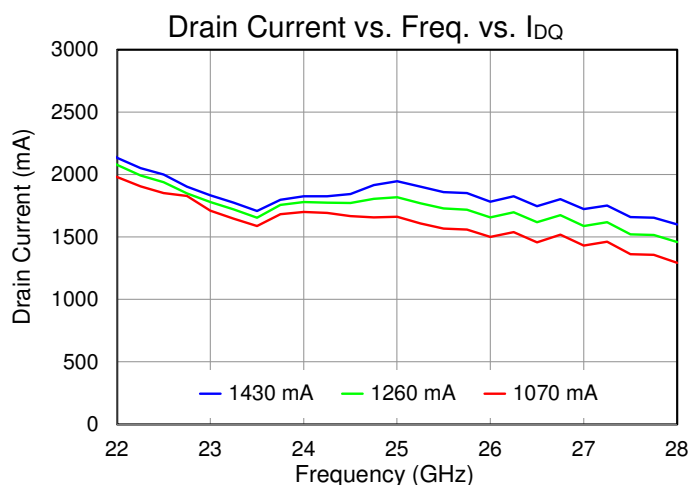
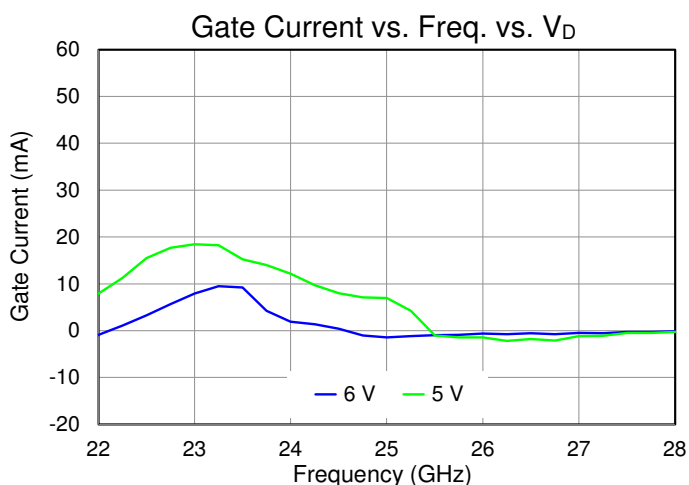
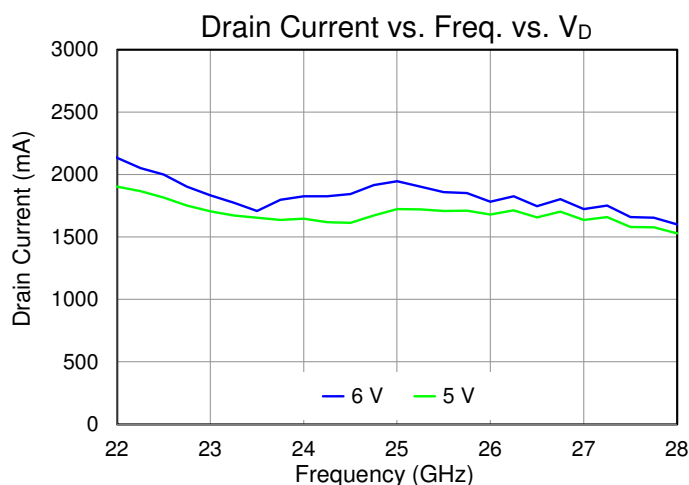
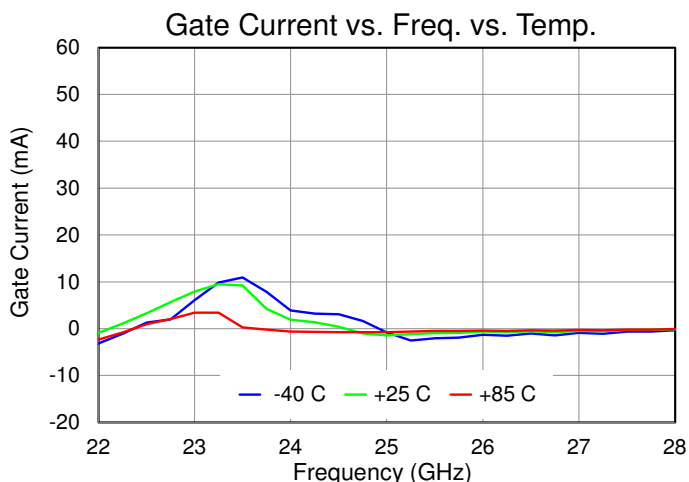
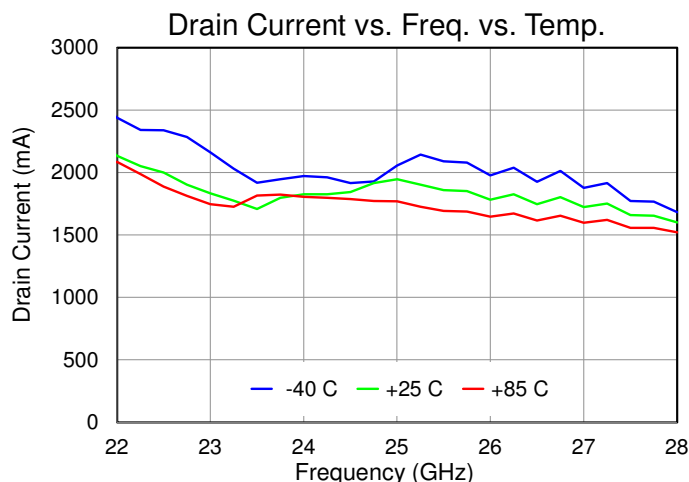
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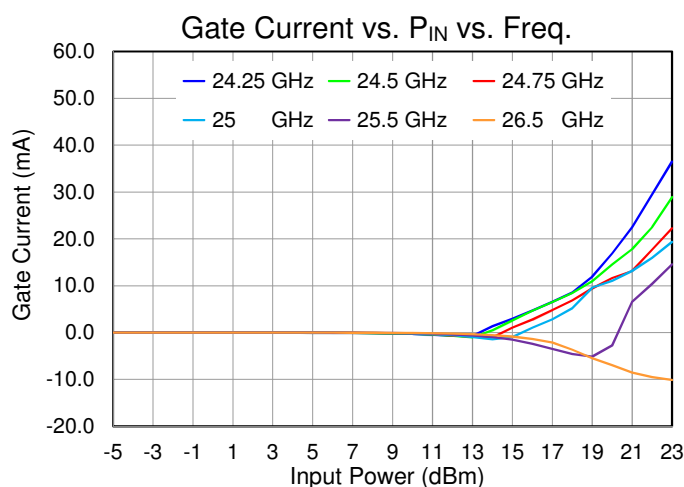
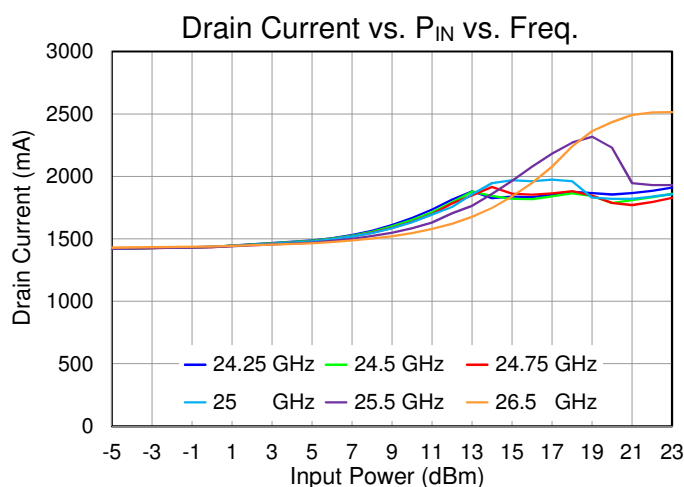
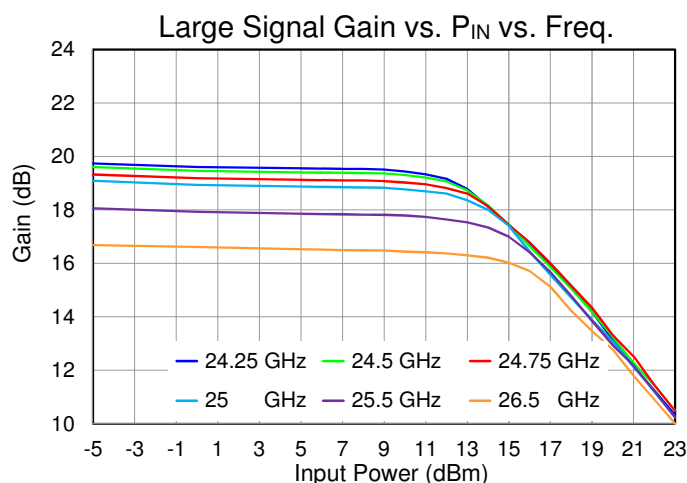
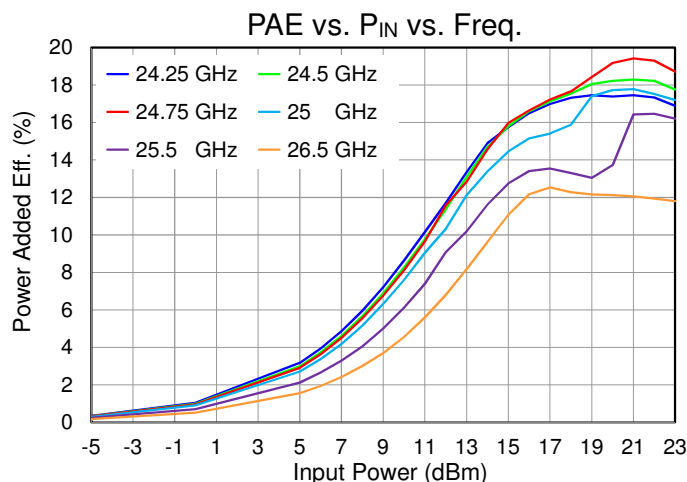
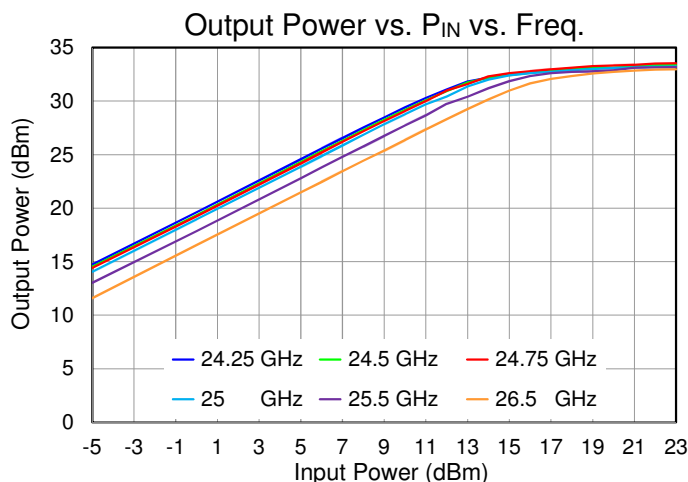
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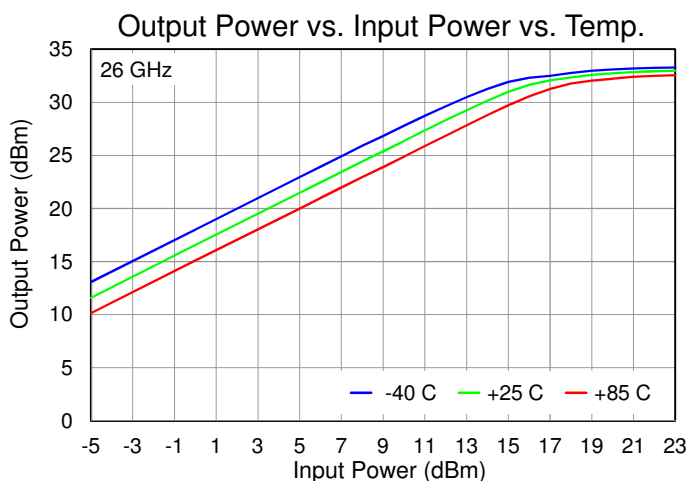
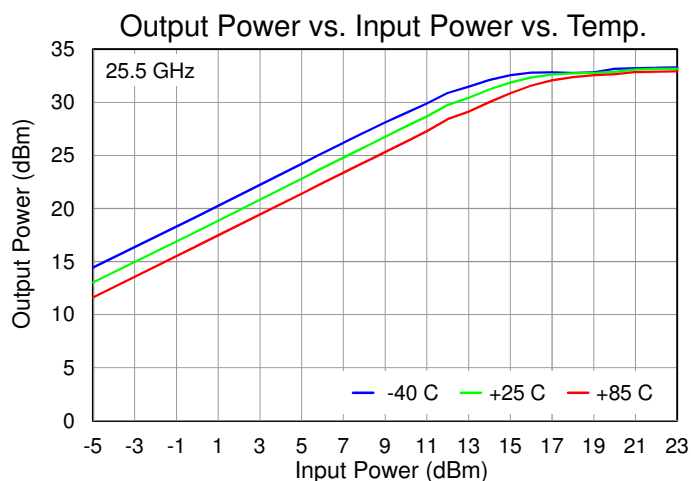
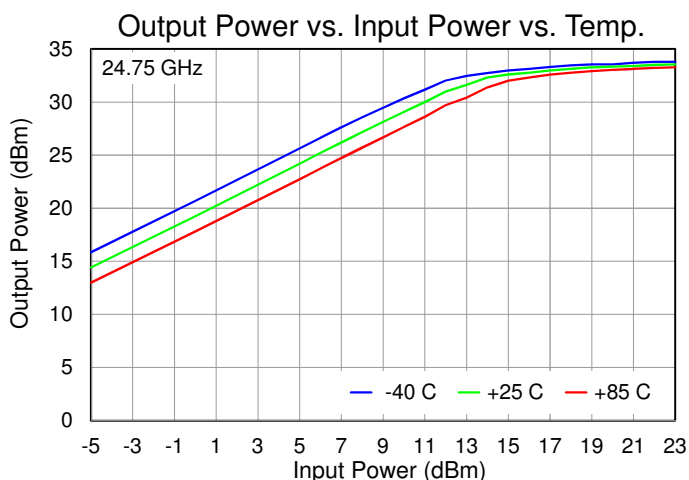
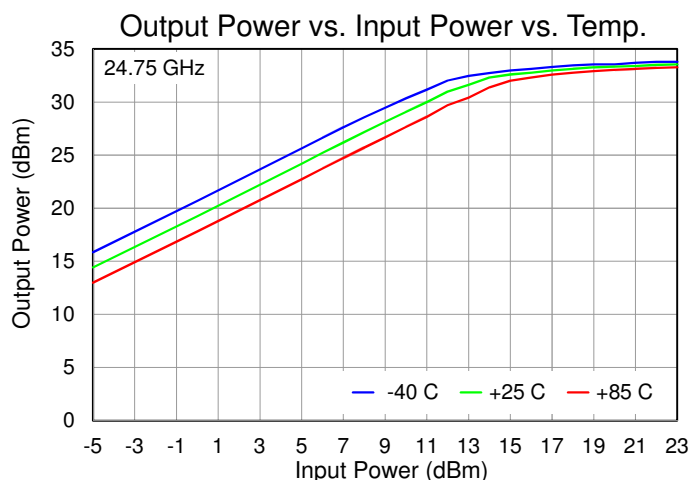
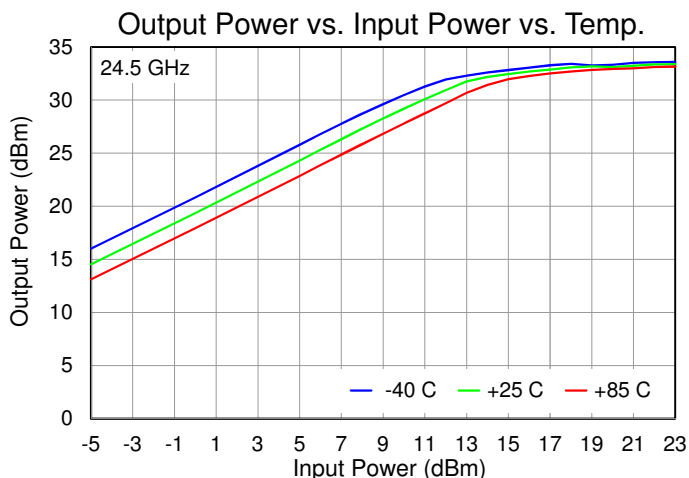
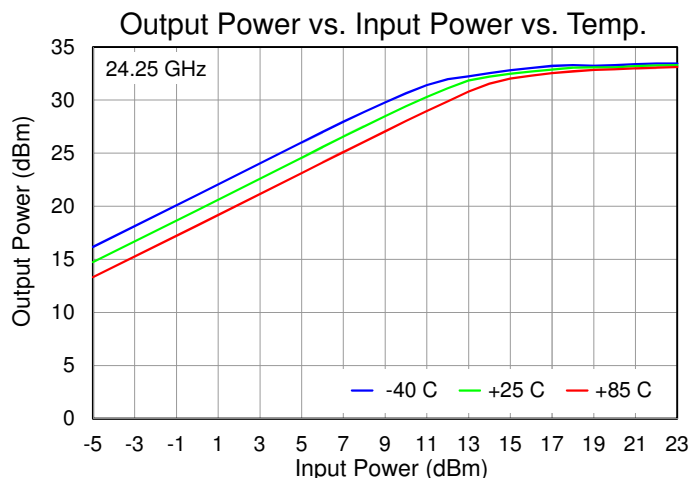
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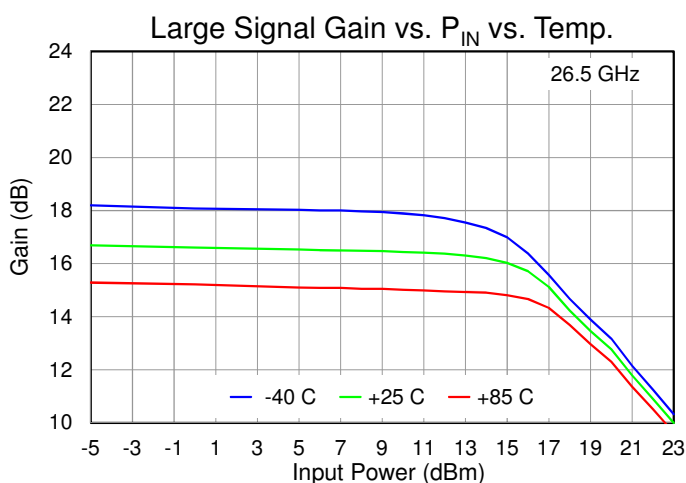
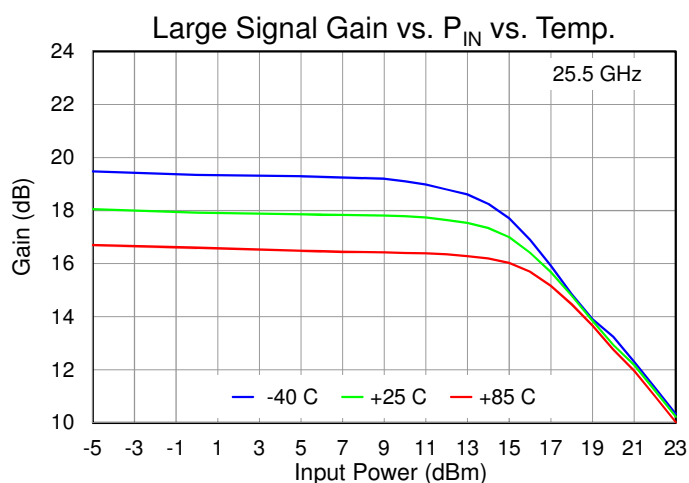
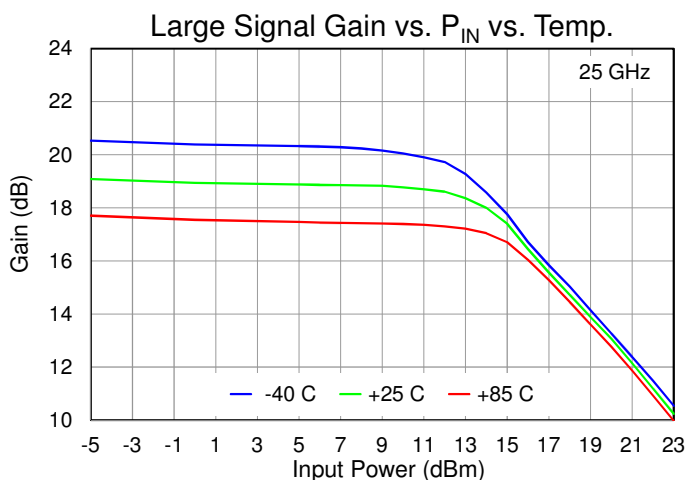
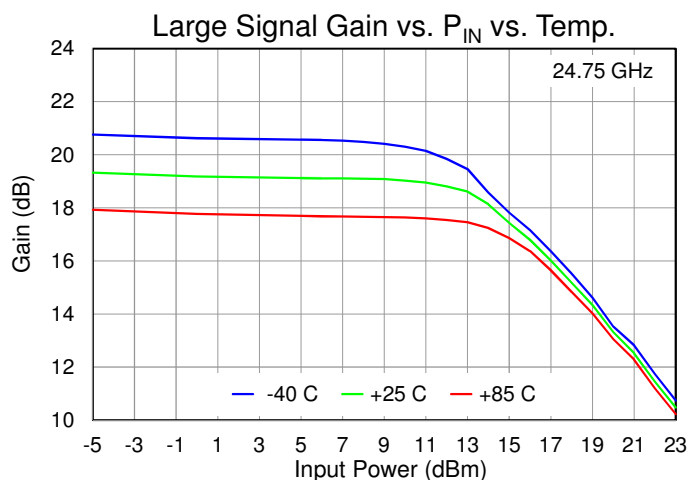
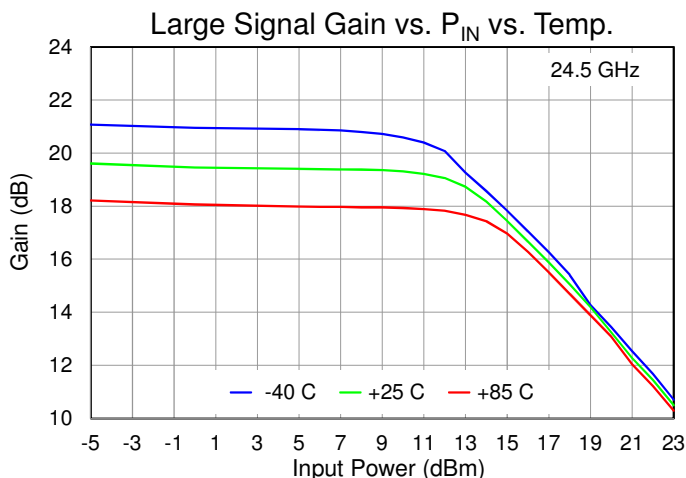
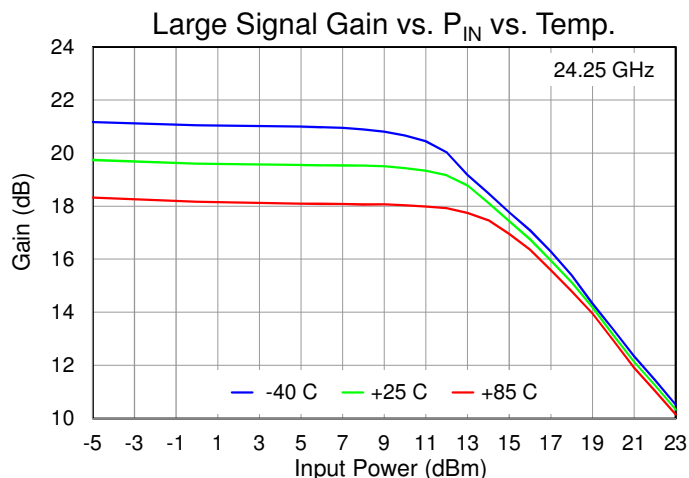
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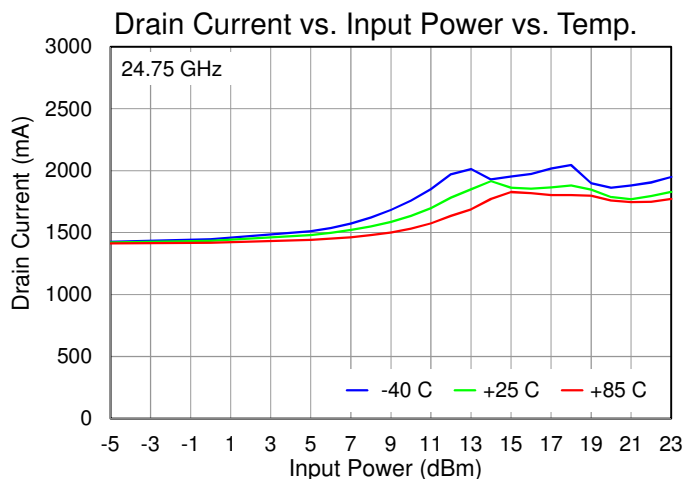
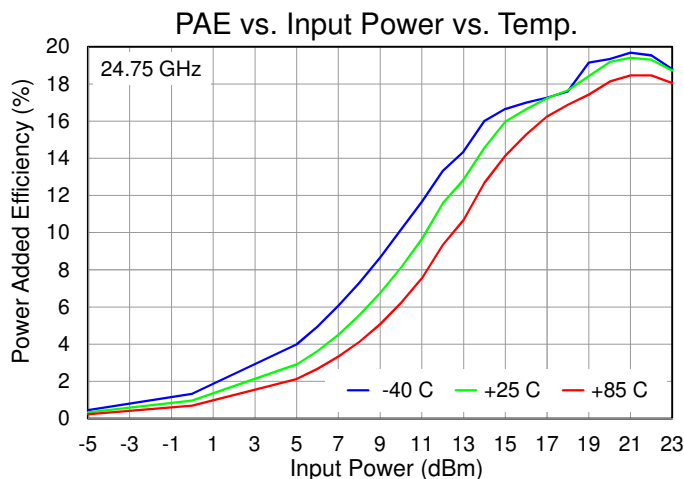
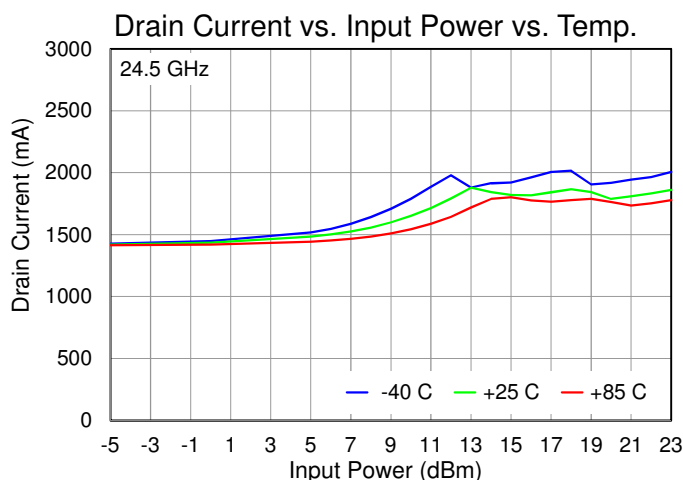
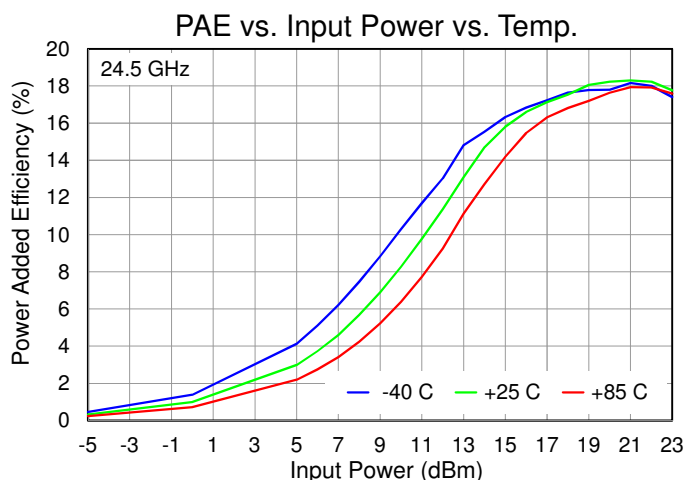
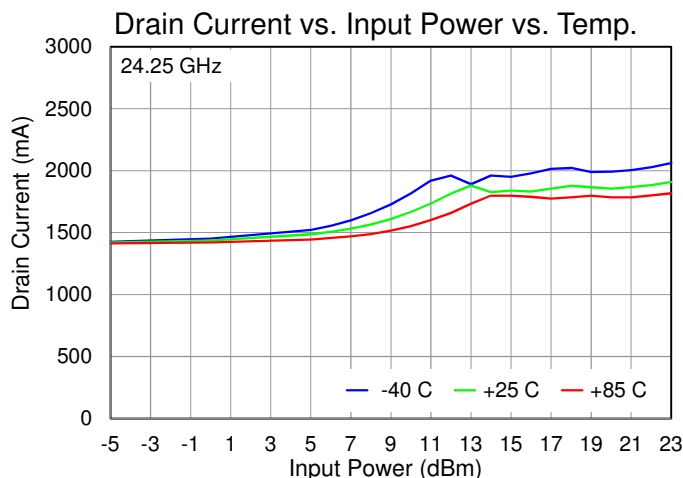
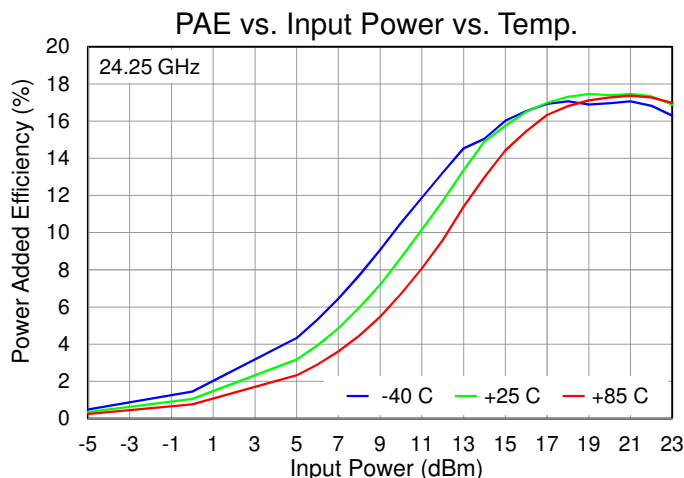
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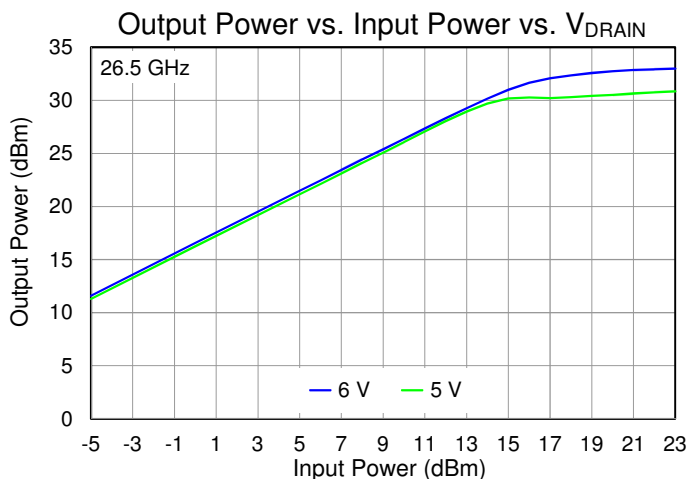
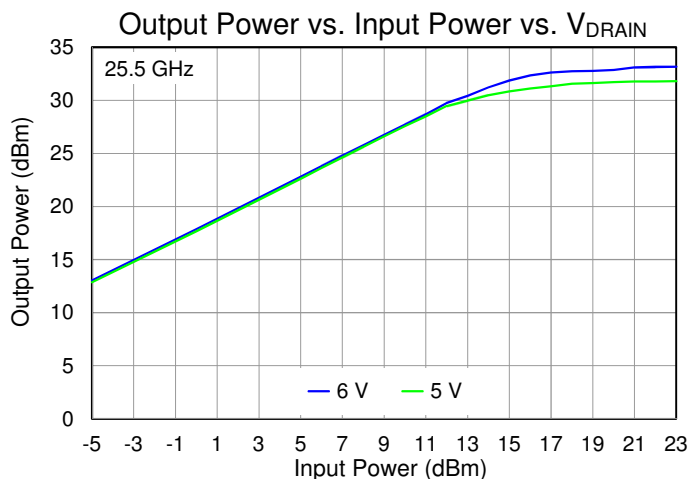
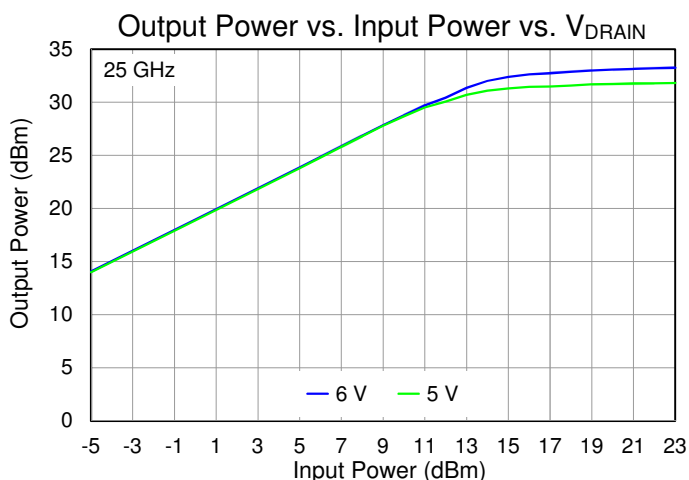
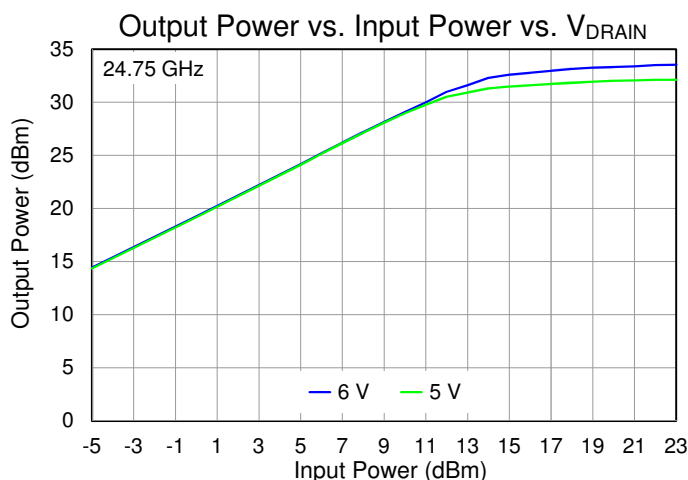
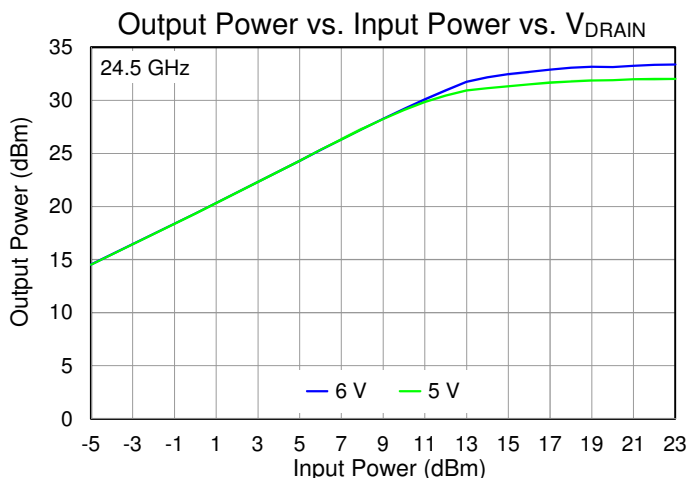
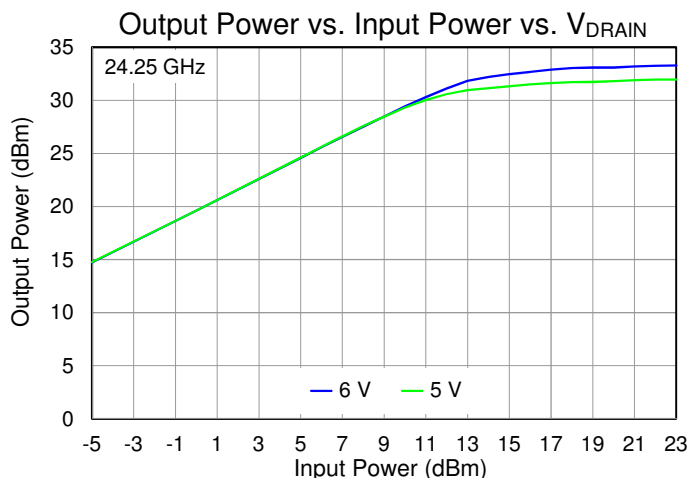
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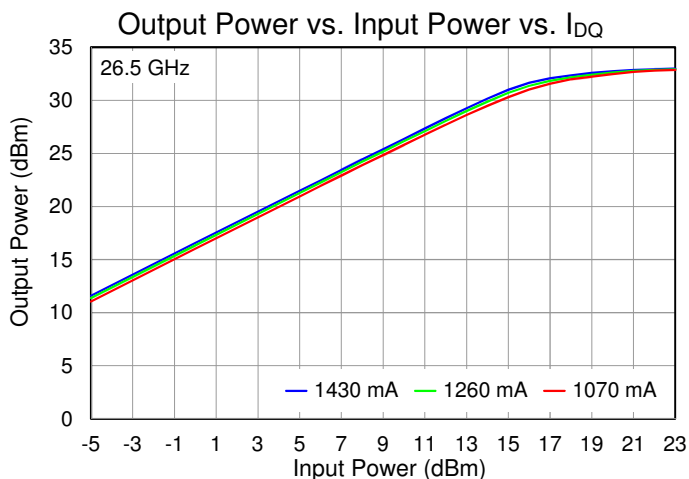
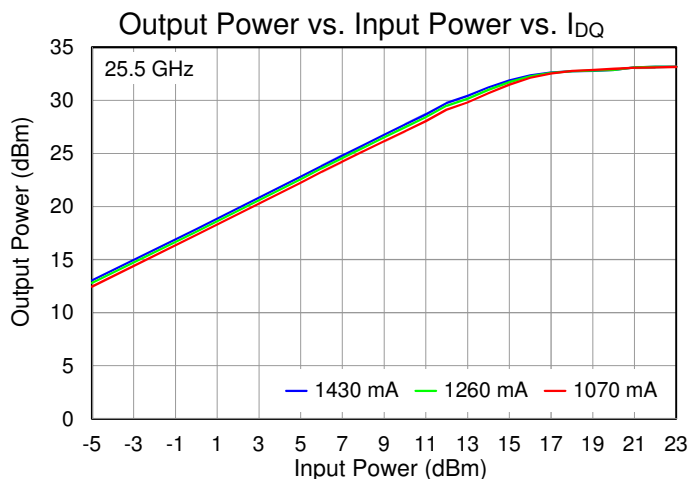
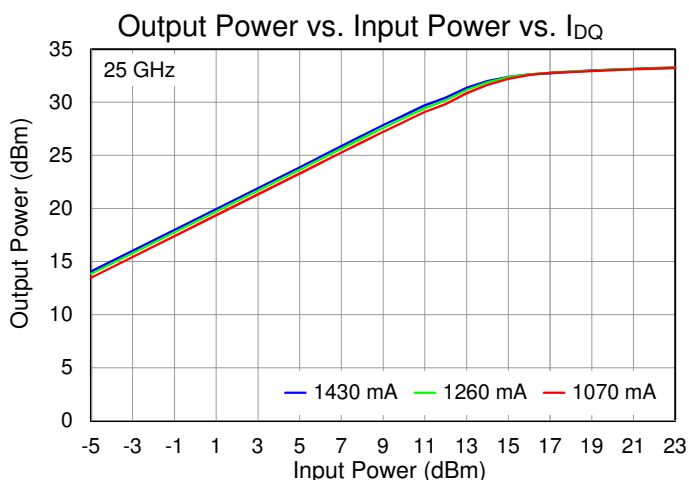
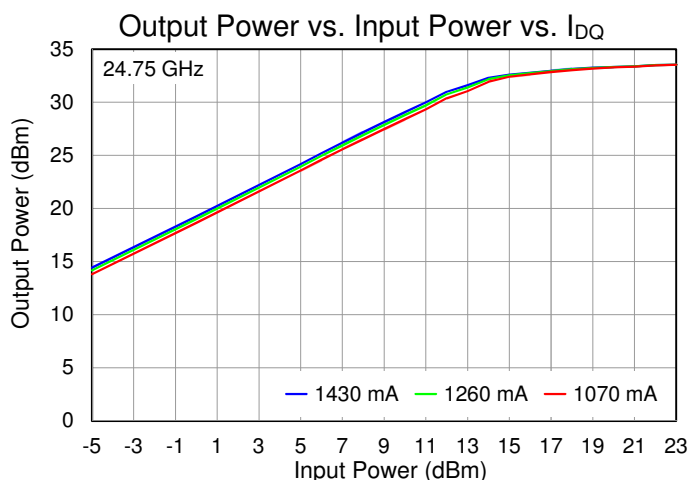
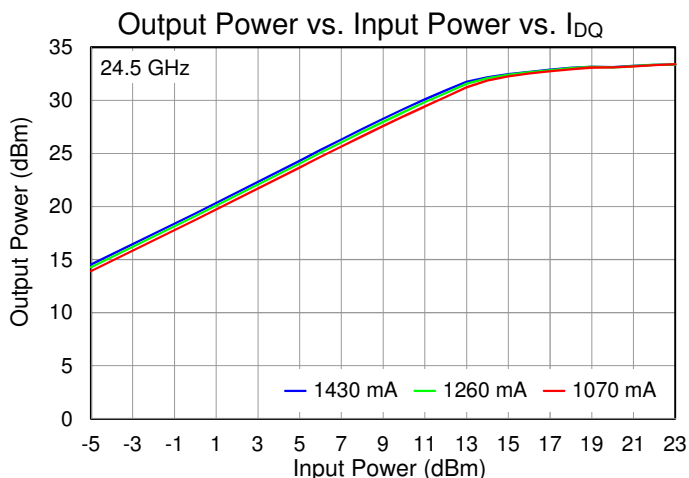
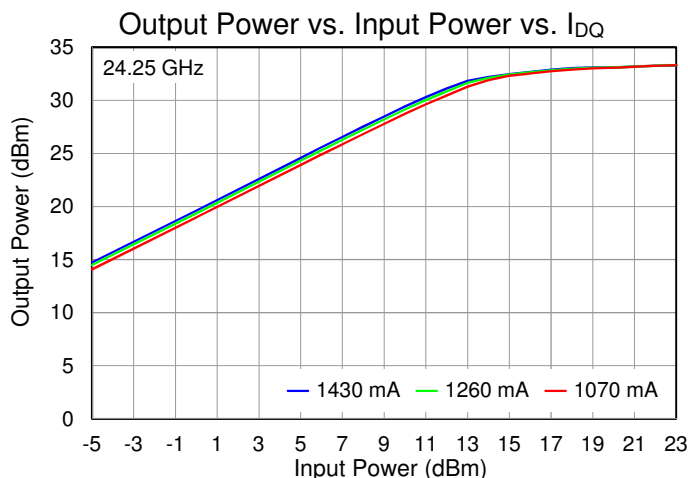
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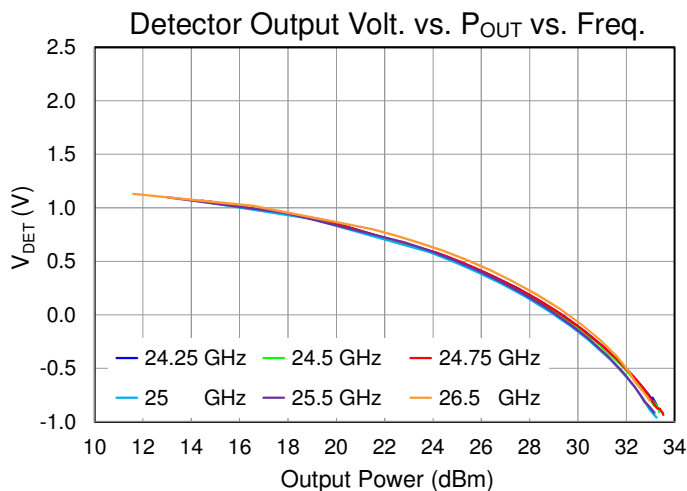
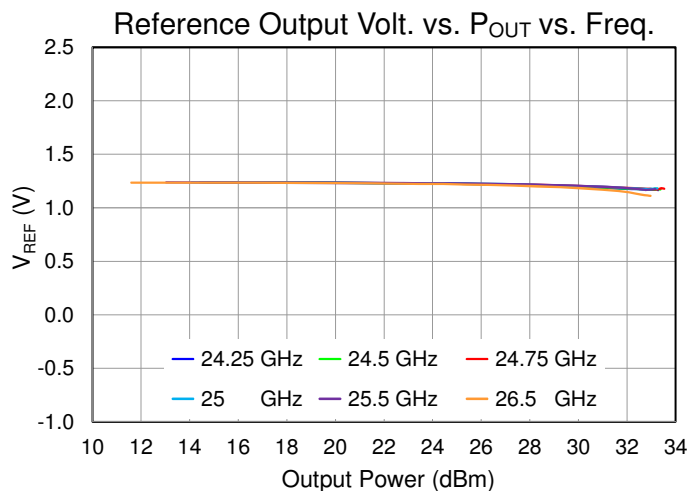
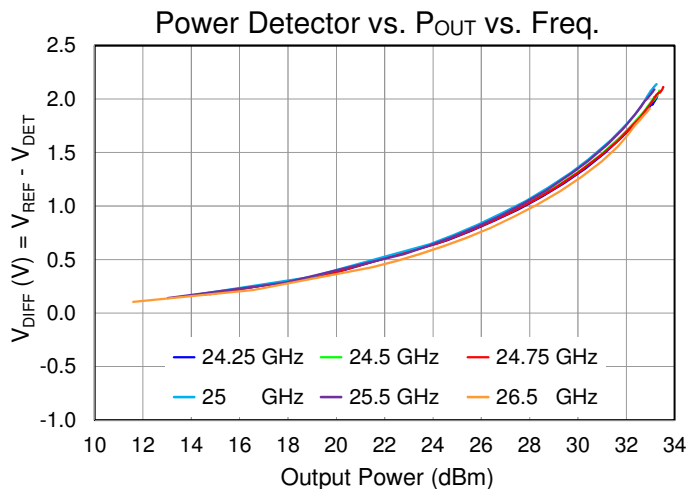
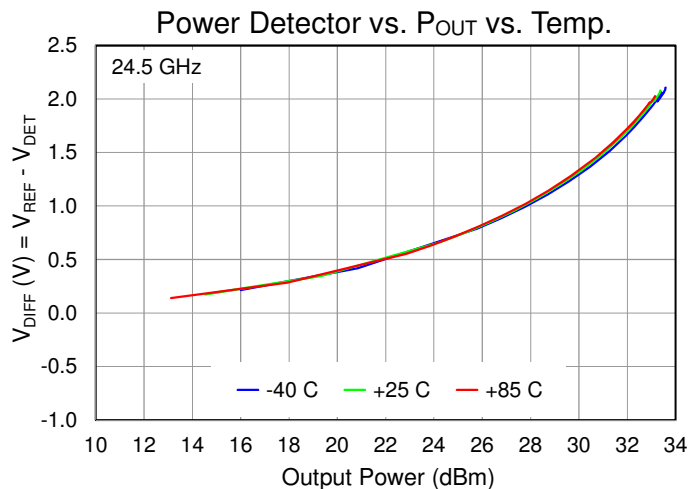
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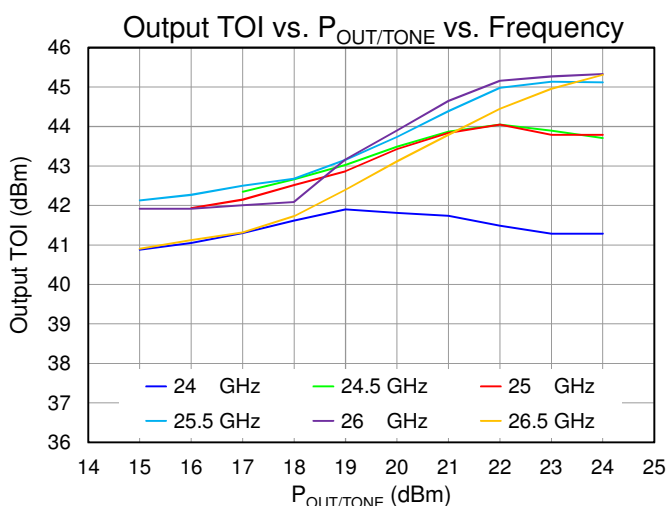
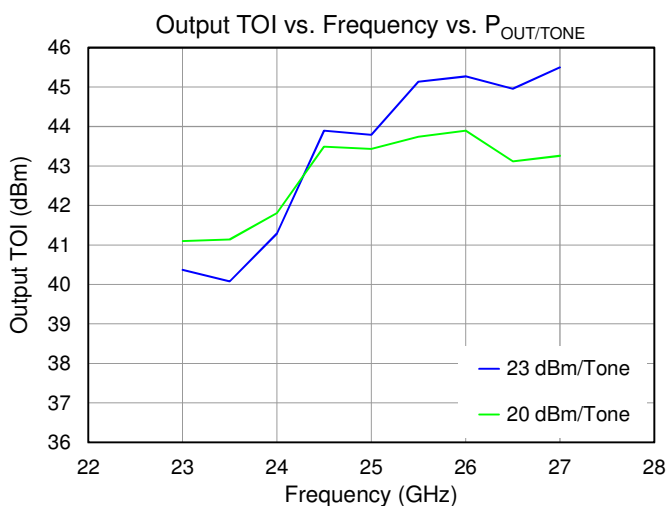
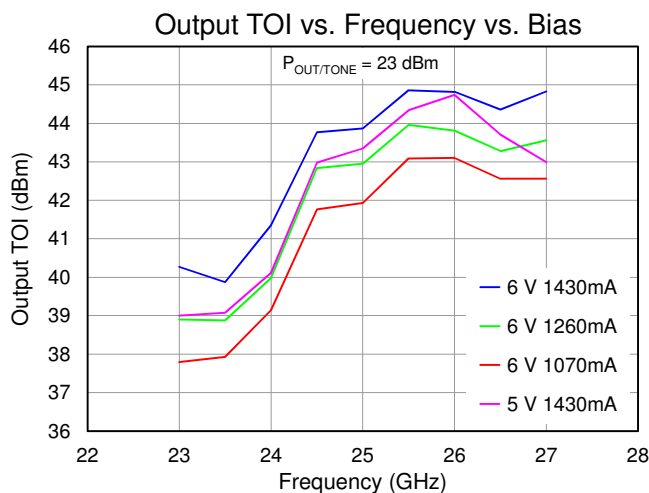
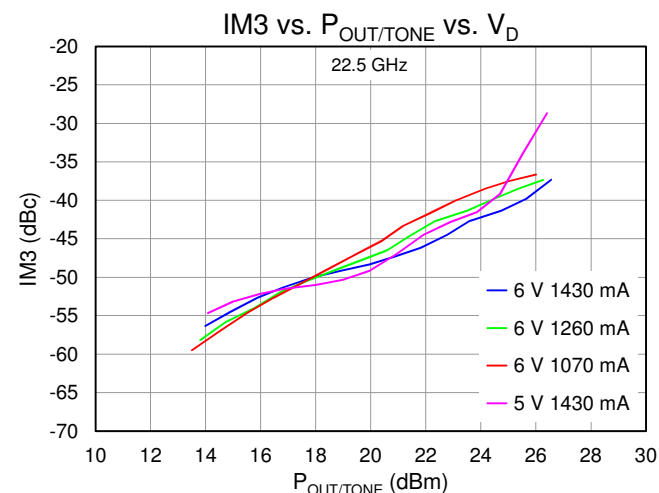
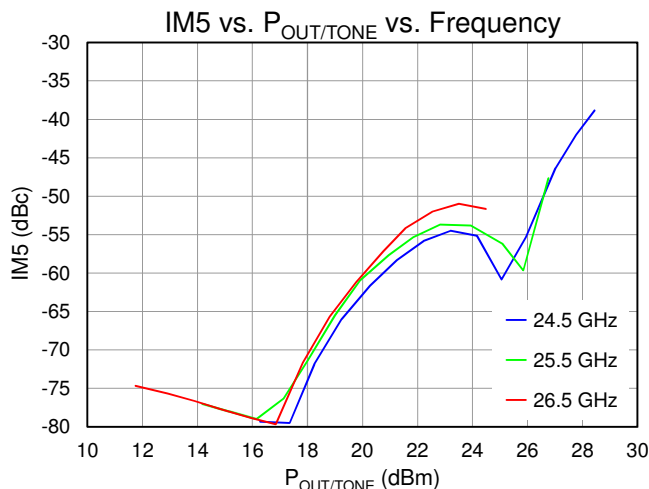
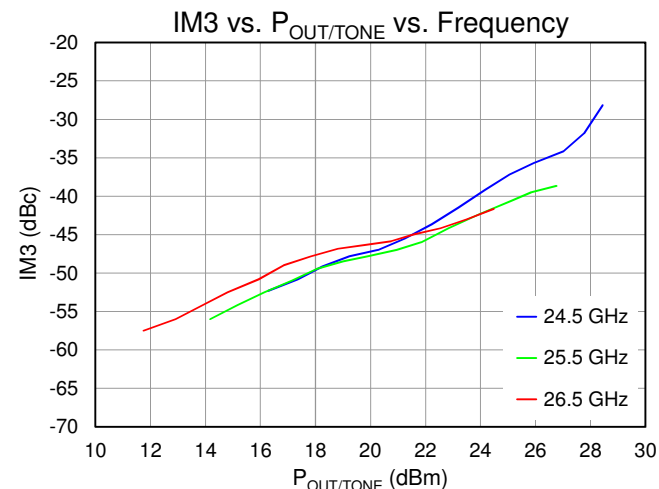
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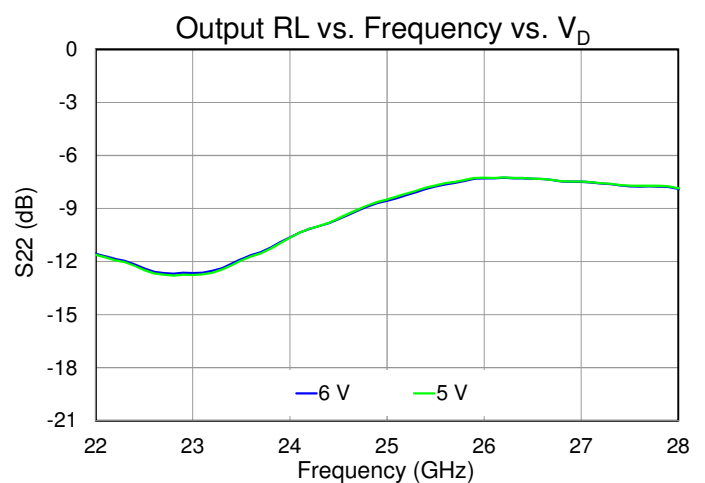
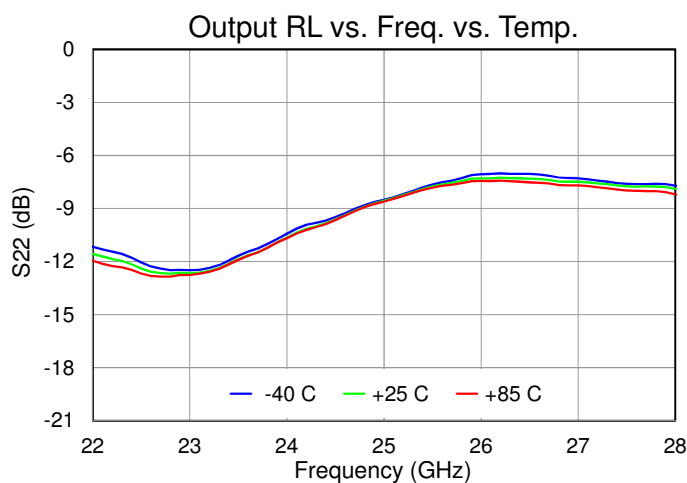
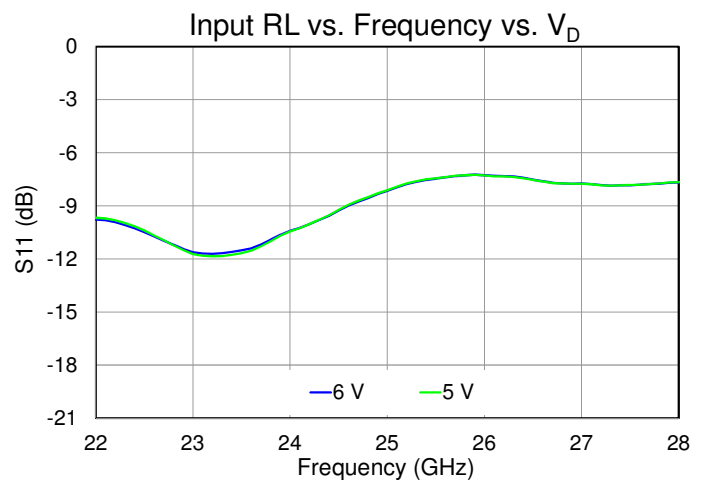
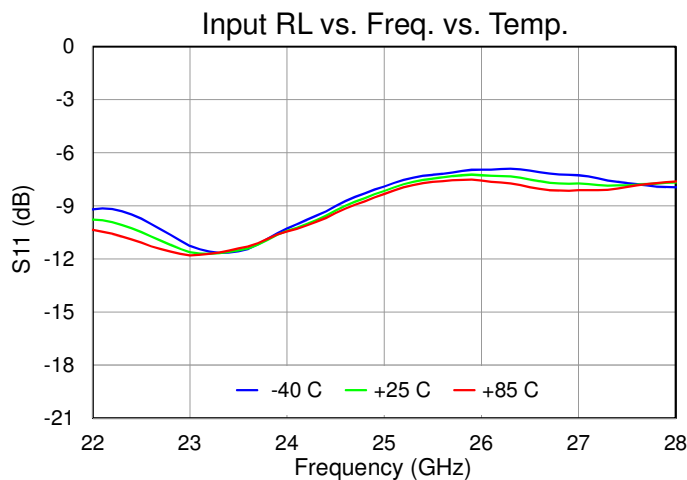
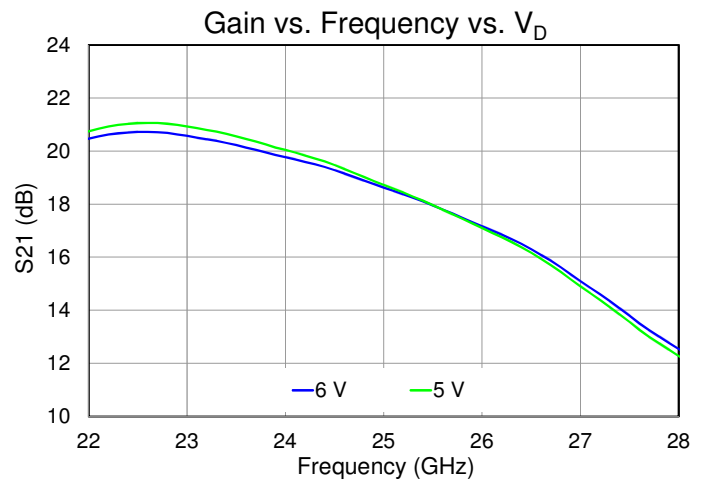
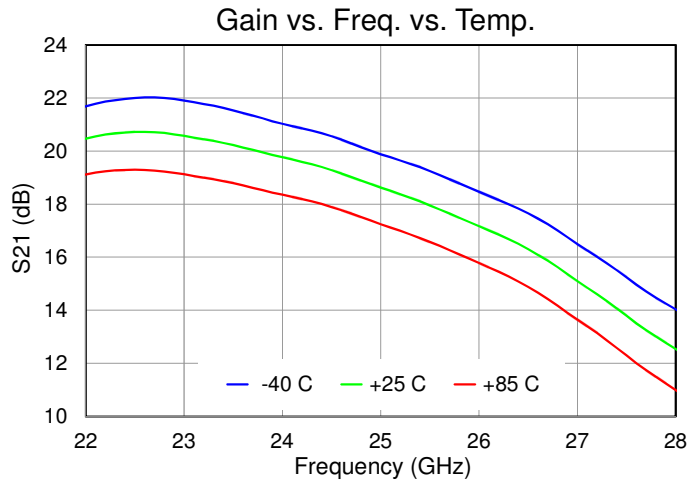
Performance Plots – Linearity

Test conditions, unless otherwise noted: CW, $V_D = 6\text{ V}$, $I_{DQ} = 1430\text{ mA}$, $\Delta f = 10\text{ MHz}$, $T_{BASE} = +25\text{ }^\circ\text{C}$ (T_{BASE} is backside of QPA4536)



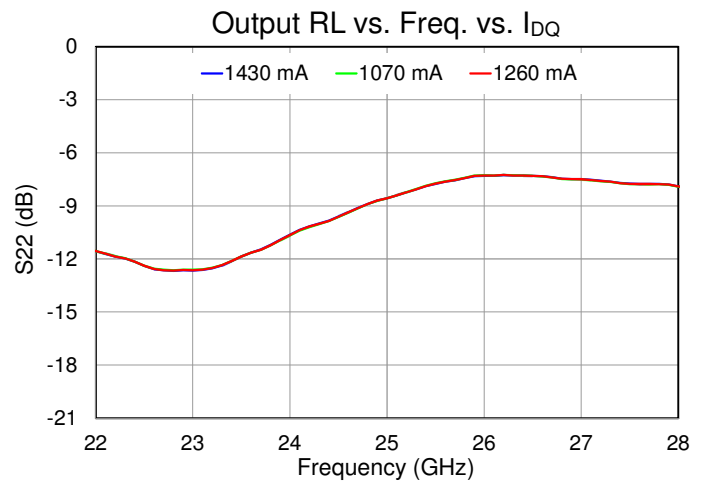
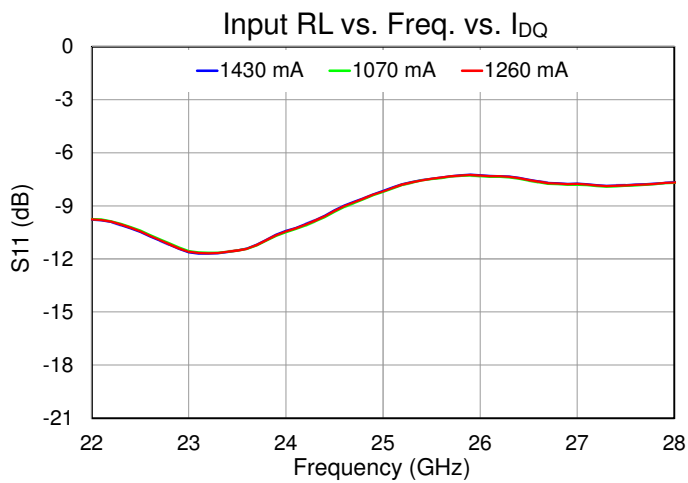
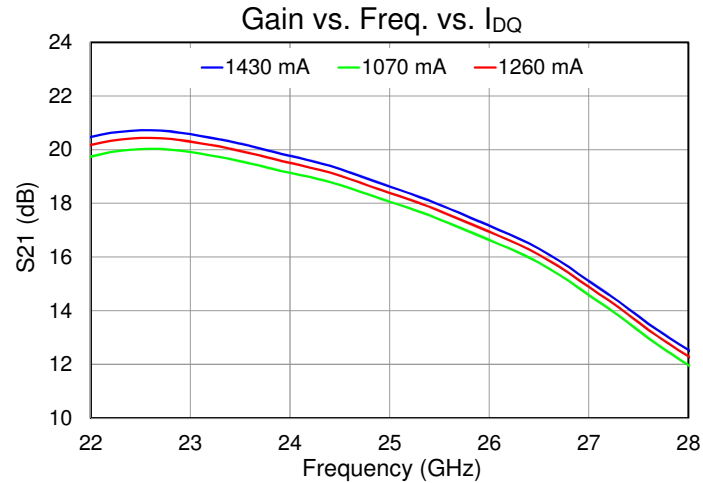
Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW, $V_D = 6\text{ V}$, $I_{DQ} = 1430\text{ mA}$, $P_{IN} = -20\text{ dBm}$, $T_{BASE} = +25\text{ }^{\circ}\text{C}$ (T_{BASE} is backside of QPA4536)



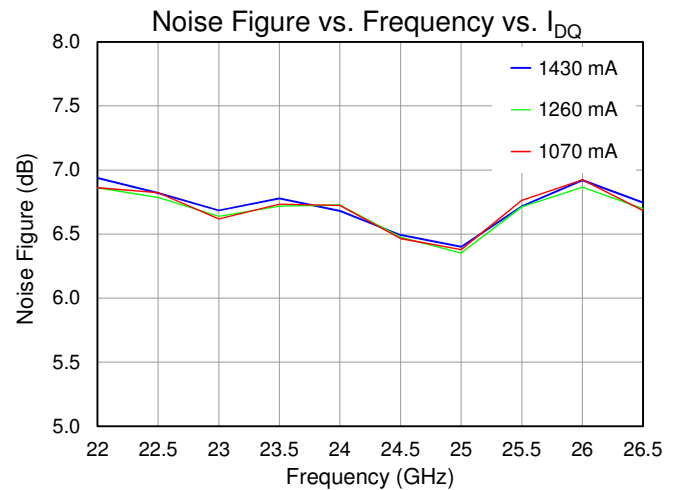
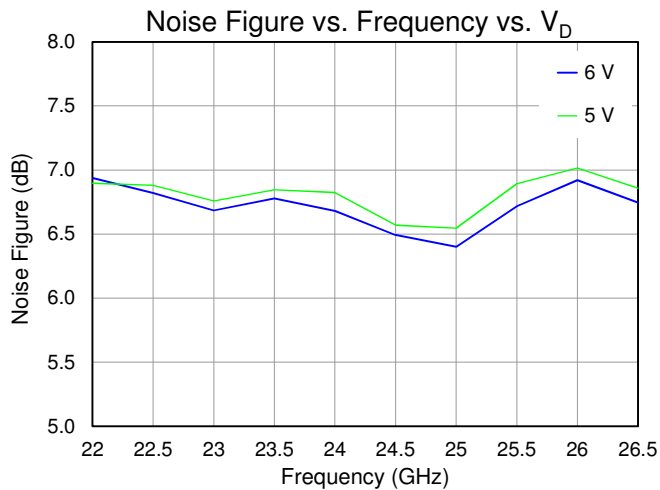
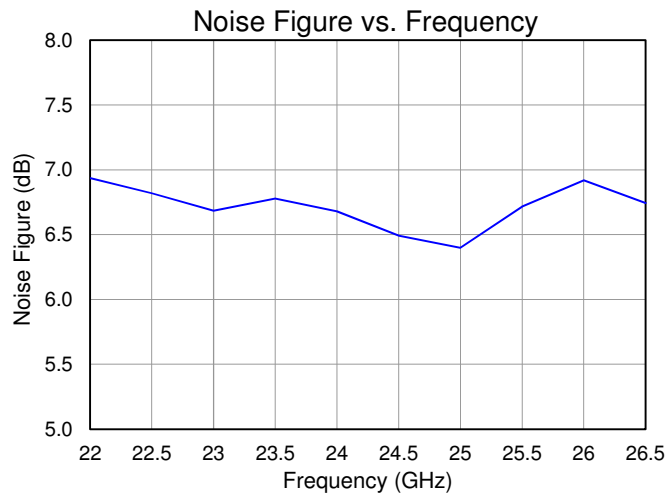
Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW, $V_D = 6\text{ V}$, $I_{DQ} = 1430\text{ mA}$, $P_{IN} = -20\text{ dBm}$, $T_{BASE} = +25\text{ }^{\circ}\text{C}$ (T_{BASE} is backside of QPA4536)



Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW, $V_D = 6\text{ V}$, $I_{DQ} = 1430\text{ mA}$, $T_{BASE} = +25\text{ }^{\circ}\text{C}$ (T_{BASE} is backside of QPA4536)



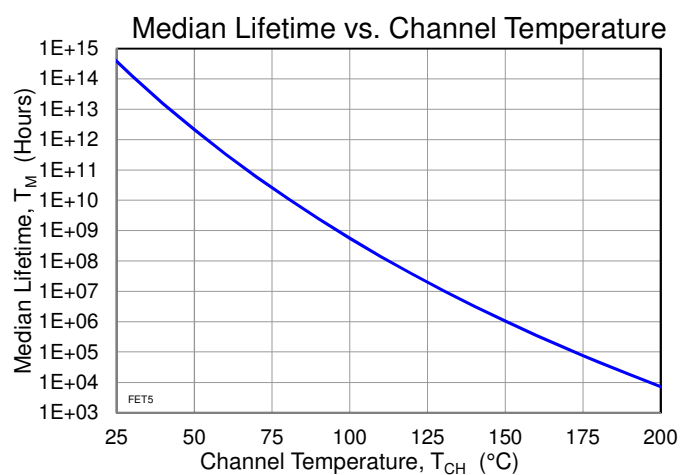
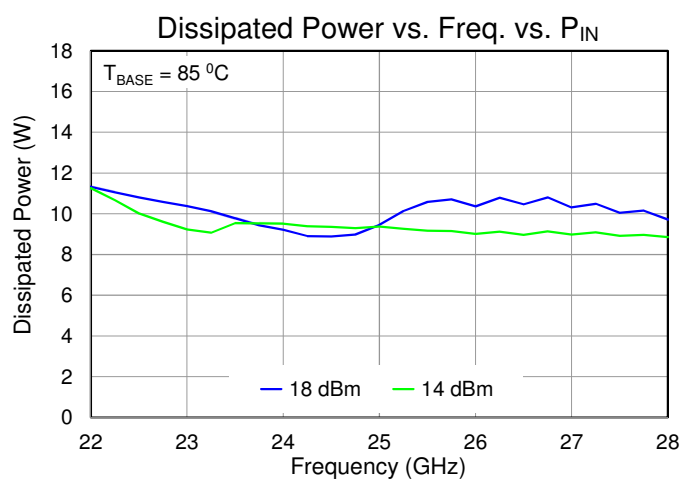
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} ⁽¹⁾	Quiescent, no RF	7.79	$^{\circ}\text{C}/\text{W}$
Channel Temperature, T_{CH}	$T_{BASE} = 85^{\circ}\text{C}$, $V_D = 6\text{ V}$, $I_{DQ} = 1430\text{ mA}$, $P_{DISS} = 8.6\text{ W}$	152	$^{\circ}\text{C}$
Thermal Resistance, θ_{JC} ⁽¹⁾	$P_{IN} = 14\text{ dBm}$, $T_{BASE} = 85^{\circ}\text{C}$, CW, $V_D = 6\text{ V}$, $I_{DQ} = 1430\text{ mA}$, Freq = 24.5 GHz, $I_{D_DRIVE} = 1790\text{ mA}$, $P_{OUT} (P_{1dB}) = 31.5\text{ dBm}$, $P_{DISS} = 9.4\text{ W}$	7.86	$^{\circ}\text{C}/\text{W}$
Channel Temperature, T_{CH}		159	$^{\circ}\text{C}$
Thermal Resistance, θ_{JC} ⁽¹⁾	$P_{IN} = 18\text{ dBm}$ ⁽²⁾ , $T_{BASE} = 85^{\circ}\text{C}$ ⁽²⁾ , CW, $V_D = 6\text{ V}$, $I_{DQ} = 1430\text{ mA}$, Freq = 26.25 GHz, $I_{D_DRIVE} = 2055\text{ mA}$, $P_{OUT} (P_{SAT}) = 32\text{ dBm}$, $P_{DISS} = 10.8\text{ W}$	7.96	$^{\circ}\text{C}/\text{W}$
Channel Temperature, T_{CH}		171	$^{\circ}\text{C}$

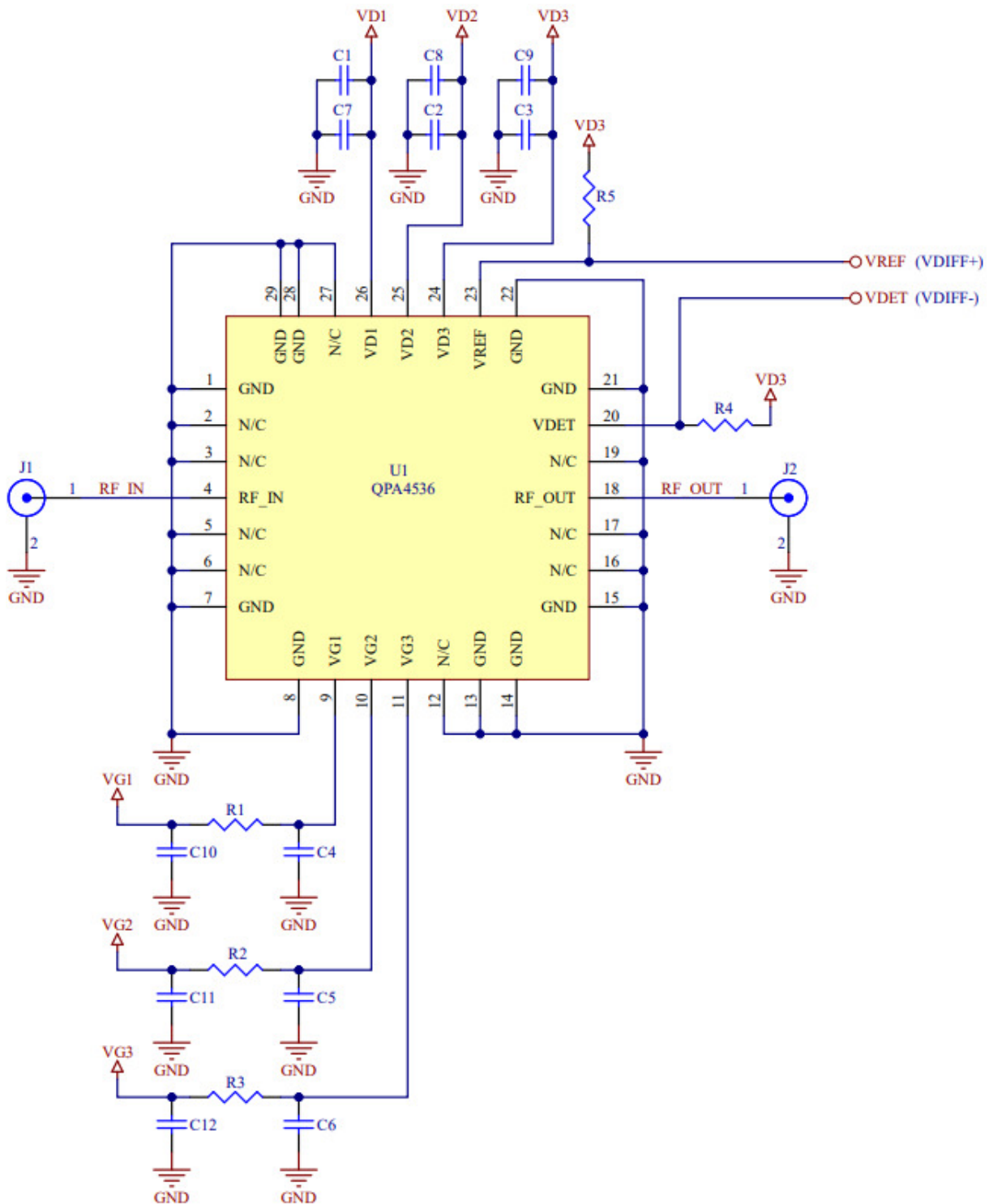
Notes:

- Thermal resistance determined to T_{BASE} (T_{BASE} is backside of QPA4536)
- Limited by thermal; operating at P_{SAT} ($P_{IN} = 18\text{ dBm}$) would degrade Median Lifetime (T_M); see plot below. Recommended reducing T_{BASE} to improve T_M .

Dissipated Power

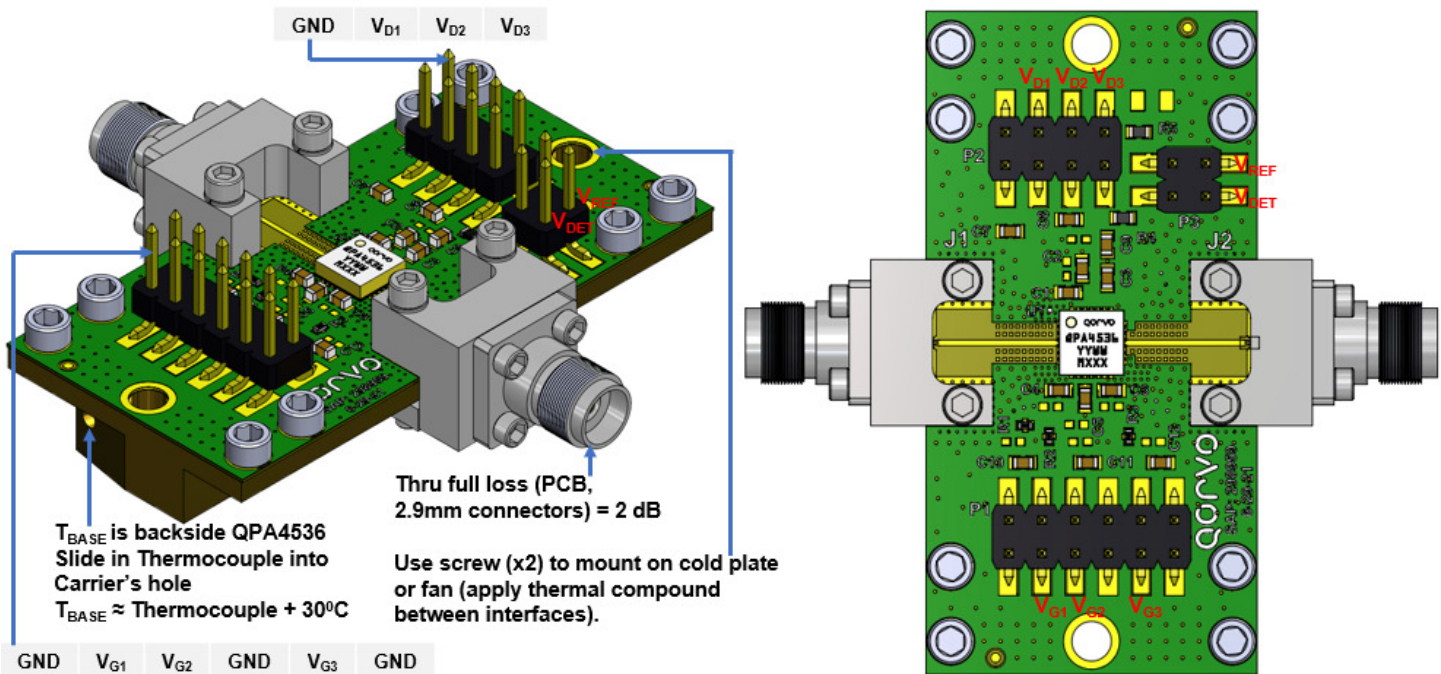


Applications Information



Combined $V_D = V_{D1} + V_{D2} + V_{D3}$, $V_G = V_{G1} + V_{G2} + V_{G3}$
See BOM page 20

Evaluation Board (EVB) Layout



Qorvo
SAP: 298959
6-29-21

LAYER STACK LEGEND

Material	Layer	Thickness	Dielectric	Material Type
Surface Material	Top Overlay	0.0010in	Solder Resist	Legend
Copper	Top Layer	0.0007in		Signal
Prepreg		0.0080in	ROGERS 4003C	Dielectric
Copper	Bottom Layer	0.0007in		Signal

Recommend Cu-filled or Epoxy-filled Vias

Finished board thickness: 0.0104in

Bill of Materials

Reference Des.	Qty	Value	Description	Part Number
C1 – C12	12	0.01 uF	CAP, 1uF, ±10%, 50V, X7R, 0603	
R1 – R3	3	10 Ω	RES, 10 Ohm, ±1%, 1/16W, 0402	
R4, R5	2	24K Ω	RES, 24K Ohm, ±5%, 1/10W, 0603	
PCB	1		PCB, see page 19	Qorvo, Custom
H1	1		CONN, HDR, 8 POS, Dual, SMD	
H2	1		CONN, HDR, 4 POS, 2 RAW, SMD, Au	
H3	1		CONN, HDR, ST, 2x6, 0.100", SMD	
J1, J2	2		Connector, RF 2.92mm, F, Pin 0.007, Dielectric 0.039	Southwest Microwave 1092-04A-12
H-Block	1		H-Block, Copper C110, 1 x 2 x 0.0275T in	Qorvo, Custom
S1 – S8	8		Screw, Cap, Socket Head, 2-56X1/8"	
Solder Preform			Preform, Solder (SAC305) 1 x 1 x 0.002 in	
Solder			Paste, solder, Syntech, Sn63/Pb37	
TC			Thermal Compound, Silver 5GR	Artic Silver 5 AS5-5G

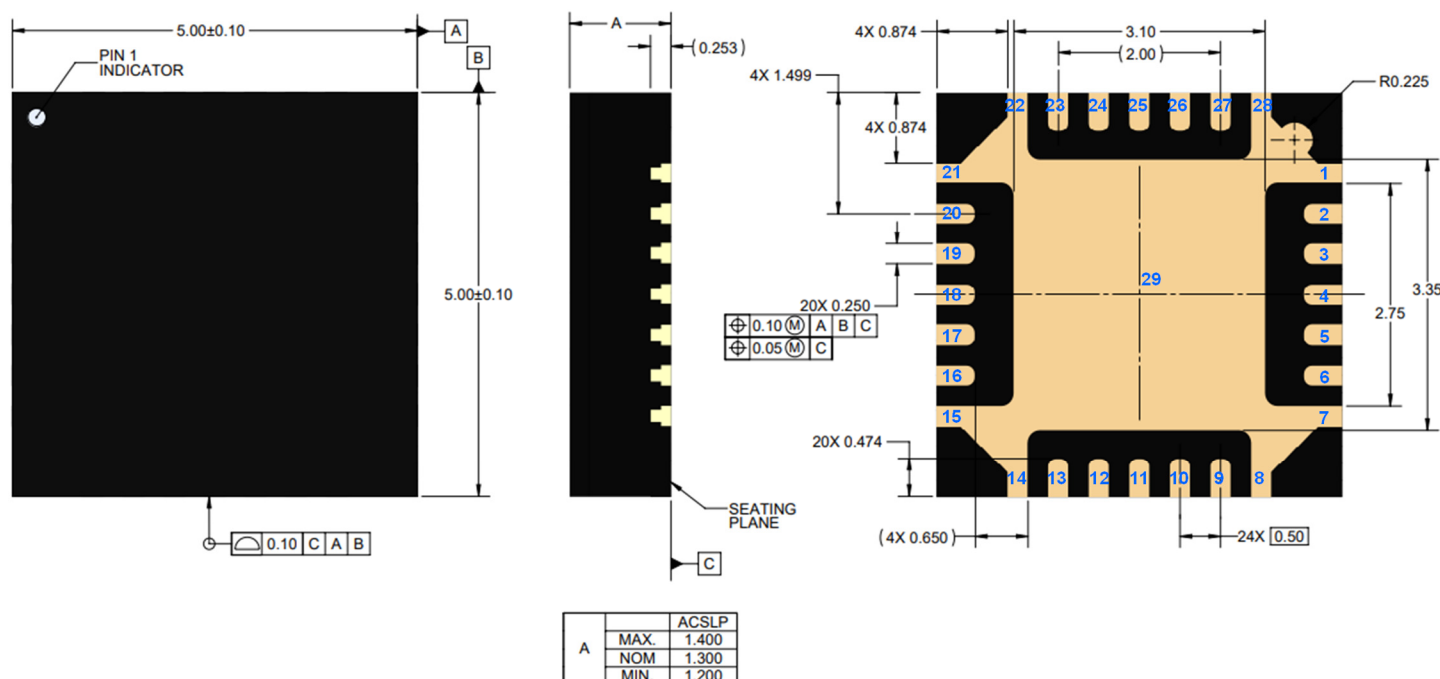
Bias-Up Procedure

1. Set I_D limit to 2.8 A, I_G limit to 60 mA
2. Set V_G to -1.5 V
3. Set V_D +6 V. Ensure $I_{DQ} \sim 0$ mA
4. Adjust V_G more positive until $I_D = 1430$ mA;
 $V_G \approx -0.6$ V +/- V typical range
5. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to -1.5 V. Ensure $I_{DQ} \sim 0$ mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Mechanical Information



Package is air-cavity and non-hermetic, leads are Au plated

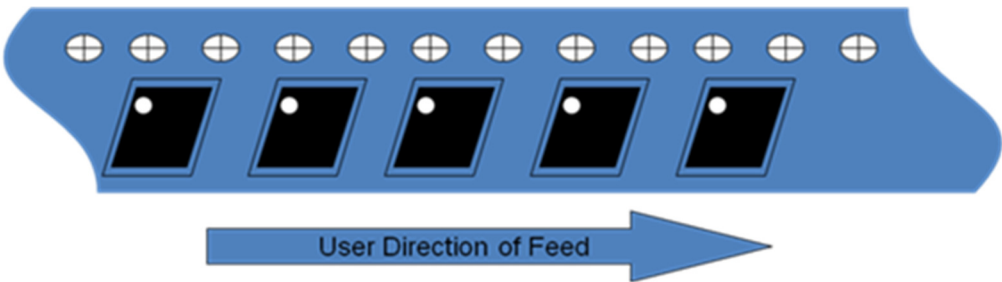
Pin Description

Pin Number	Symbol	Description
1, 7, 8, 13, 14, 15, 21, 22, 28, 29	GND	Ground and backside paddle (29); multiple vias should be employed to minimize inductance and thermal resistance
2, 3, 5, 6, 12, 16, 17, 19, 27	N/C	No internal connection; recommend grounding these pins for best RF performance and minimize inductance
4	RF _{IN}	RF Input. Matched to 50 Ω, DC blocked
9	V _{G1}	Gate voltage for stage 1 ⁽¹⁾
10	V _{G2}	Gate voltage for stage 2 ⁽¹⁾
11	V _{G3}	Gate voltage for stage 3 ⁽¹⁾
18	RF _{OUT}	RF Output. Matched to 50 Ω, DC blocked
20	V _{DET}	Detector diode output voltage. Varies with RF output power
23	V _{REF}	Reference diode output voltage
24	V _{D3}	Drain voltage for stage 3 ⁽¹⁾
25	V _{D2}	Drain voltage for stage 2 ⁽¹⁾
26	V _{D1}	Drain voltage for stage 1 ⁽¹⁾

1. External bypassing required; refer to page 18 for recommendation

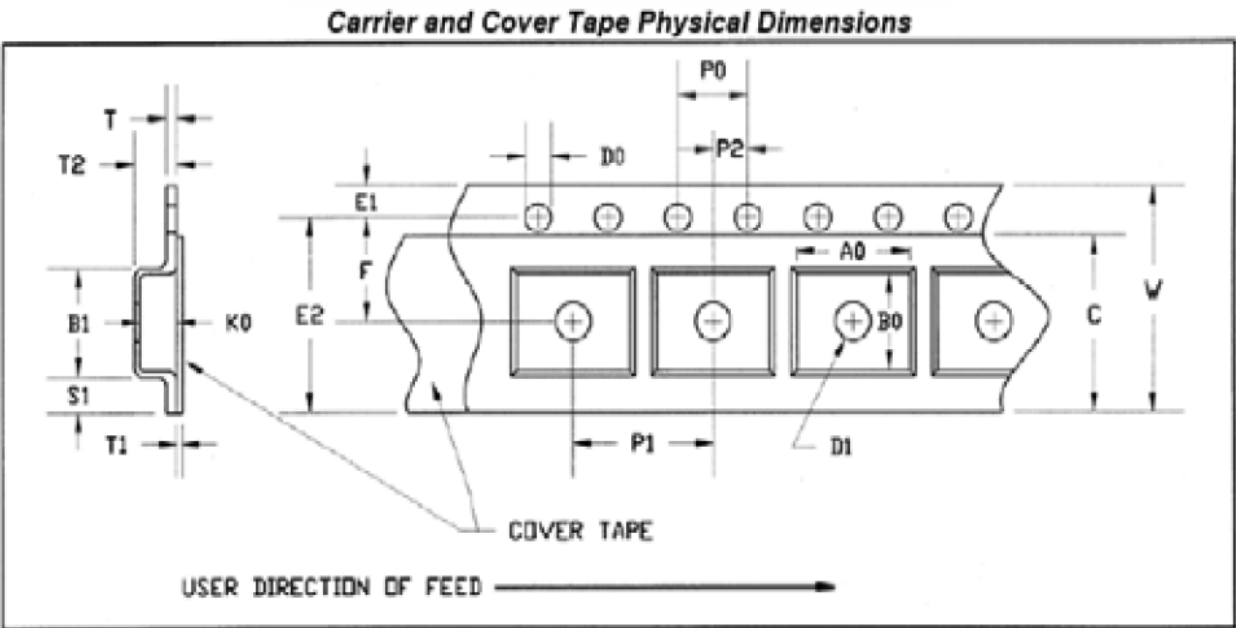
Tape and reel Information

Standard T/R size = 250 pieces on a 7" reel



CARRIER AND COVER TAPE DIMENSIONS

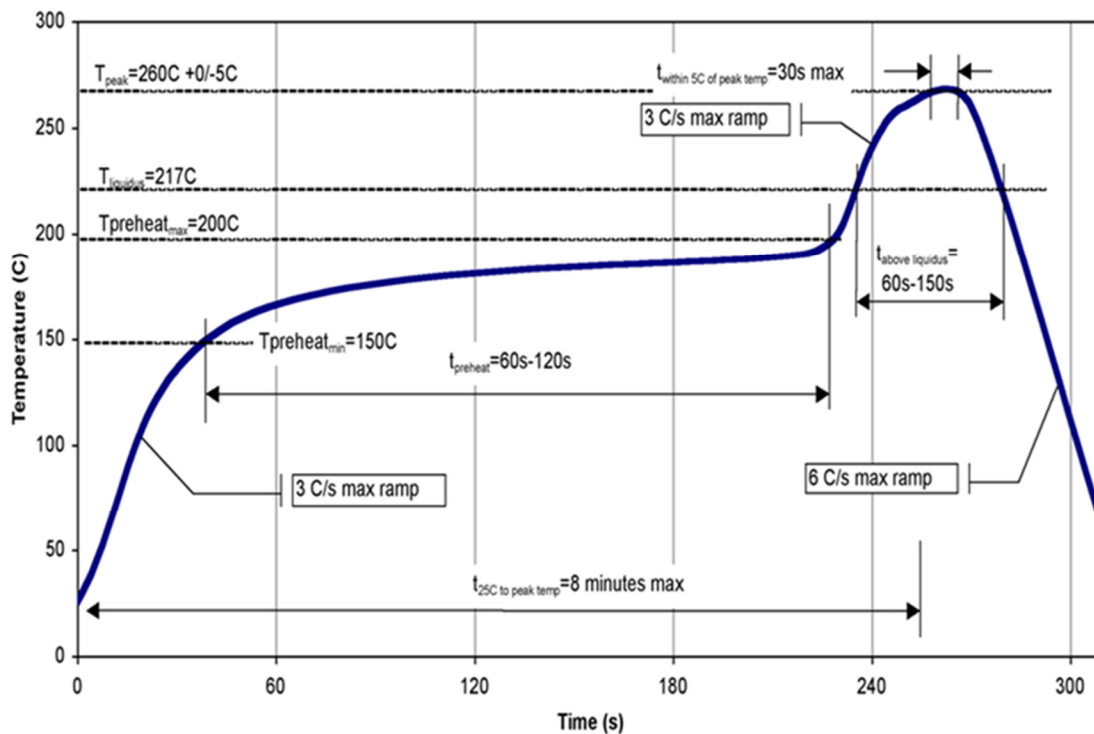
Part	Feature	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.209	5.3
	Width	B0	0.209	5.3
	Depth	K0	0.065	1.65
	Pitch	P1	0.314	8
Centerline Distance	Cavity to Perforation – Length Direction	P2	0.079	2
	Cavity to Perforation – Width Direction	F	0.217	5.5
Cover Tape	Width	C	0.362	9.2
Carrier Tape	Width	W	0.472	12



Solderability

- Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C
- Do not expose the package lid to temperatures > 280 °C
- Contact plating: Ni-Au
- Solder rework not recommended

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	C3	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	5A	IPC/JEDEC J-STD-020



Caution!

ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU .

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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