QPA4003

26.5 – 29.5 GHz 5 W GaN Power Amplifier

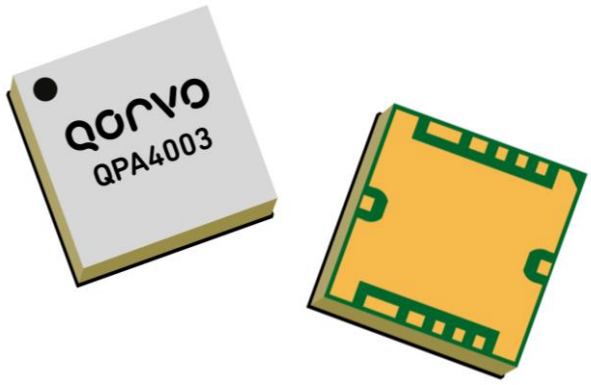
Product Description

Qorvo's QPA4003 is a Ka-band power amplifier fabricated on Qorvo's 0.15um GaN on SiC process (QGaN15). Operating from 26.5 to 29.5 GHz, it achieves 1.25 W linear power with lower than −33 dBc intermodulation distortion products and 29 dB small signal gain. Saturated output power is greater than 37 dBm (5 W) with an associated power-added efficiency of 22 %.

The QPA4003 is packaged in a 5.0 x 5.0 mm laminate package. It can support a variety of operating conditions to best support system requirements. With good thermal properties, it can support a range of bias voltages.

The QPA4003 is fully matched to 50 ohms. RF I/O power are shorted to ground. The QPA4003 is ideally suited to support satellite communications and 5G infrastructure.

Lead-free and RoHS compliant.

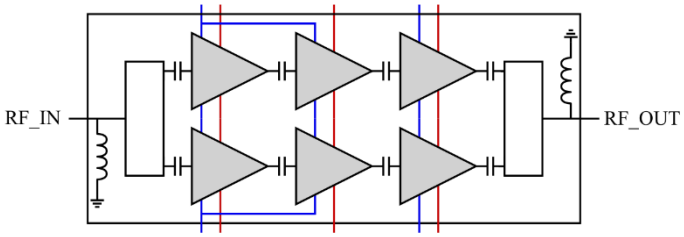


Product Features

- Frequency Range: 26.5 – 29.5 GHz
- P_{SAT} (P_{IN} = 16 dBm): 37 dBm
- PAE (P_{IN} = 16 dBm): 22 %
- Power Gain (P_{IN} = 16 dBm): 22 dB
- Small Signal Gain: 29 dB
- IMD3 (P_{OUT} = 31 dBm/tone): −33 dBc
- Bias: V_D = 20 V, I_{DQ} = 580 mA
- Package Dimensions: 5.0 x 5.0 x 1.621 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details

Functional Block Diagram



Top View

Applications

- 5G Infrastructure
- Satellite Communications

Ordering Information

Part No.	Description
QPA4003	26.5 – 29.5 GHz 5 W GaN Power Amplifier
QPA4003S2	2 piece sample bag
QPA4003TR7	MOQ pieces on 7-inch reel
QPA4003EVB01	QPA4003 Evaluation Board Kit

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	−5 to 0 V
Drain Current, Stages 1 + 2 (I_{D12})	1.3 A
Drain Current, Stage 3 (I_{D3})	1.5 A
Gate Current (I_G)	See plot on page 14
Power Dissipation (P_{DISS}), 85°C	24 W
Input Power (P_{IN}), 50 Ω, V_D=24 V, I_{DQ}=580 mA, 85 °C	21 dBm
Input Power (P_{IN}), 3:1 VSWR, V_D=24 V, I_{DQ}=580 mA, 85 °C	21 dBm
Package Soldering Temperature (30 Seconds)	260 °C
Storage Temperature	−40 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value / Units
Drain Voltage, All Stages (V_D)	20 V
Drain Current, Stages 1 + 2 (I_{DQ12})	480 mA
Drain Current, Stage 3 (I_{DQ3})	100 mA
Operating Temperature Range	−40 to +85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

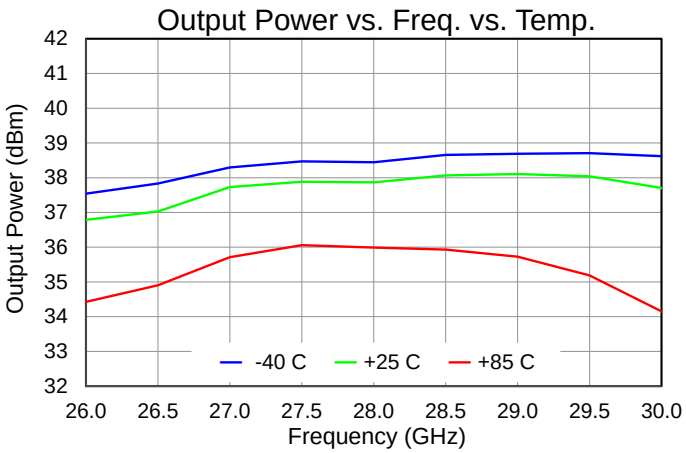
Electrical Specifications

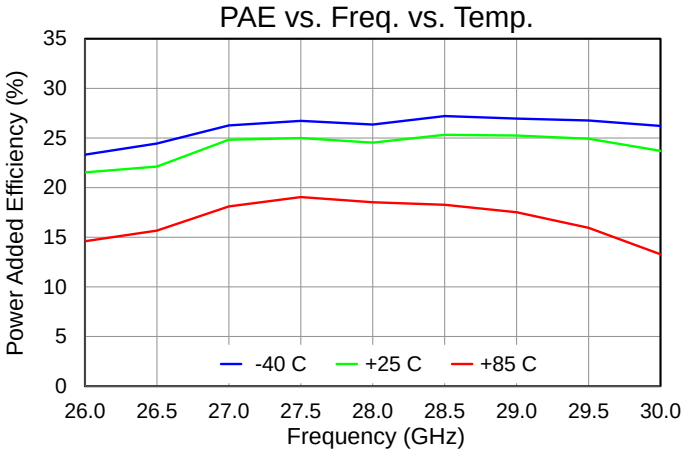
Parameter		Min	Typ	Max	Units
Operational Frequency		26.5		29.5	GHz
Output Power (P_{IN}=16 dBm)	26.5 GHz 28.0 GHz 29.5 GHz		37.0 37.9 38.0		dBm dBm dBm
Power Added Efficiency (P_{IN}=16 dBm)	26.5 GHz 28.0 GHz 29.5 GHz		22.1 24.5 24.9		% % %
Small Signal Gain	26.5 GHz 28.0 GHz 29.5 GHz		27.7 28.9 29.5		dB dB dB
Input Return Loss	26.5 GHz 28.0 GHz 29.5 GHz		31 11 12		dB dB dB
Output Return Loss	26.5 GHz 28.0 GHz 29.5 GHz		13 17 12		dB dB dB
IMD3 (P_{OUT}/Tone = 31 dBm, 160 MHz tone separation, I_{DQ} = 555 mA)	26.75 GHz 27.50 GHz 28.50 GHz 29.25 GHz		−33.6 −33.8 −36.6 −37.9		dBc dBc dBc dBc
P_{OUT} Temp. Coeff. (85 °C to 25 °C, P_{IN} = 16 dBm))			−0.036		dB/°C
Sm. Sig. Gain Temp. Coefficient (85 °C to −40 °C)			−0.093		dB/°C
Gate Leakage (V_D = 10 V, V_G = −4)		−4.6			mA

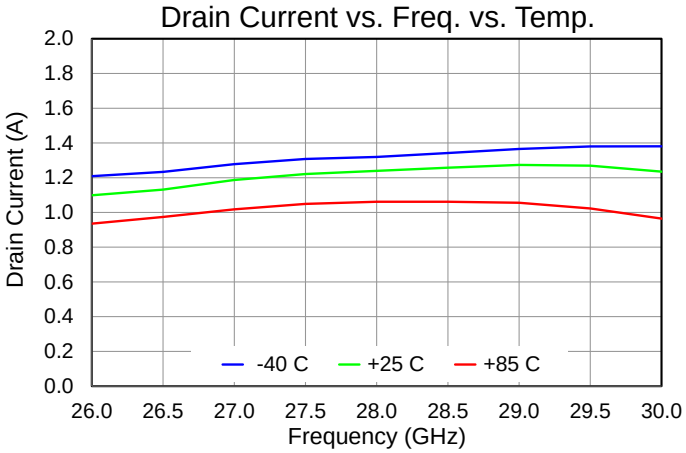
Test conditions, unless otherwise noted: T = 25 °C, V_D = 20 V, I_{DQ} = 580 mA

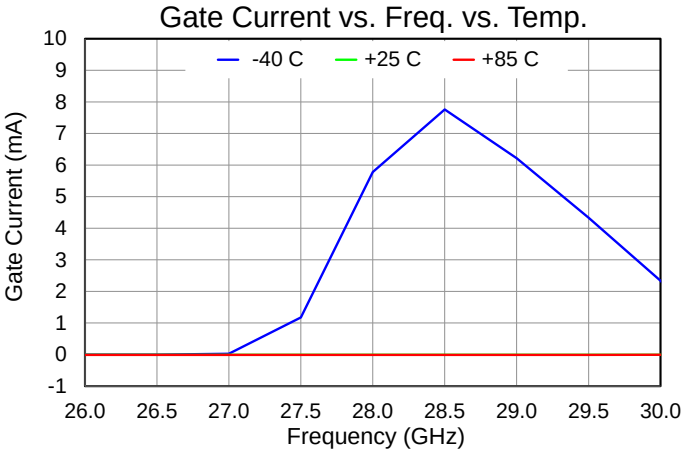
Performance Plots – Large Signal (CW)

Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 580 mA, P_{IN} = 16 dBm



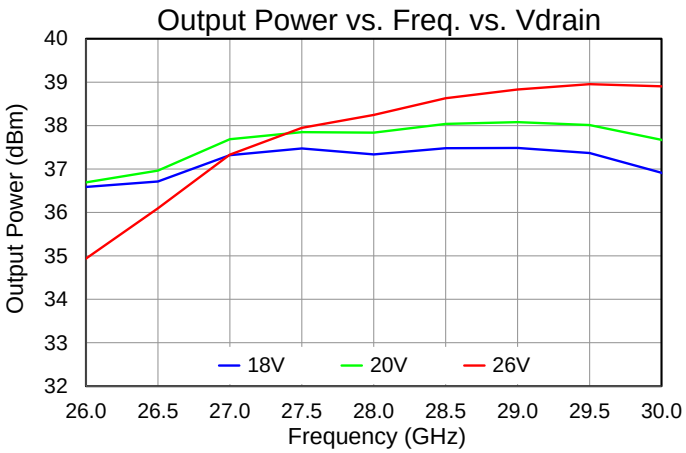


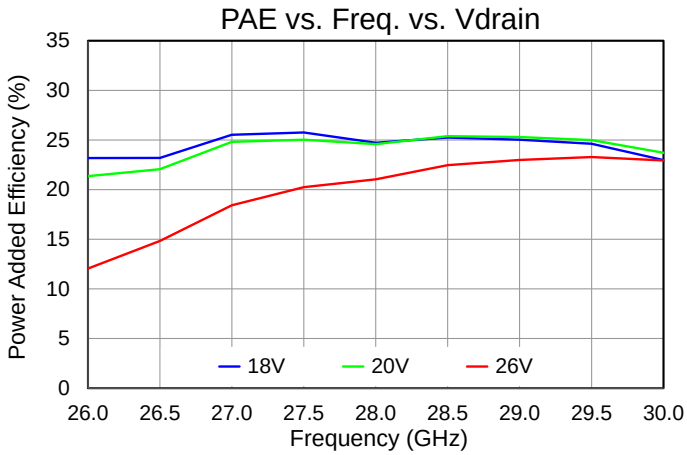


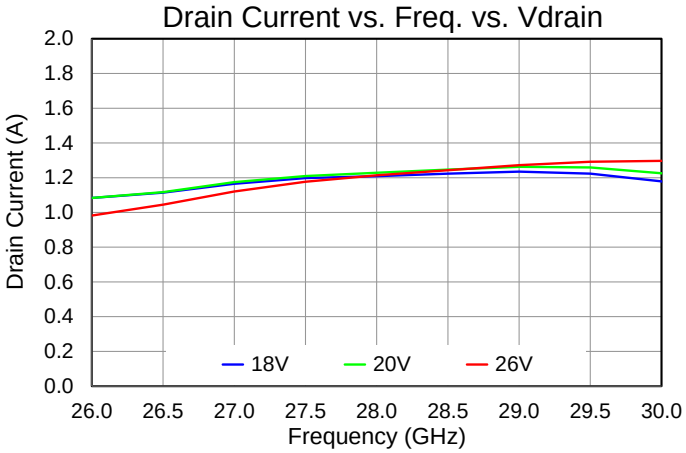


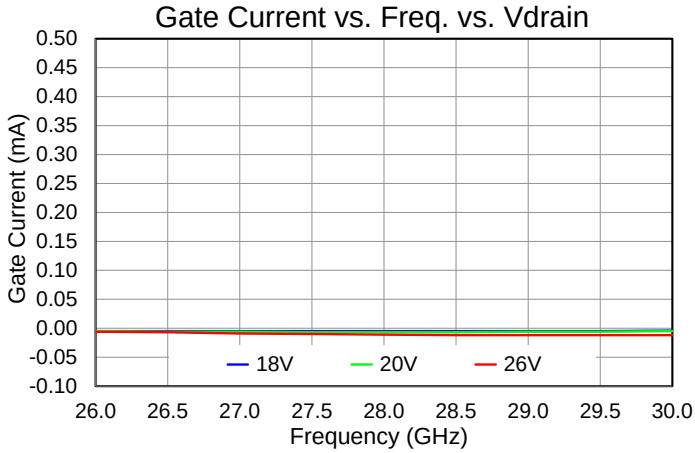
Performance Plots – Large Signal (CW)

Test conditions, unless otherwise noted: I_{DQ} = 555 mA, T = 25 °C, P_{IN} = 16 dBm



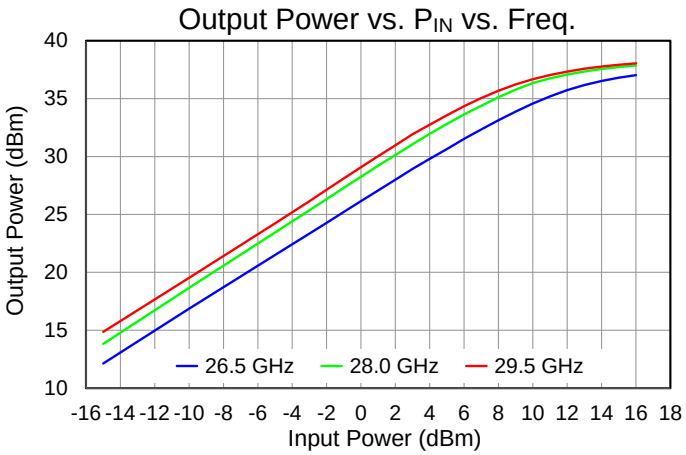


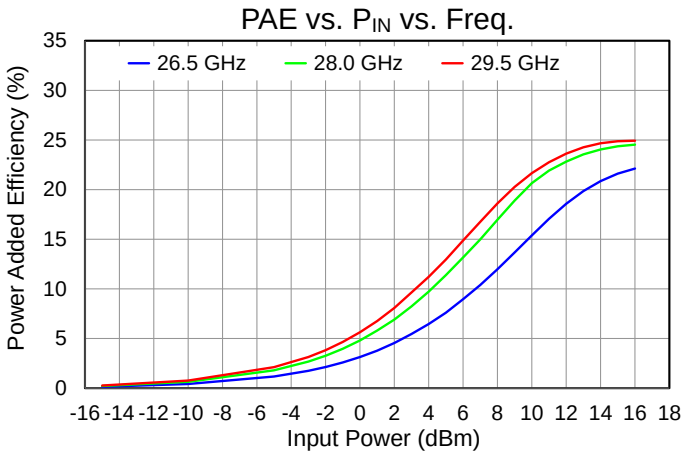


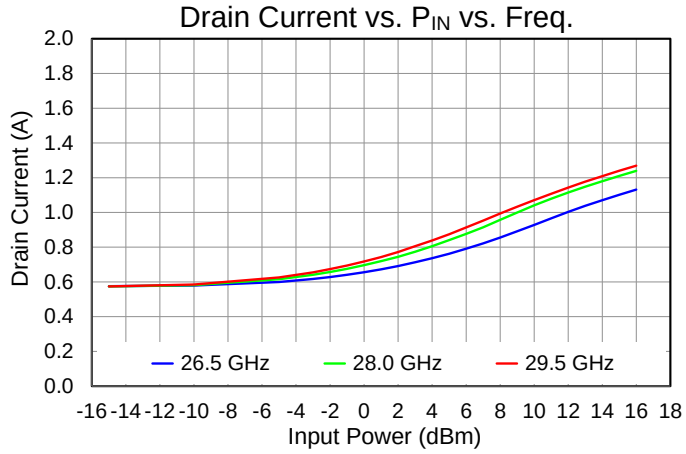


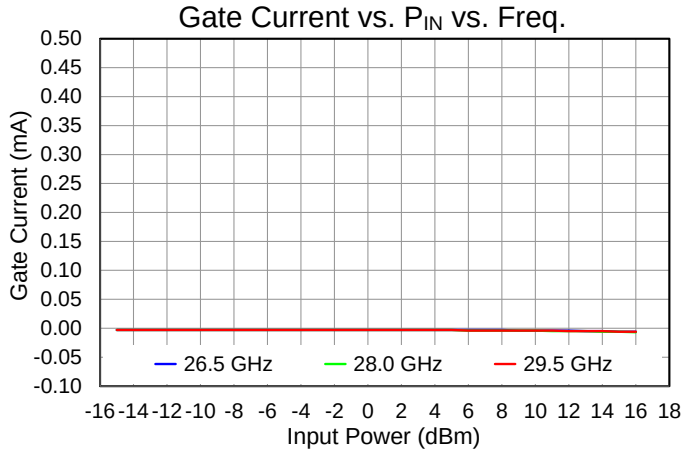
Performance Plots – Large Signal

Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 580 mA, T = 25 °C



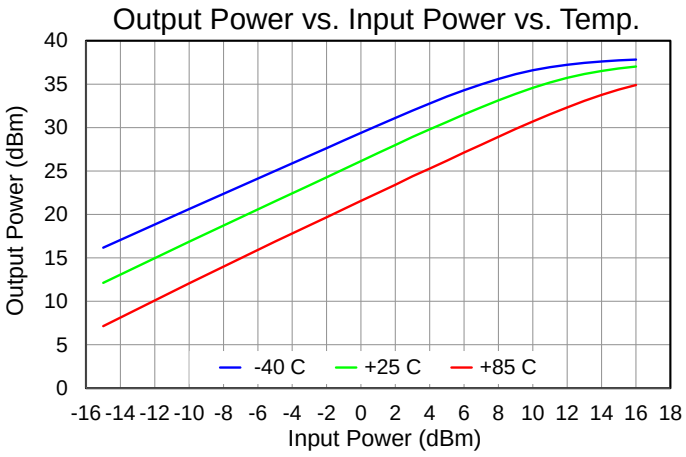


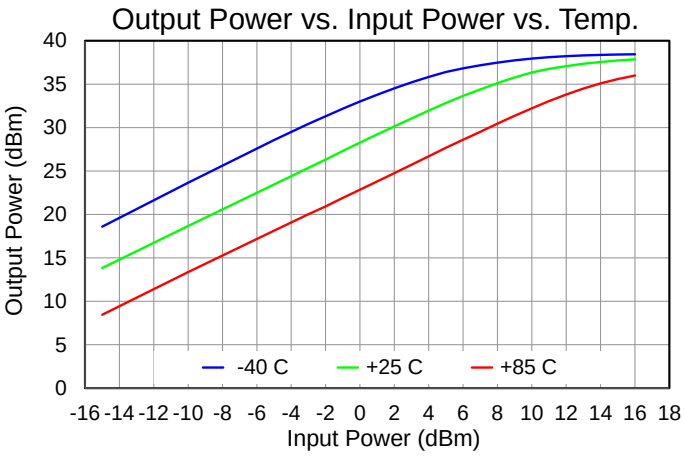


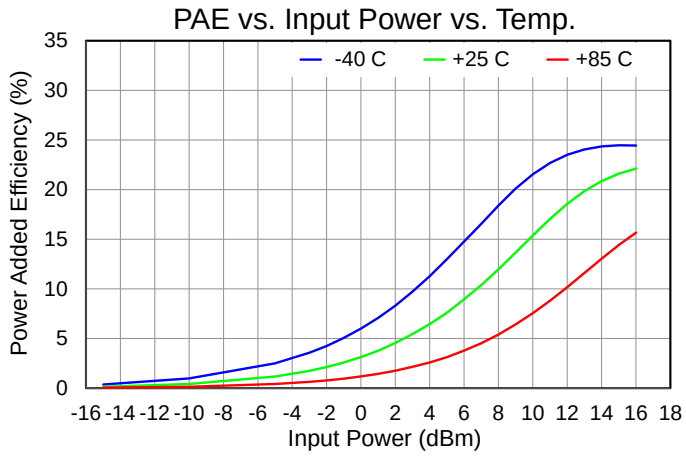


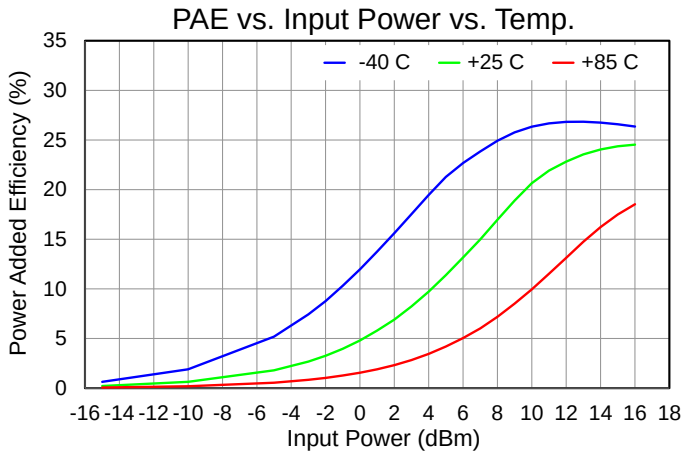
Performance Plots – Large Signal

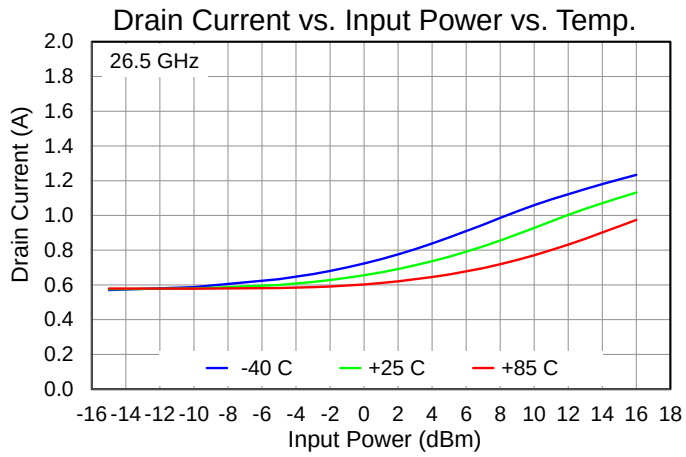
Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 580 mA

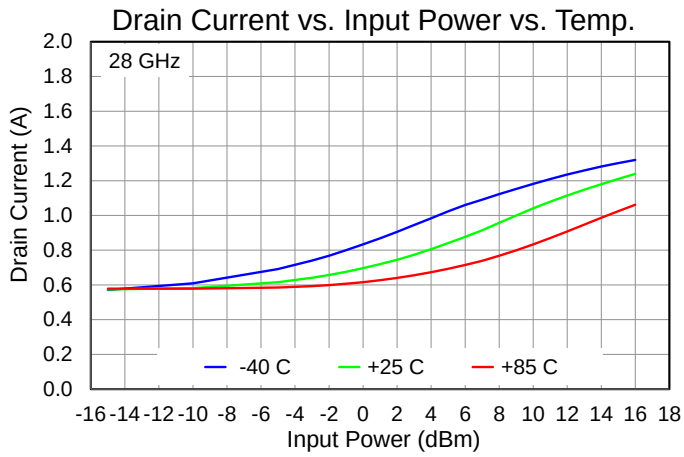






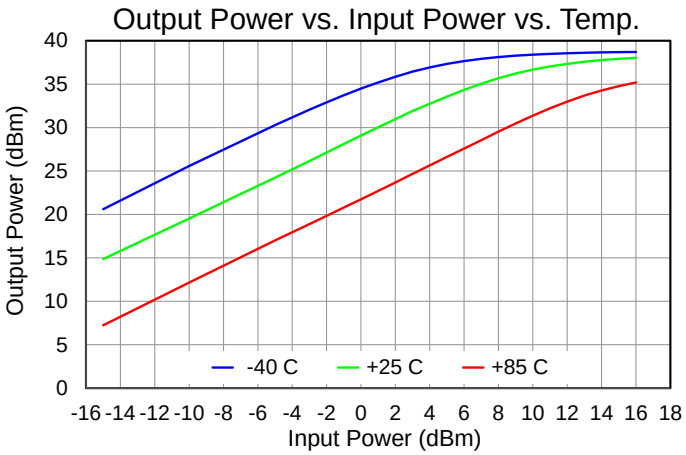


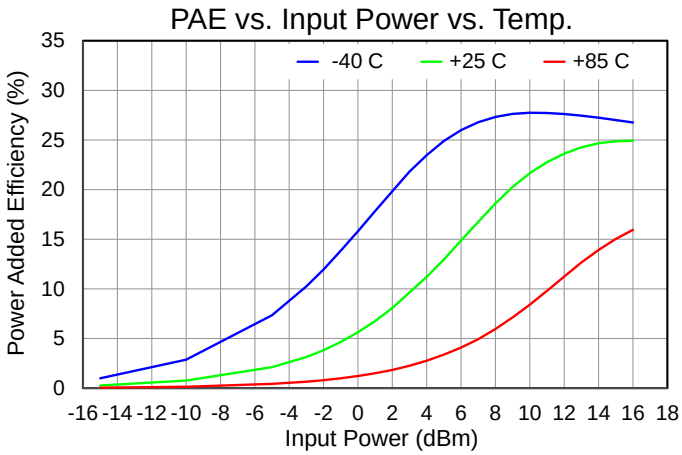


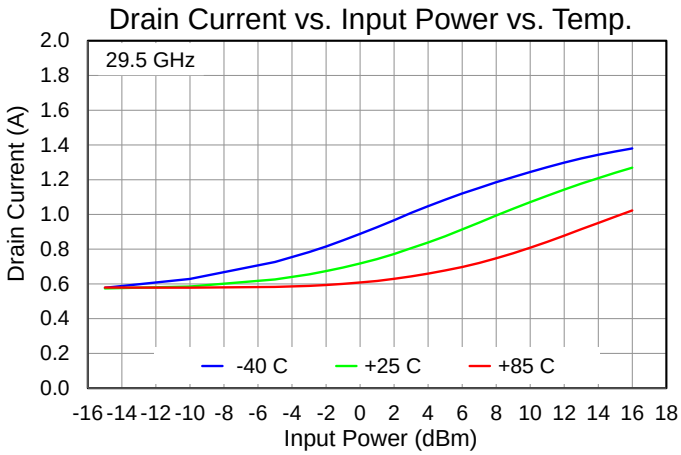


Performance Plots – Large Signal

Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 580 mA

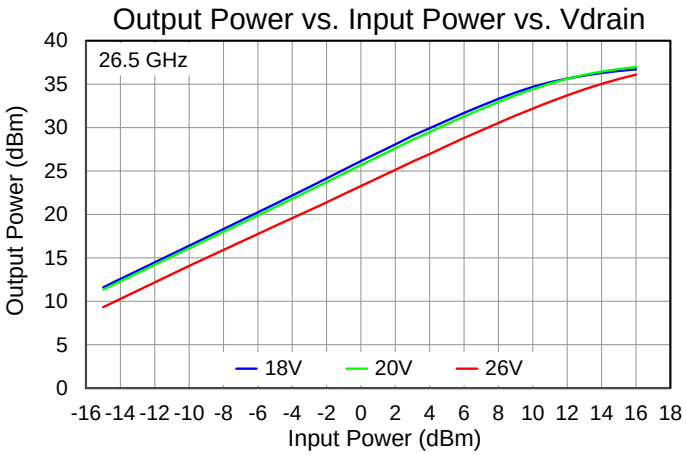


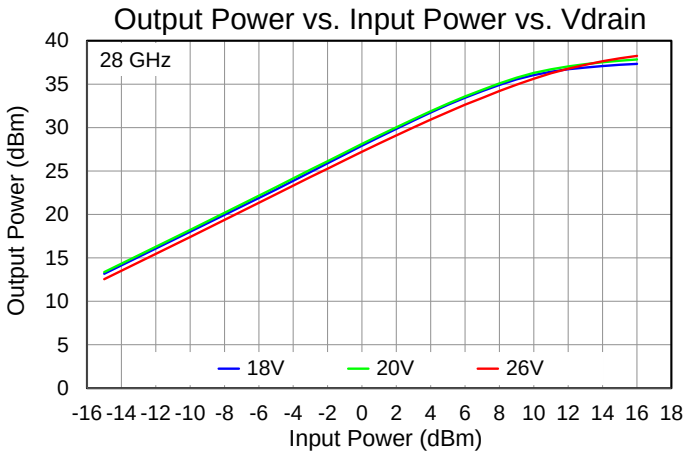


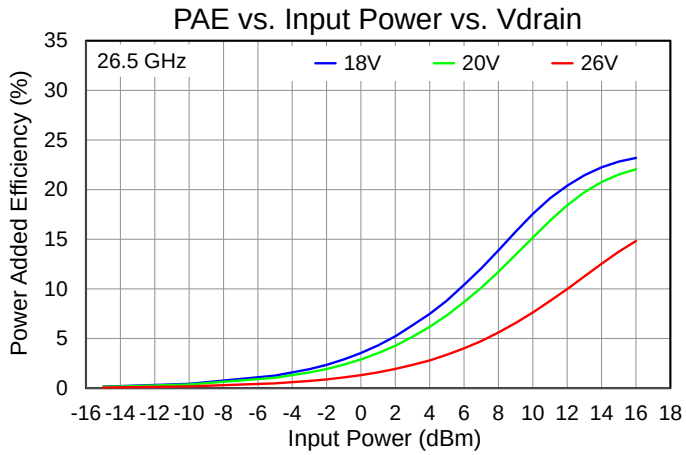


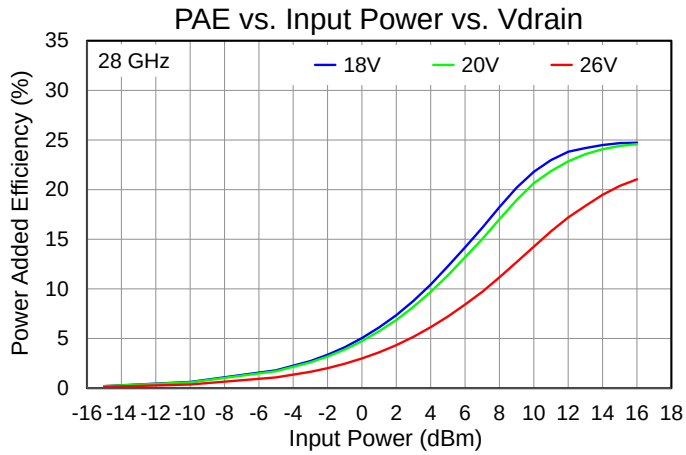
Performance Plots – Large Signal

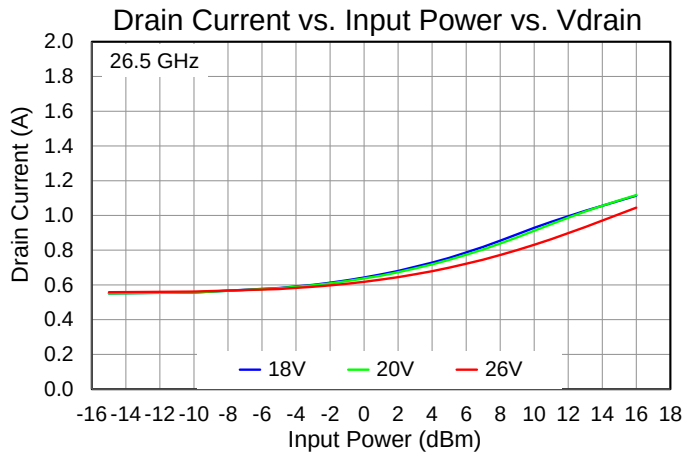
Test conditions, unless otherwise noted: I_{DQ} = 555 mA, T = 25 °C

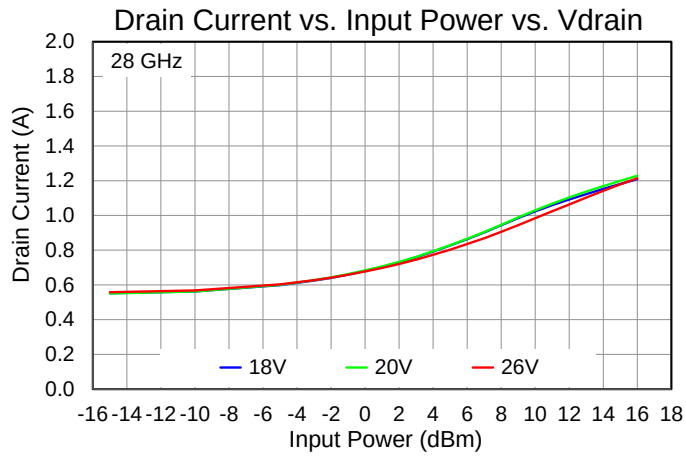






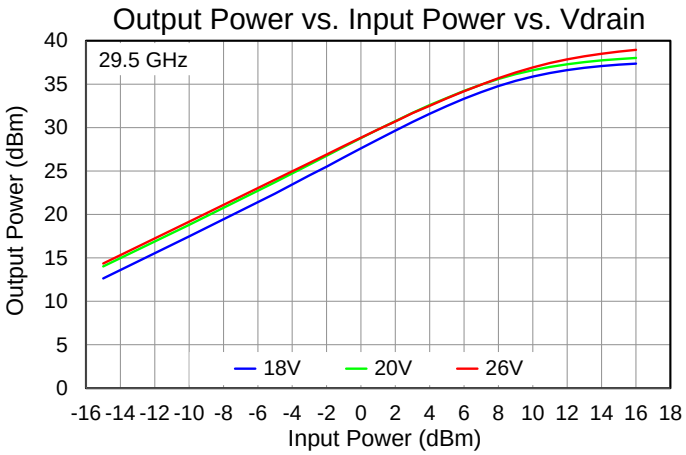


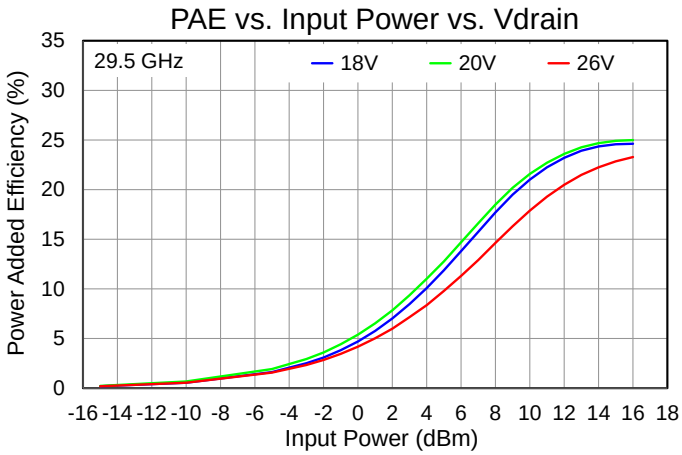


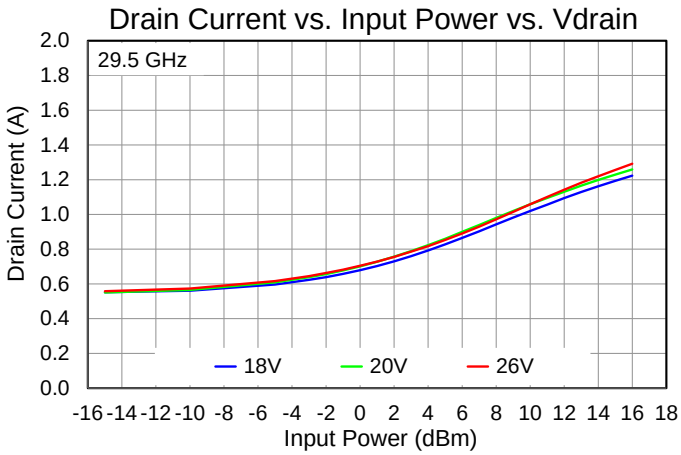


Performance Plots – Large Signal (CW)

Test conditions, unless otherwise noted I_{DQ} = 555 mA, T = 25 °C



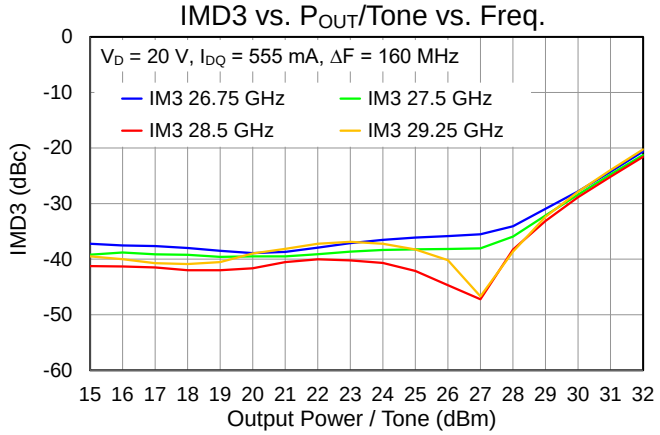




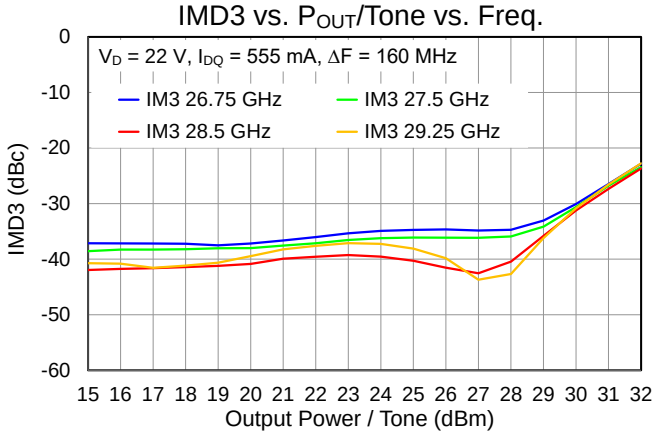
Performance Plots – Linearity

Test conditions, unless otherwise noted: I_{DQ} = 555 mA, T = 25 °C, Tone Separation = 160 MHz

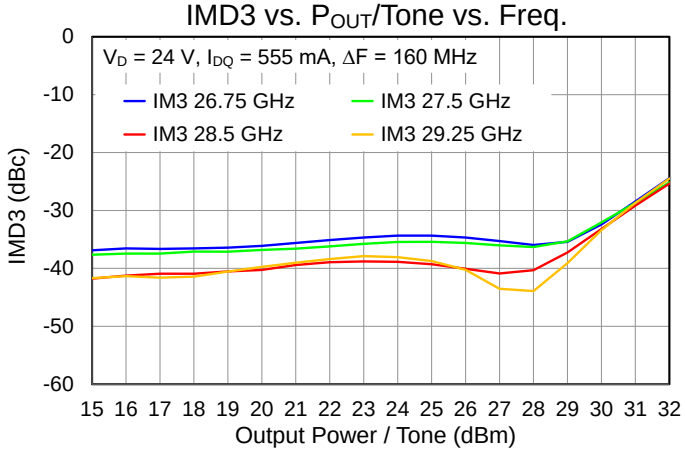
IMD3 vs. P_{OUT}/Tone vs. Freq.



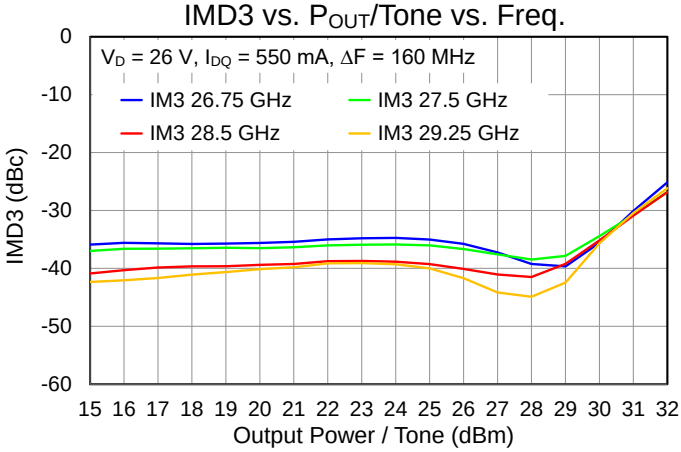
IMD3 vs. P_{OUT}/Tone vs. Freq.



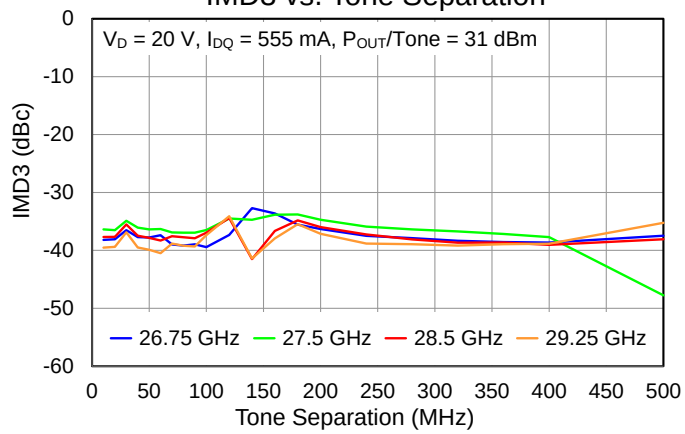
IMD3 vs. P_{OUT}/Tone vs. Freq.



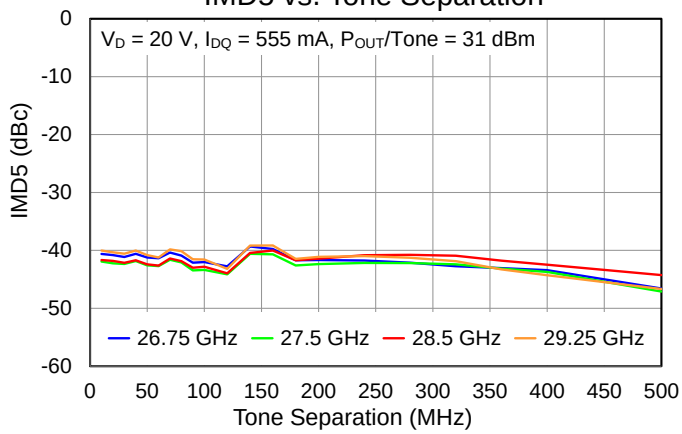
IMD3 vs. P_{OUT}/Tone vs. Freq.



IMD3 vs. Tone Separation

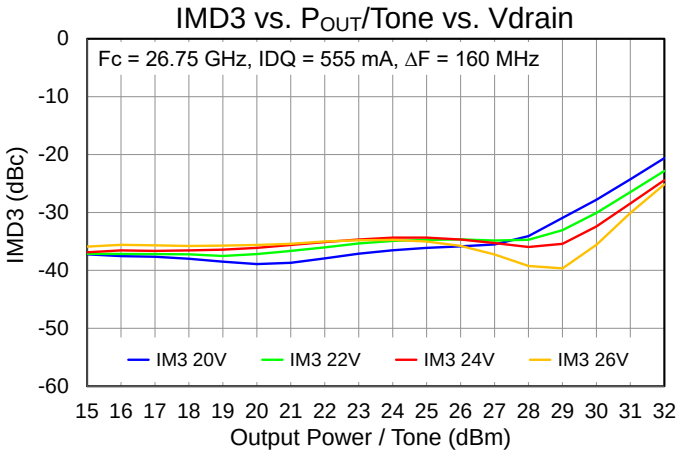


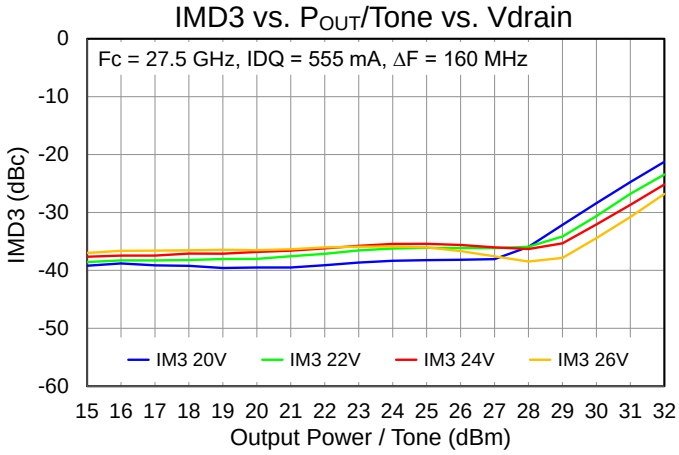
IMD5 vs. Tone Separation

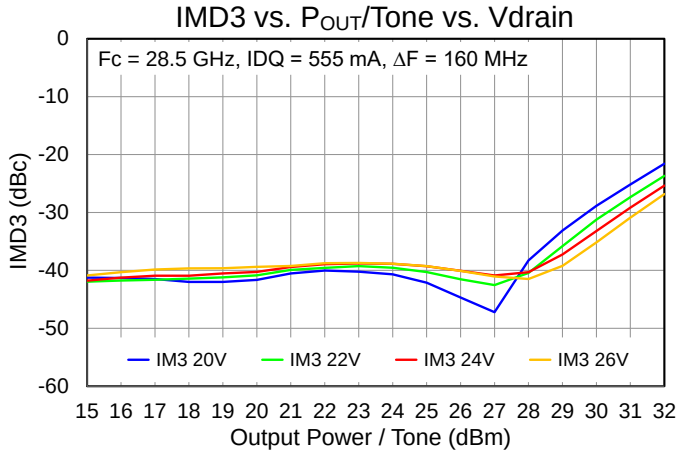


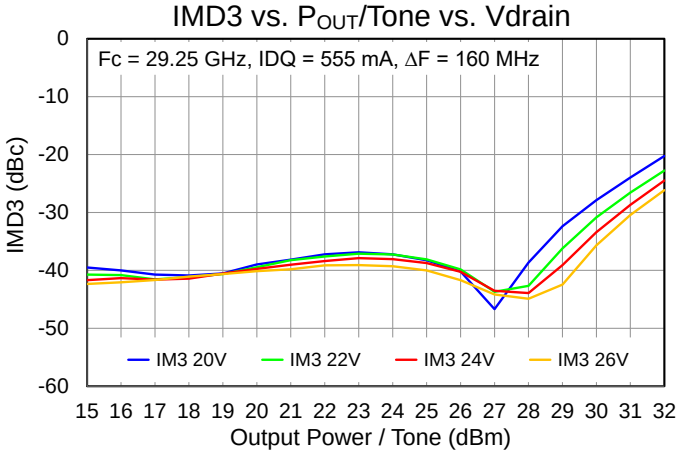
Performance Plots – Linearity

Test conditions, unless otherwise noted: I_{DQ} = 555 mA, T = 25 °C, Tone Separation = 160 MHz



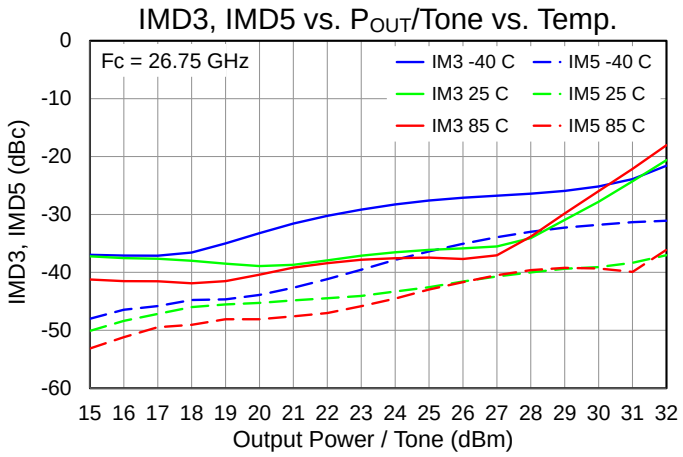


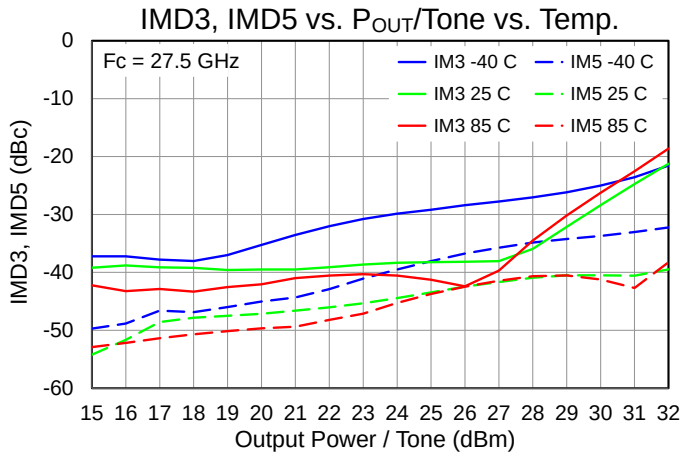


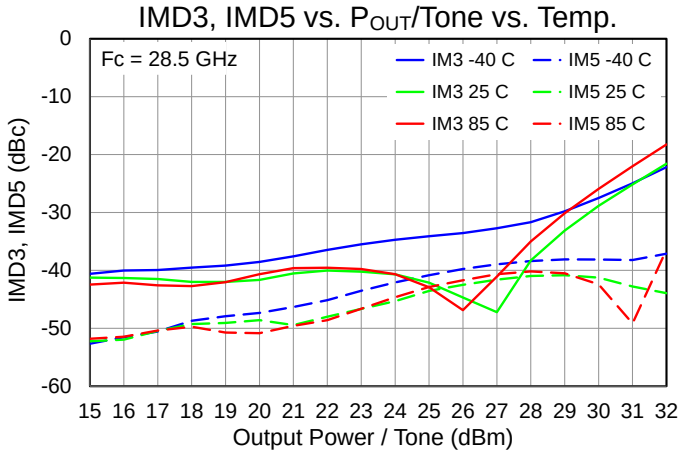


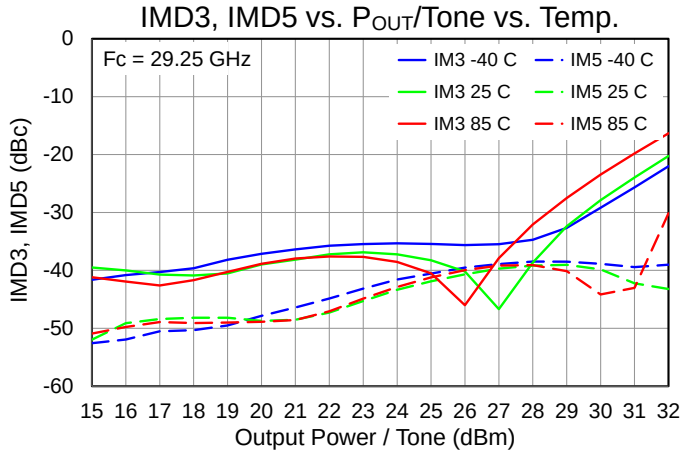
Performance Plots – Linearity

Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 555 mA, T = 25 °C, Tone Separation = 160 MHz





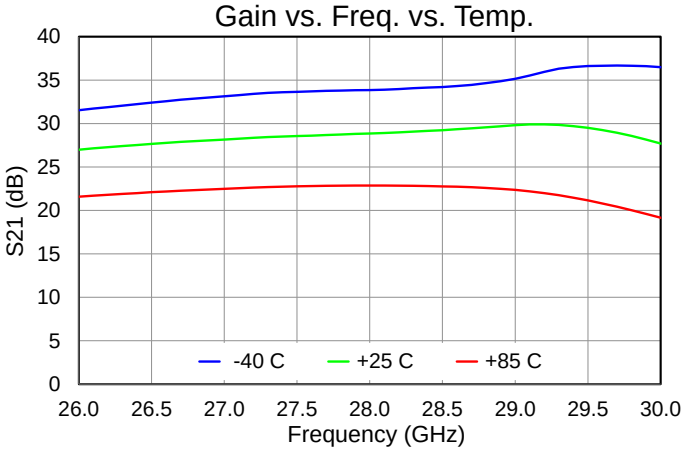




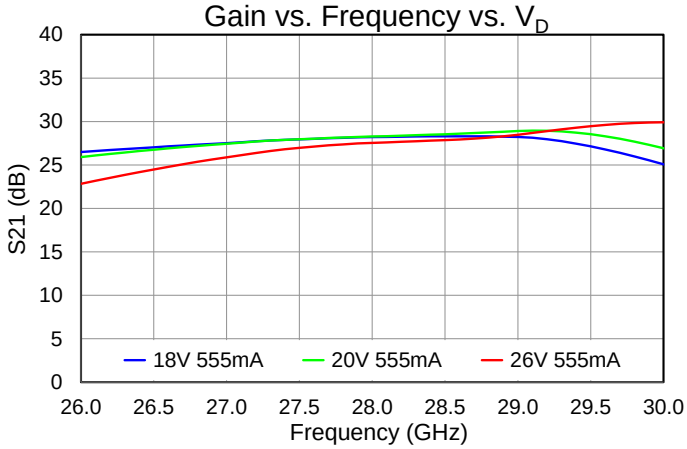
Performance Plots – Small Signal

Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 580 mA, T = 25 °C

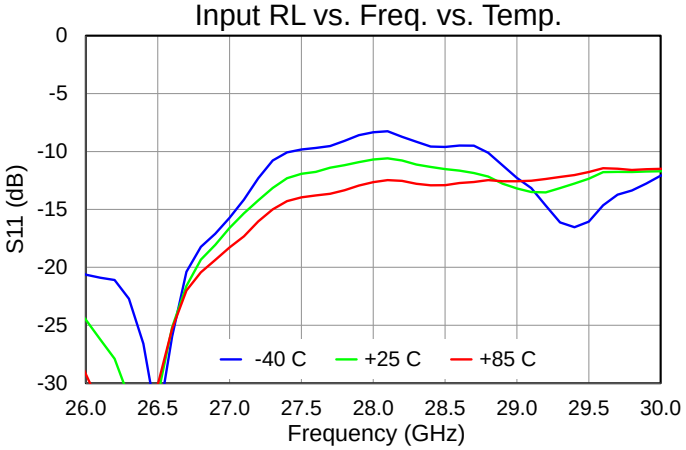
Gain vs. Freq. vs. Temp.



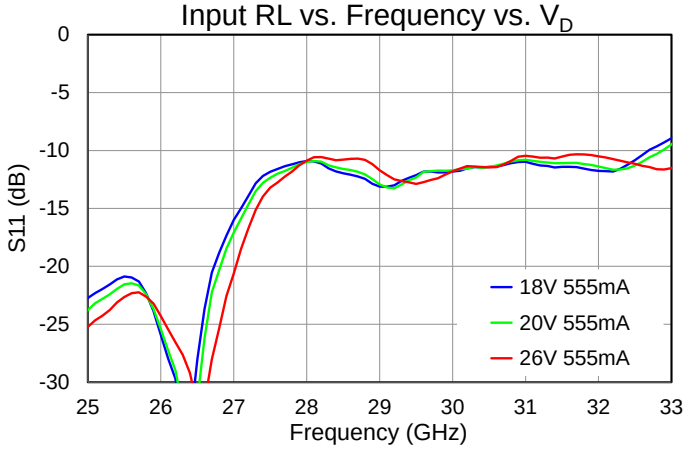
Gain vs. Frequency vs. V_D



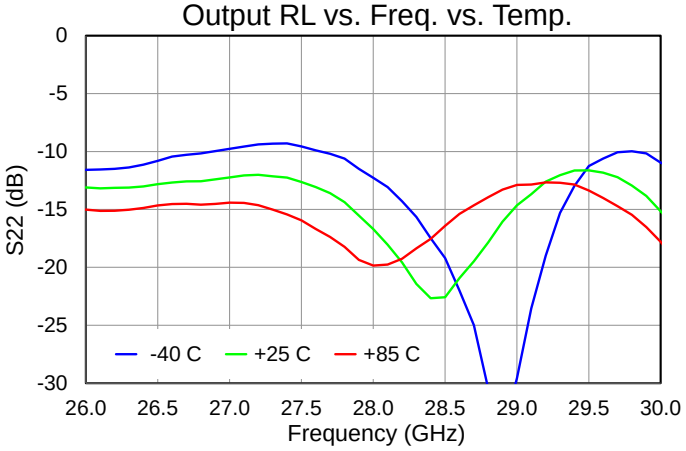
Input RL vs. Freq. vs. Temp.



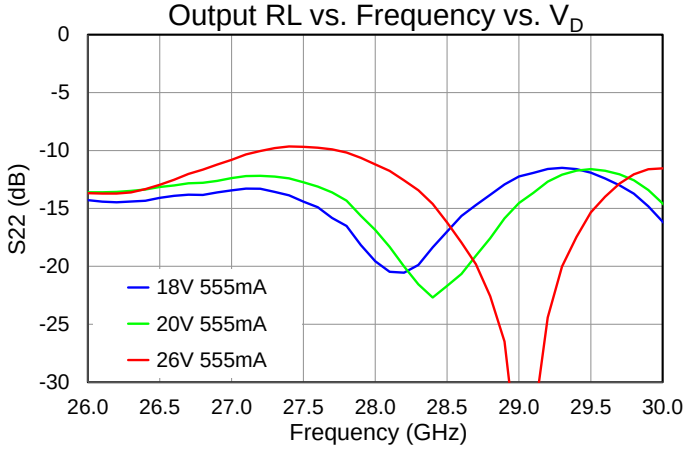
Input RL vs. Frequency vs. V_D



Output RL vs. Freq. vs. Temp.



Output RL vs. Frequency vs. V_D

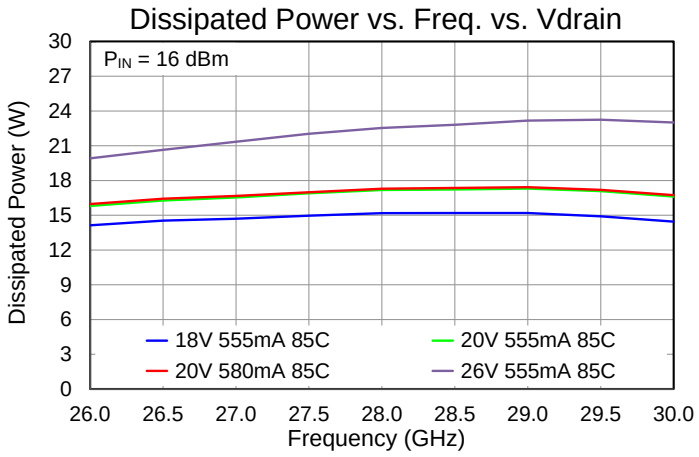


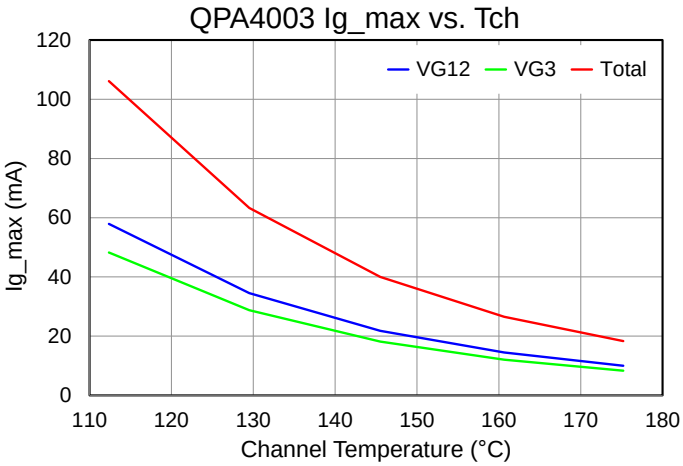
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 20 V, I_{DQ} = 580 mA, P_{DISS} = 11.6 W, No RF (quiescent DC operation)	3.853	ºC/W
Channel Temperature, T_{CH} (No RF) (2)		129.7	ºC
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 20 V, I_{DQ} = 580 mA, Freq = 29.0 GHz, I_{D_Drive} = 1056 mA, P_{IN} = 16 dBm, P_{OUT} = 35.73 dBm, P_{DISS} = 17.42 W	3.387	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		144.0	ºC

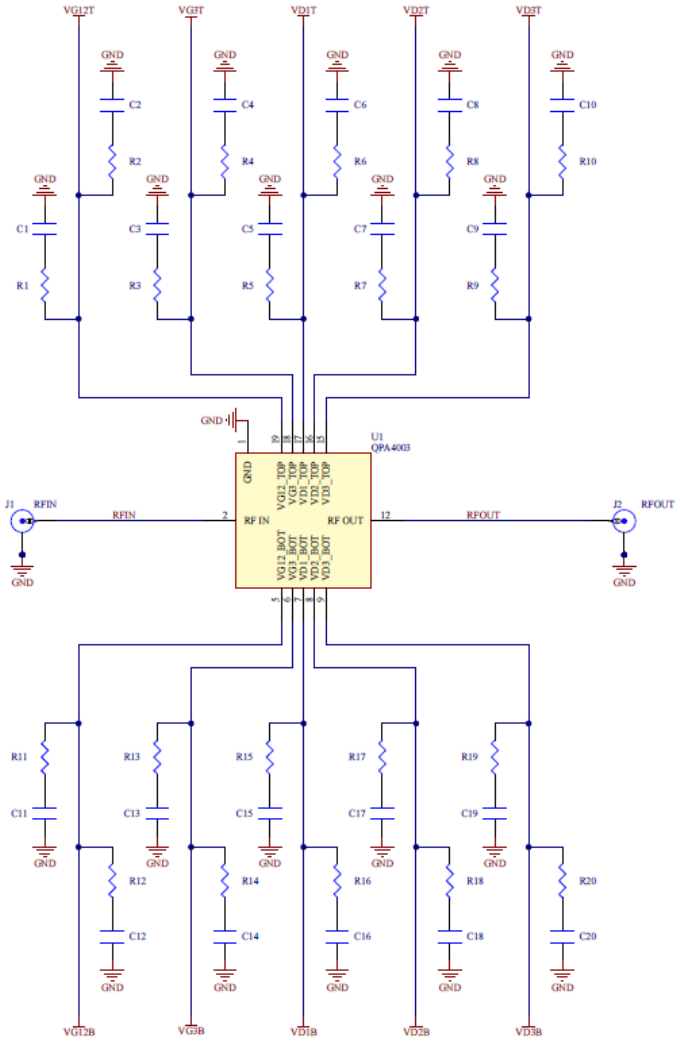
Notes:
1. Thermal resistance is referenced to the back of package (85 ºC)
2. IR Scan equivalent. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Dissipated Power and Maximum Gate Current





Applications Information



Notes:

1. V_G and V_D must be biased from both sides. V_{G12} and V_{G3} may be biased separately or tied together. V_{D1}, V_{D2}, and V_{D3} should be tied together.

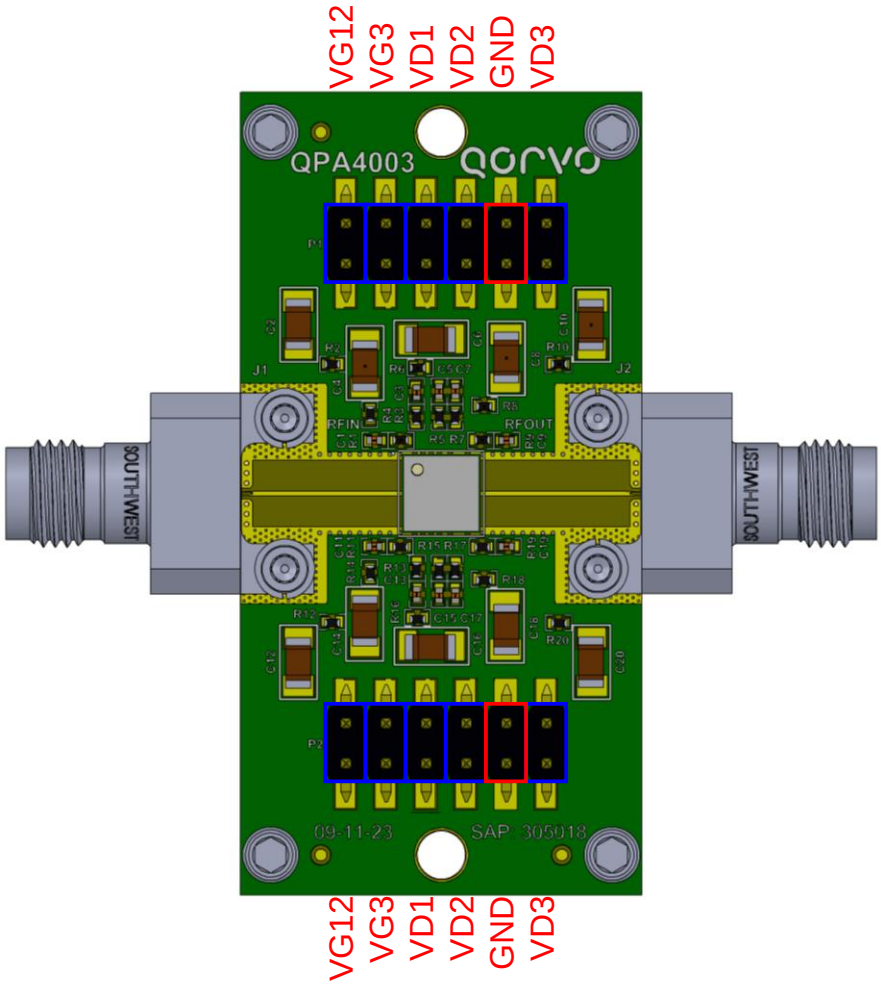
Bias Up Procedure

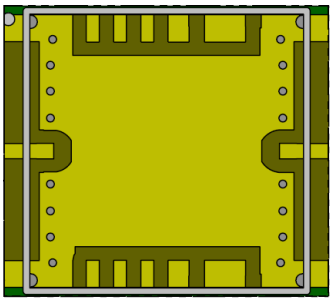
1. Set I_D limit to 1850 mA, I_{G12} limit to 20 mA, and I_{G3} limit to 20 mA
2. Set V_{G12} and V_{G3} to −4 V
3. Set V_D to +20 V; ensure I_{DQ} is approximately 0 mA
4. Adjust V_{G12} until I_{DQ} ≈ 480 mA. Adjust V_{G3} until I_{DQ} ≈ 580 mA
5. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_{G12} and V_{G3} to −4 V; ensure I_{DQ} is approximately 0 mA
3. Set all V_D to 0 V
4. Turn off V_D supplies
5. Turn off V_G supplies

Evaluation Board (EVB) Assembly Drawing





PCB Package Location

PCB NOTES:

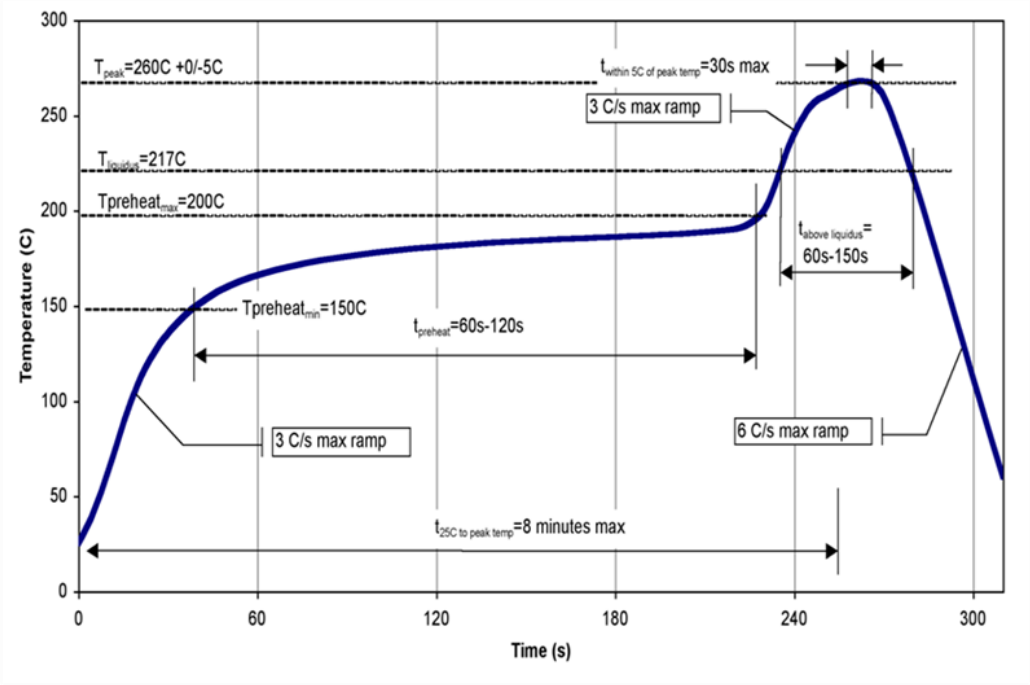
1. PCB is multi layer, with the RF layer made from Taconic TSM-DS3B dielectric, 0.005 inch thick, 0.5 oz. copper both sides. Cooper coin is placed in the PCB under the DUT location for improved thermal conductivity.
2. V_G and V_D must be biased from both sides. V_{G12} and V_{G3} may be biased separately or tied together. V_{D1}, V_{D2}, and V_{D3} should be tied together.

Bill of Materials

Reference Des.	Value	Description	MFG.	Part No.
C1,C3,C5,C7,C9,C11,C13,C15,C17,C19	0.01 uF	CAP, 0.01uF, 10%, 50V, X7R, 0402	Various	–
C2,C4,C6,C8,C10,C12,C14,C16,C18,C20	10 uF	CAP, 10uF, 20%, 50V, 20%, X5R, 1206	Various	–
R1,R2,R3,R4,R5,R6,R7,R8,R9,R10,R11, R12,R13,R14,R15,R16,R17,R18,R19,R20	0 Ω	RES, 0 OHM, JMPR, 0402	Various	–
J1, J2	2.4 mm	2.4 mm (F) RF Connector	Southwest Microwave	1492-04A-12

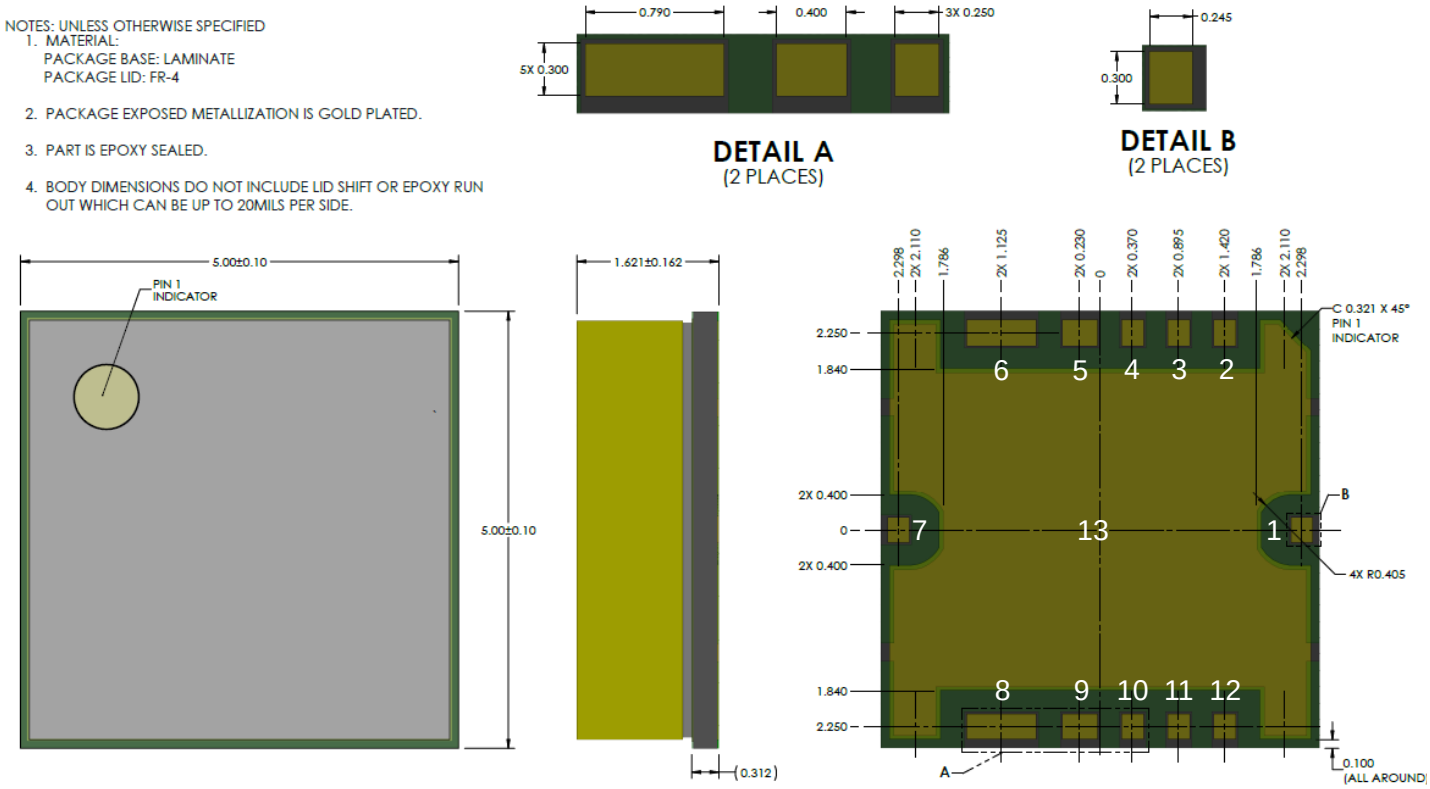
Assembly Notes

- Compatible with lead-free soldering processes with 260°C peak reflow temperature.
- Contact plating: Ni-Au
- Solder rework is not recommended



Recommended soldering temperature profile

Mechanical Information and Pad Description



Tolerances:

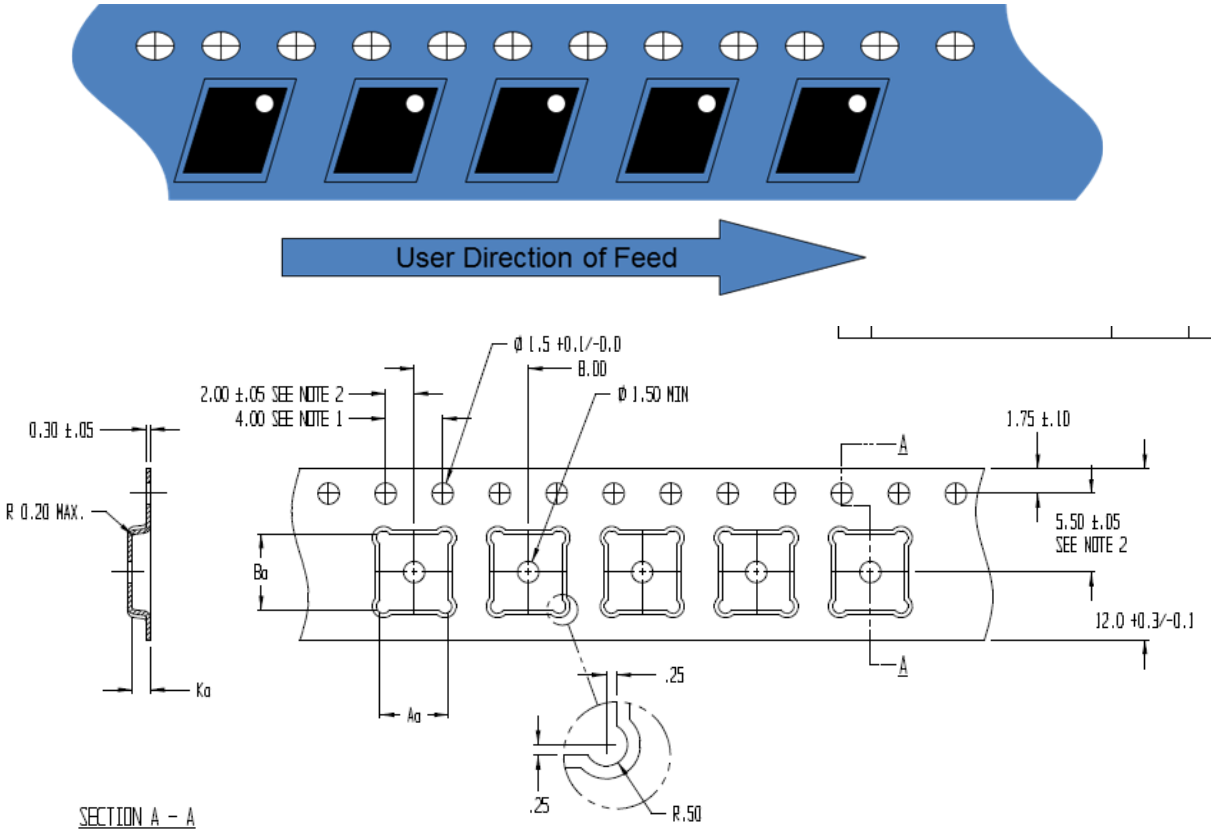
.XX = ± .25
.XXX = ± .100
.XXXX = ± .0245

Unless otherwise specified, dimensions are in mm

Pad Description

Pad No.	Symbol	Description
1	RF IN	Input; matched to 50 Ω; DC grounded
2	VG12_TOP	Gate bias, stages 1&2 top. Refer to page 15 for bypassing network.
3	VG3_TOP	Gate bias, stage 3 top. Refer to page 15 for bypassing network.
4	VD1_TOP	Drain bias, stage 1 top. Refer to page 15 for bypassing network.
5	VD2_TOP	Drain bias, stage 2 top. Refer to page 15 for bypassing network.
6	VD3_TOP	Drain bias, stage 3 top. Refer to page 15 for bypassing network.
7	RF OUT	Output; matched to 50 Ω; DC grounded
8	VD3_BOT	Drain bias, stage 3 bottom. Refer to page 15 for bypassing network.
9	VD2_BOT	Drain bias, stage 2 bottom. Refer to page 15 for bypassing network.
10	VD1_BOT	Drain bias, stage 1 bottom. Refer to page 15 for bypassing network.
11	VG3_BOT	Gate bias, stage 3 bottom. Refer to page 15 for bypassing network.
12	VG12_BOT	Gate bias, stages 1&2 bottom. Refer to page 15 for bypassing network.
13	GND	Backside ground to be attached to the PCB ground plane

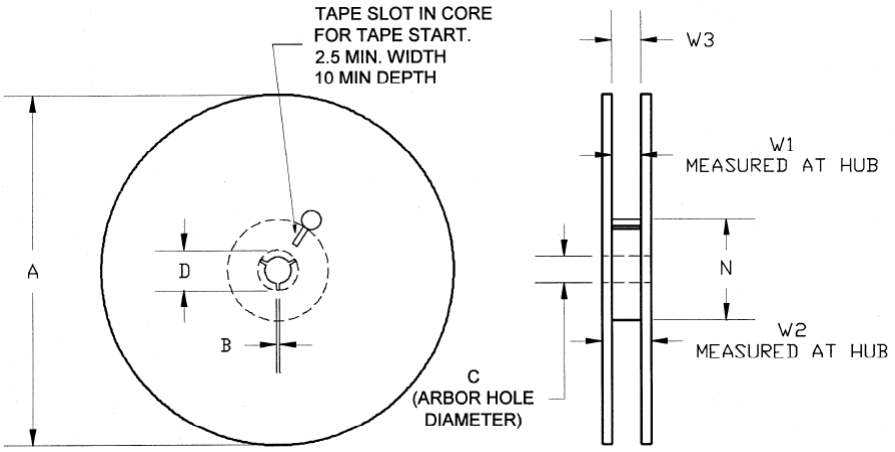
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.208	5.3
	Width	B0	0.208	5.3
	Depth	K0	0.079	2.0
	Pitch	P1	0.315	8.0
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.0
	Cavity to Perforation - Width Direction	F	0.217	5.5
Cover Tape	Width	C	0.362	9.2
Carrier Tape	Width	W	0.472	12

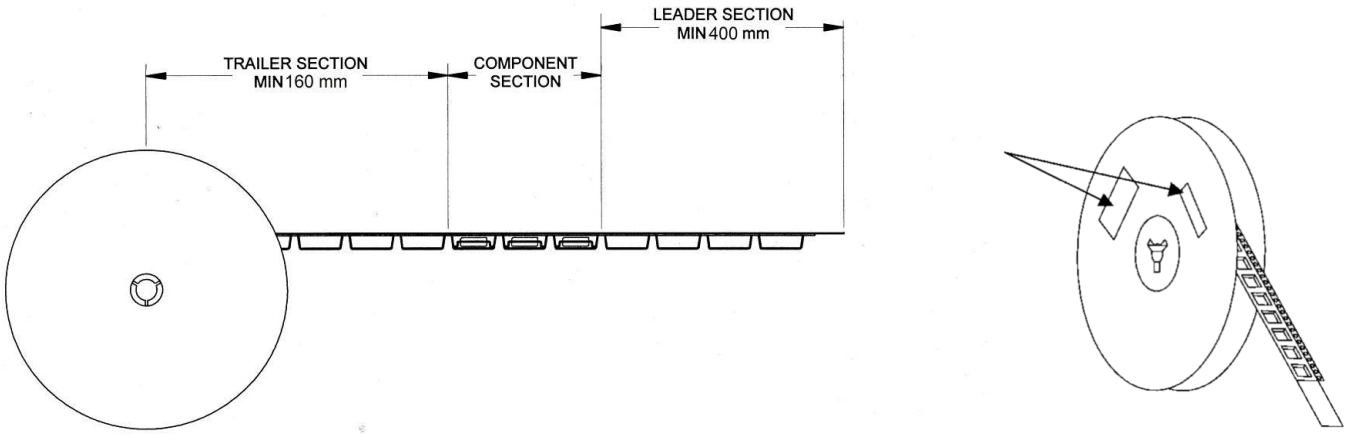
Tape and Reel Information – Reel Dimensions

Standard T/R size = 500 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.724	18.4
	Space Between Flange	W1	0.488	12.4
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.795	20.2

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESD/JEDEC JS-001
ESD – Charge Device Model (CDM)	C3	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	MSL5a	JEDEC IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Soldering of the component leads is compatible with the latest version of J-STD-020, lead-free solder, 260 °C. The use of no-clean solder to avoid washing after soldering is recommended.

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. **THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.**

Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Qorvo:

QPA4003EVB01 QPA4003TR7 QPA4003