TQC9312

3.3 – 3.8 GHz ½ W Digital Variable Gain Amplifier

Applications

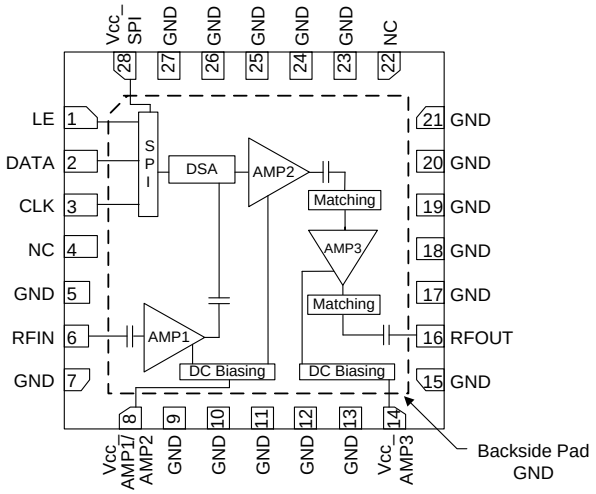
- 3G / 4G Wireless Infrastructure
- Repeaters
- Small cells

28-pin 6x6 mm leadless SMT package

Product Features

- 3.3 – 3.8 GHz Frequency Range
- 40 dB Gain (min attenuation state) at 3.5 GHz
- 31.5 dB Gain Range in 0.5 dB Steps
- +44.5 dBm Output IP3
- +27.8 dBm Output P1dB
- Fully Internally Matched Module
- Integrated Blocking Capacitors, Bias Inductors
- 3-wire SPI™ Control Programming

Functional Block Diagram



General Description

The TQC9312 is a digital variable gain amplifier (DVGA) featuring high linearity over the entire gain control range. This amplifier module integrates two gain blocks, a digital-step attenuator (DSA), and a high linearity ½ W amplifier. The module has the added feature of integrating all matching components, bias chokes and blocking capacitors. The internal 6-bit DSA provides a 31.5 dB gain control range in 0.5 dB steps, and is controlled with a serial periphery interface (SPI™).

The TQC9312 features variable gain from 9 dB to 40dB at 3.5 GHz, +44.5 dBm output IP3, and +27.8 dBm P1dB. The module operates from a single +5V supply and is available in a compact 28-pin 6x6 mm leadless SMT package.

The TQC9312 is pin compatible with the TQM879008 (1.5-2.7GHz, 0.5W P1dB) and TQM879006A (1.4-2.7GHz, 0.25W P1dB). This allows one to size the right type of device for specific system level requirements as well as making the DVGA family ideal for applications where a common PCB layout is used for different frequency bands.

Pin Configuration

Pin No.	Label
1	LE
2	DATA
3	CLK
4, 22	NC
6	RFIN
8	VCC_AMP1 / AMP2
14	VCC_AMP3
16	RFOUT
28	VCC_SPI
5, 7, 9-13, 15,17-21, 23-27	GND
Backside Pad	GND

Ordering Information

Part No.	Description
TQC9312	3.3-3.8 GHz DVGA
TQC9312-PCB	Fully Assembled Evaluation Board Includes USB control board

Standard T/R size = 2500 pieces on a 13” reel.

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to +150°C
RF Input Power, 50Ω,T = 25°C	+23 dBm
V_{DD}, Power Supply Voltage	+5.5 V
Digital Input Voltage	V_{CC}+0.5V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{CC} (pins 8, 14, 28)	+4.75	+5.0	+5.25	V
Case Temperature	−40		+85	°C
Tj (for>10^6 hours MTTF)			170	°C

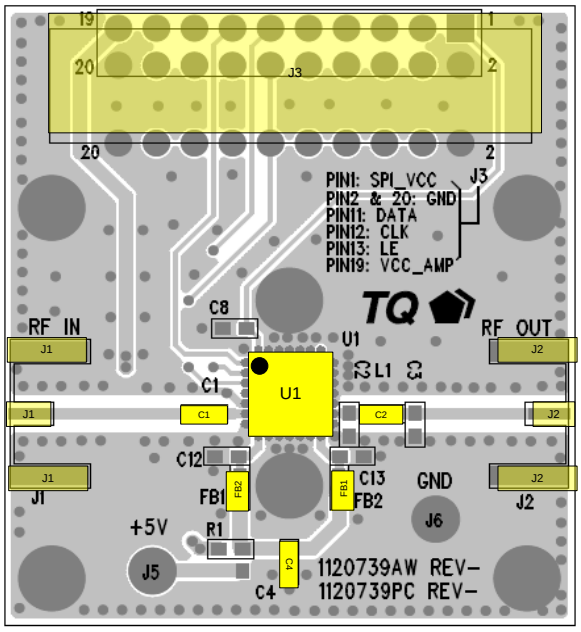
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

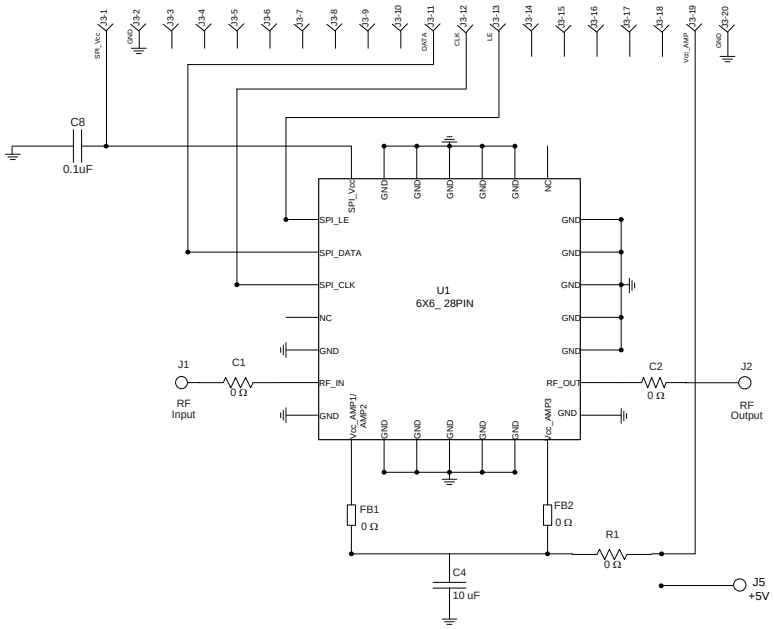
Electrical Specifications

Test conditions: V_{CC}=+5 V, $V_{CC\text{-}SPI}$ = +5V, Temp= +25°C, 50Ω system, Maximum Gain State

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		3300		3800	MHz
Test Frequency			3500		MHz
Gain		37	40	43	dB
Gain Control Range	0.5 dB Step Size		31.5		dB
Attenuation Accuracy	3 wire SPI, major states	± (0.5 + 8% of Atten. Setting) Max			dB
Control Interface	3-wire SPI		6		Bits
Input Return Loss			15		dB
Output Return Loss			17.4		dB
Output P1dB			+27.8		dBm
Output IP3	Pout =+11 dBm/tone, Δf=1MHz	+39	+44.5		dBm
Noise Figure			4		dB
I/O Impedance			50		Ω
Supply Voltage	AMP1, AMP2, AMP3		+5		V
Supply Current		220	285	320	mA
Thermal Resistance, θ_{jc}	Module (junction to case)			20.5	°C/W

TQC9312-PCB Evaluation Board





Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. All Components are of 0603 size unless stated otherwise.
3. See Serial Control Interface section for SPI Timing Diagram.
4. 0 Ω jumpers may be replaced with copper traces in the target application layout.
5. Different ground pins are used for SPI (digital) and analog supply voltages.
6. The primary RF microstrip characteristic line impedance is 50 Ω.
7. The single power supply is used to provide supply voltage to AMP1, AMP2 and AMP3.

Bill of Material –TQC9312-PCB

Reference Des.	Value	Description	Manufacturer	Part Number
U1		3.5 GHz ½ W DVGA	TriQuint	TQC9312
C8	0.1 uF	Cap, Chip, 0603, 16V, X7R, 10%	various	
C4	10 uF	Cap, Chip, 0603, 6.3V, X5R, 20%	various	
C1, C2, FB1, FB2	0 Ω	Res, Chip, 0603, 1/16W, 5%	various	

Typical Performance – TQC9312-PCB

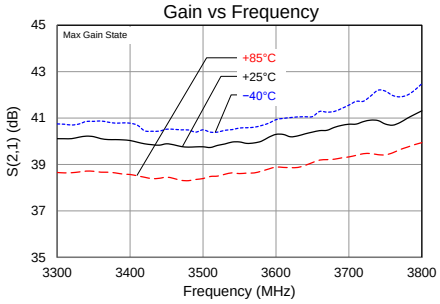
Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CC} = 285mA, Temp=25°C, 50 Ω system, Maximum Gain State

Parameter	Typical Value						Units
Frequency	3300	3400	3500	3600	3700	3800	GHz
Gain	40.1	40	39.8	40.3	40.7	41.3	dB
Input Return Loss	17	17.8	15	12.6	12.6	14	dB
Output Return Loss	17	17.5	17.4	17.4	15.6	14.8	dB
Output P1dB	+28.3	+28.2	+27.8	+27.5	+27.1	+26.7	dBm
Output IP3 (Pout=+11 dBm/tone, Δf =1 MHz)	+43.4	+43.4	+44.5	+44	+46	+44	dBm

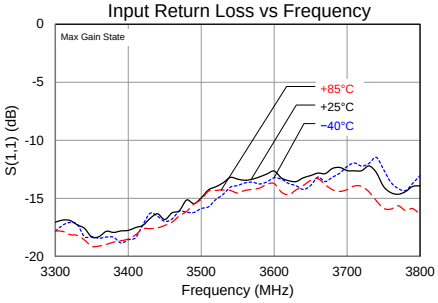
Typical Performance Plots – TQC9312-PCB

Test conditions unless otherwise specified: V_{CC}=+5 V, I_{CC} = 285mA, Temp= +25°C, 50Ω system

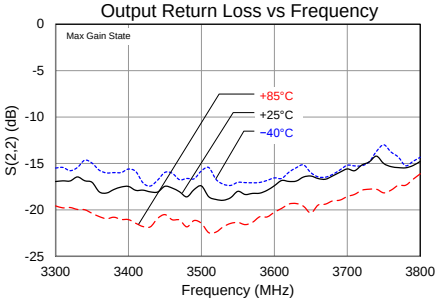
Gain vs Frequency



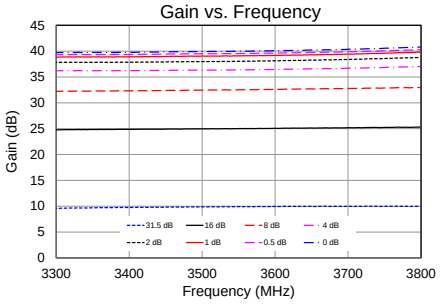
Input Return Loss vs Frequency



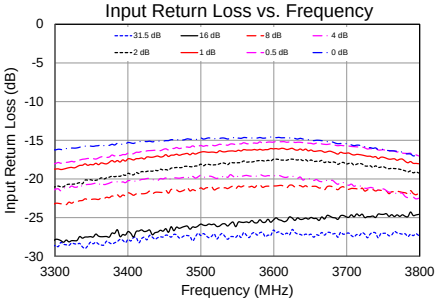
Output Return Loss vs Frequency



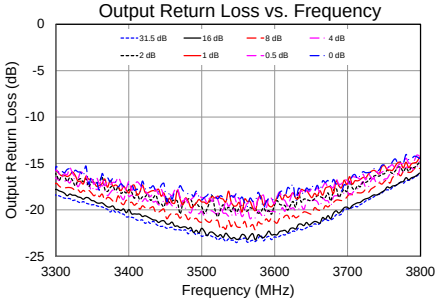
Gain vs. Frequency



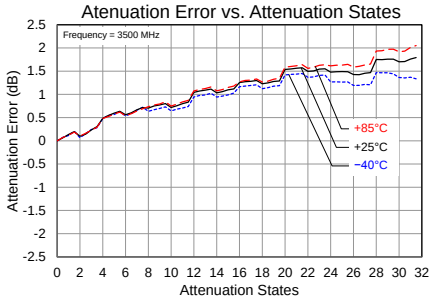
Input Return Loss vs. Frequency



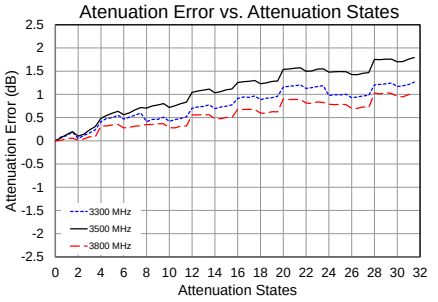
Output Return Loss vs. Frequency



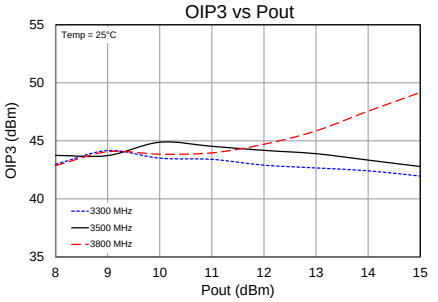
Atenuation Error vs. Attenuation States



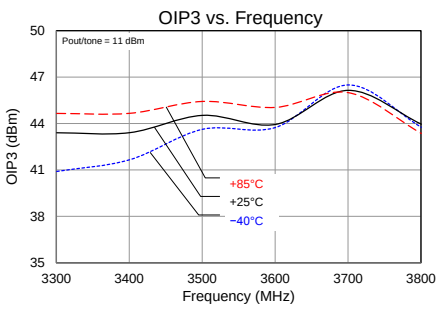
Atenuation Error vs. Attenuation States



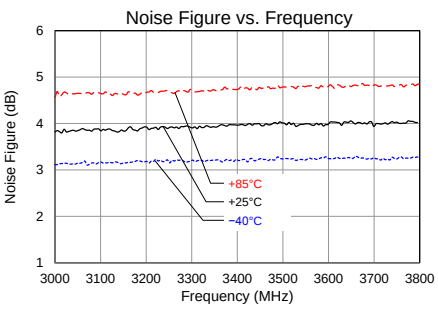
OIP3 vs Pout



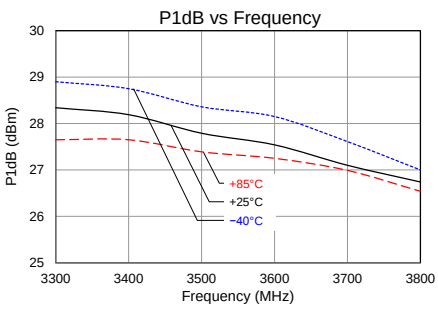
OIP3 vs. Frequency



Noise Figure vs. Frequency



P1dB vs Frequency



Serial Control Interface

The TQC9312 has a CMOS SPI™ input compatible serial interface. This serial control interface converts the serial data input stream to parallel output word. The input is 3-wire (CLK, LE and SID) SPI™ input compatible. At power up, the serial control interface resets the DSA to the minimum gain state. The 6-bit SID (Serial Input Data) word is loaded into the register on rising edge of the CLK, MSB first. When LE is high, CLK is internally disabled.

Serial Control Timing Characteristics (Test conditions: V_{CC} = +5 V, Temp.=25°C)

Parameter	Condition	Min	Max	Units
Clock Frequency	50% Duty Cycle		20	MHz
LE Setup Time, t_{LESUP}	after last CLK rising edge	10		ns
LE Pulse Width, t_{LEPW}		16		ns
SERIN set-up time, t_{SDSUP}	before CLK rising edge	8		ns
SERIN hold-time, t_{SDHLD}	after CLK rising edge	8		ns
LE Pulse Spacing t_{LE}	LE to LE pulse spacing	630		ns
Propagation Delay t_{PLO}	LE to Parallel output valid	10		ns

Serial Control DC Logic Characteristics (Test conditions: V_{CC} = +5 V, Temp.=25°C)

Parameter	Condition	Min	Max	Units
Input Low State Voltage, V_{IL}		0	0.8	V
Input High State Voltage, V_{IH}		1.8	V_{CC}	V
Input Current, I_{IH} / I_{IL}	On SID, LE and CLK pins	−10	+10	µA

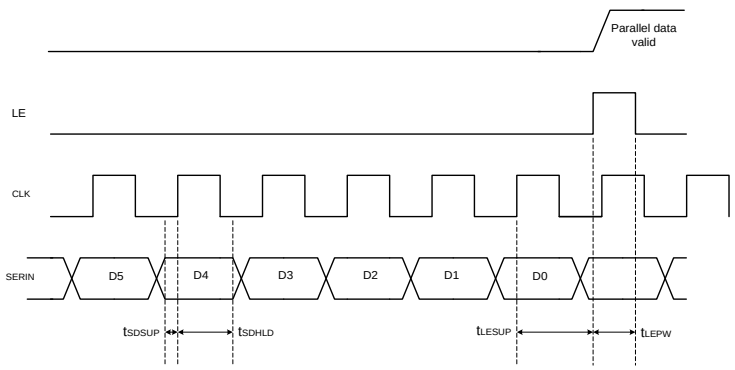
SERIN Control Logic Truth Table

6-Bit Control Word						Attenuation State
MSB					LSB	
D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	Reference : IL
1	1	1	1	1	0	0.5 dB
1	1	1	1	0	1	1 dB
1	1	1	0	1	1	2 dB
1	1	0	1	1	1	4 dB
1	0	1	1	1	1	8 dB
0	1	1	1	1	1	16 dB
0	0	0	0	0	0	31.5 dB

Any combination of the possible 64 states will provide an attenuation of the sum of bits selected.

Timing Diagram

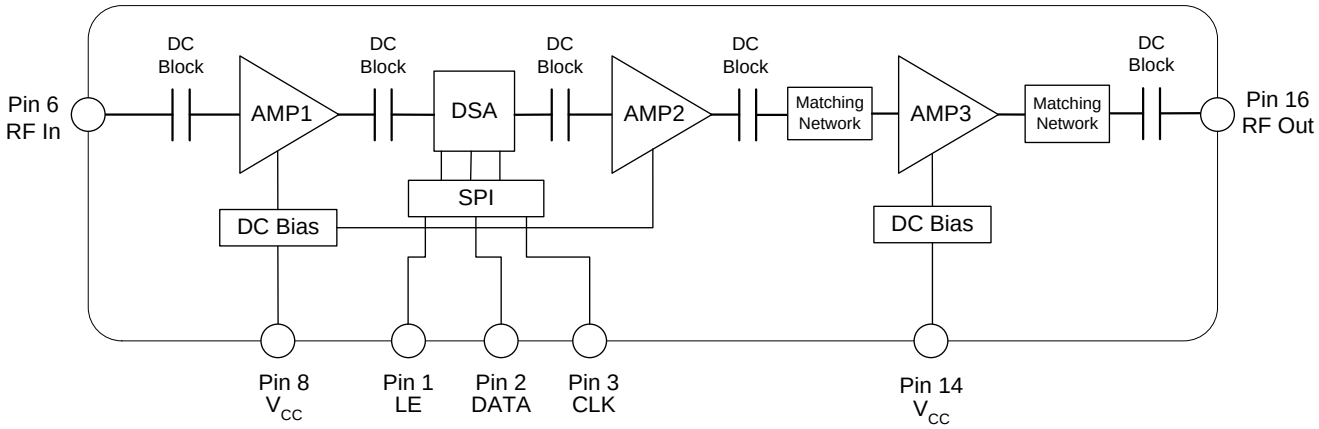
CLK is internally disabled when LE is high



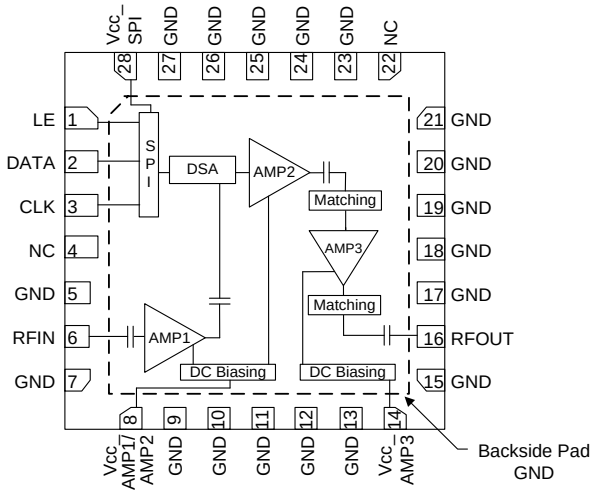
Detailed Device Description

The TQC9312 is a 50 Ω internally matched digital variable gain amplifier (DVGA) featuring high linearity over the entire gain control range. The amplifier module features the integration of two gain block, a digital-step attenuator (DSA), along with a high linearity ½ W amplifier. The module is unconditionally stable. Internal blocking capacitors and bias structures keep external parts count to a minimum. The DVGA is optimized for Band 41.

Functional Block Diagram



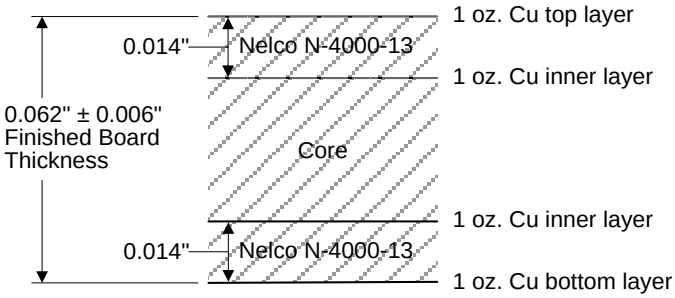
Pin Configuration and Description



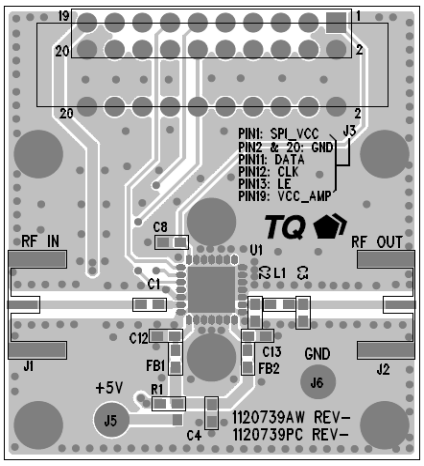
Pin No.	Label	Description
1	LE	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
2	DATA	Serial data input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
3	CLK	Serial clock input.
4, 22	N/C	No connect or open. This pin is not connected in this module
6	RFIN	Input, matched to 50 ohms. Internally DC blocked.
8	VCC_AMP1/ AMP2	Supply Voltage to AMP1 and AMP2. This pin is connected internally to bypass capacitors followed by inductor inside the module.
14	VCC_AMP3	Supply Voltage to AMP3. This pin is connected internally to bypass capacitors followed by inductor inside the module.
16	RFOUT	Output matched to 50 ohms. Internally DC blocked.
28	VCC_SPI	SPI and DSA DC supply. This pin is connected to bypass capacitor internally.
5, 7, 9-13, 15,17-21, 23-27	GND	RF/DC Ground Connection
Backside Pad	GND	RF/DC Ground Connection

Evaluation Board PCB Information

TriQuint PCB 1120739 Material and Stack-up

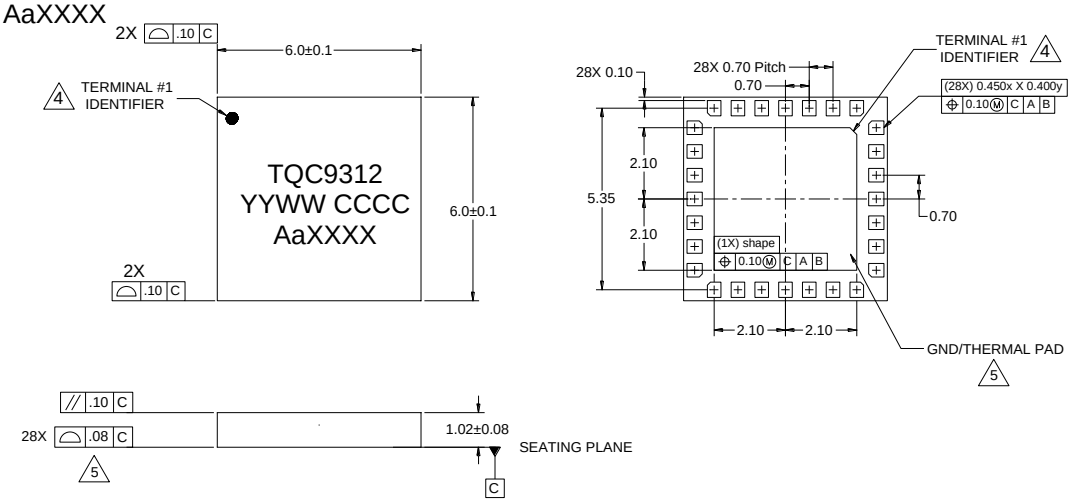


Microstrip line details: width = .030”, spacing = .036”.



Package Marking and Dimensions

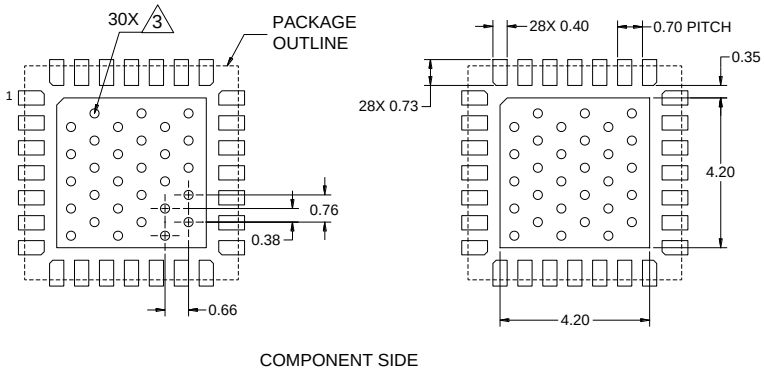
Marking: Part number – TQC9312
Year/week code – YYWW CCCC
Assembly code– AaXXXX



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
4. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.
5. Package body length/width does not include plastic flash protrusion across mold parting line.

PCB Mounting Pattern



COMPONENT SIDE

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: 1C
Value: Passes ≥1000V to < 2000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: C3
Value: Passes ≥ 1000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 3
Test: +260 °C convection reflow
Standard: JEDEC standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C max. reflow temp.) and tin/lead (245 °C max. reflow temp.) soldering processes.

Package lead plating: electrolytic plated Au over Ni

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.triquint.com **Tel: 877-800-8584**
Email: customer.support@qorvo.com

For information about the merger of RFMD and TriQuint as Qorvo:

Web: www.qorvo.com

For technical questions and application information:

Email: sjcapplications.engineering@qorvo.com

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