

## Overview

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Qorvo's PAC5524EVK1 development platform is a complete hardware solution enabling users not only to evaluate the PAC5524 device, but also develop power applications revolving around this powerful and versatile ARM® Cortex®-M4F based microcontroller. The module contains a PAC5524 Power Application Controller® (MCU) and all the necessary circuitry to properly energize the MCU and its internal peripherals once power is applied.

To aid in the application development the PAC5524EVK1 offers access to each and every one of the PAC5524 device's signals by means of a series of male header connectors.

The PAC5524EVK1 also contains access to an external USB to UART module enabling users to connect the evaluation module to a PC computer through a conventional Virtual Comm Port which can then be used in the communication efforts by taking advantage of the PAC5524's UART interface. Graphical User Interface (GUI) software suites can be employed to externally control particular application's features.

Finally, the PAC5524EVK1 module gives access to the PAC5524's SWD and JTAG ports allowing users to both program the application into the device's FLASH memory, as well as debug the application in real time. The provided 4 pin connector is compatible with a decent variety of SWD based debugger/programmer modules, widely available. In parallel, a MIPI20 connector is made available to provide JTAG with TRACE functionality, greatly expanding the existent debugging capabilities.

Active-Semi's PAC5524EVK1 evaluation kit consists of the following:

- PAC5524EVK1 Body module
- PAC5524EVK1 User's Guide
- Schematics, BOM and Layout Drawings

## PAC5524EVK1 Evaluation Module

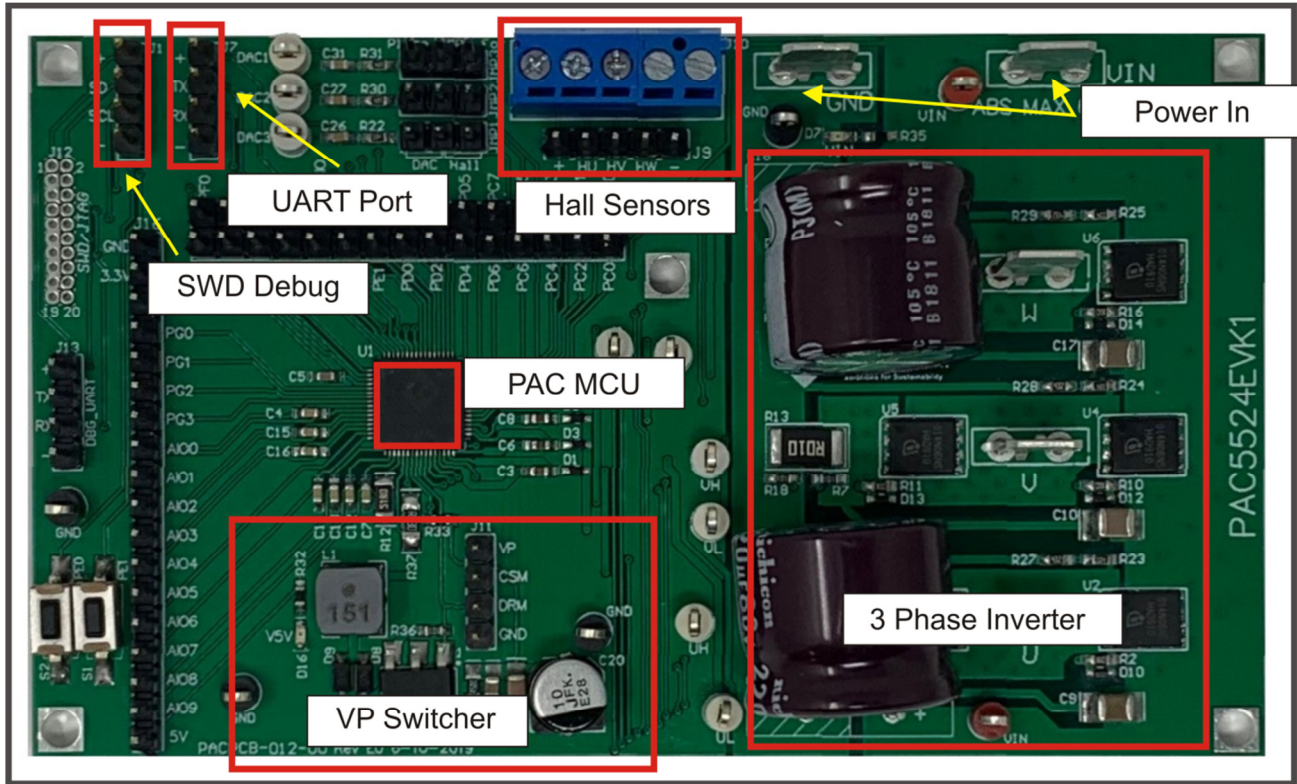


Figure 1: PAC5524EVK1 Block Diagram

### Solution Benefits:

- Ideal for high voltage (up to 60V Abs Max) general purpose power applications and controllers
- Single-IC PAC5524 with configurable PWM outputs, ADC inputs, I2C, UART, SPI communication ports and GPIO.
- Gate driving for up to three half H Bridge (tri phase) inverter.
- Schematics, BOM, Layout drawings available

The following sections provide information about the hardware features of Active-Semi's PAC5524EVK1 turnkey solution.



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## PAC5524EVK1 Resources

### Pinout and Signal Connectivity

The following diagram shows the male header pinout for the PAC5524EVK1 evaluation module, as seen from above:

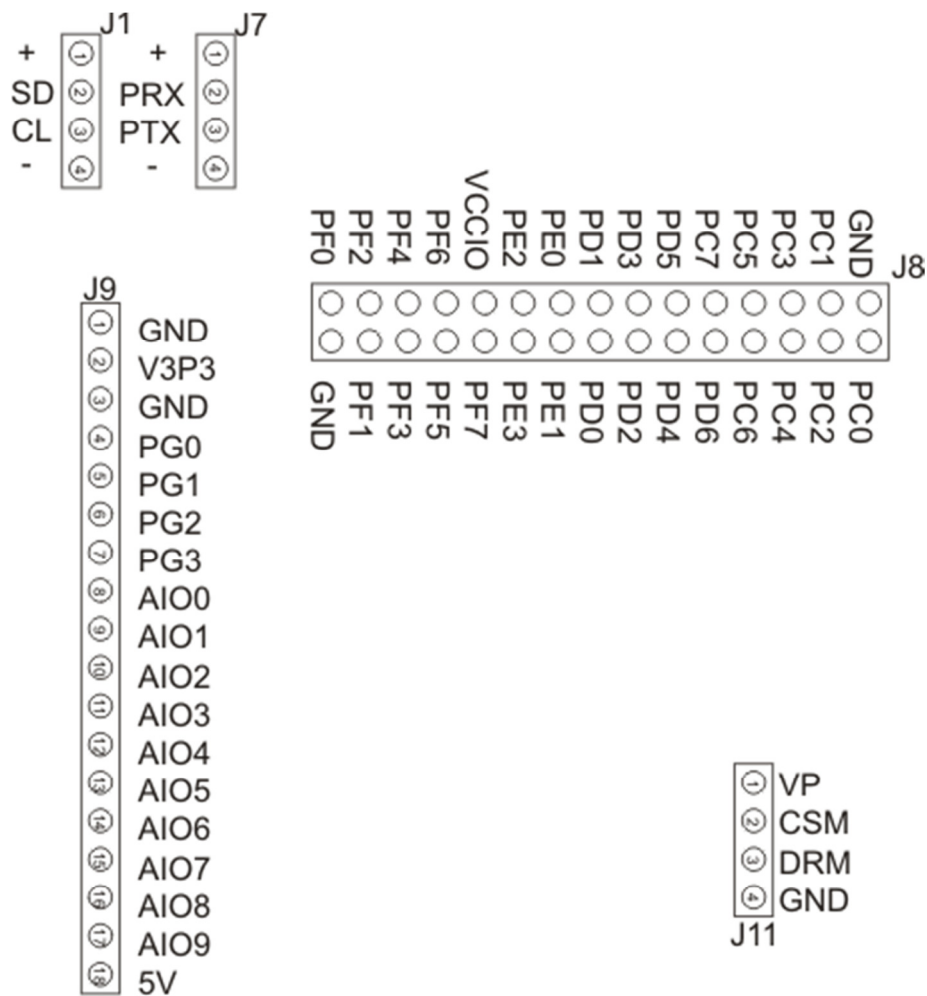


Figure 2 PAC5524EVK1 Headers and Test Stakes Pinout

## Power Input

Power to the PAC5524EVK1 evaluation module can be applied to the VIN and GND spade connectors. Power to the PAC5524EVK1 evaluation module should not exceed 60V (Abs Max).

The PAC5524EVK1 is optimized to operate with voltages ranging from 14V to 36V Nominal (60V Abs Max). When the VIN input voltage goes above 8V, the system exits UVLO protection and all subsystems, including voltage regulators, analog front end and microcontroller, are enabled.

## LED's

When an operational voltage is applied, LED D16 will light up. This is the LED which notifies VSYS (5V) rail is up and running. VP (12V gate drive), 3.3V (for analog circuitry) and 1.2V (for CPU core) regulators will also be operating at this point in time. Module is ready for use.

The following table shows the available LEDs and their associated diagnostic function.

LED	Description
D16	VSYS (5V). Light up when the PAC5524 device is successfully powered up by VIN.
D7	VIN. Lights up as VIN voltage is applied.

## SWD Debugging

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Connector J1 offers access to the PAC5524 SWD port lines.

J1 Pin	Terminal	Description
1	+	VCCIO (3.3V)
2	SD	SWD Serial Data
3	CL	SWD Serial Clock
4	-	GND (System Ground)

### JTAG Debugging

Connector J12 is a standard MIPI20 offering access to the JTAG port as well as single data line TRACE debug.

J12 Pins	Terminal	Description
1	VCC	VCC Power
2	SWDIO/TMS	Serial Wire Debug Data Input Output / JTAG Test Mode Select
3	GND	GND (System GND)
4	SWCLK/TCK	Serial Wire Debug Clock / JTAG Clock
5	GND	GND (System GND)
6	SWO/TDO	Serial Wire Debug Output / JTAG Data Output
7	NC	Not Connected
8	TDI	JTAG Data Input
9	GND	GND (System GND)
10	NC	Not Connected
11	GND	GND (System GND)
12	TRACE CLK	ETM Trace Clock
13	GND	GND (System GND)
14	TRACE DATA 0	ETM Trace Data 0
15	GND	GND (System GND)
16	NC	Not Connected
17	GND	GND (System GND)
18	NC	Not Connected
19	GND	GND (System GND)
20	NC	Not Connected

### Serial Communications

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Connector J7 offers access to the PAC5524 UART port lines.

J7 Pin	Terminal	Description
1	+	VCCIO (3.3V)
2	TX	MCU Transmit Line (PE3)
3	RX	MCU Receive Line (PE2)
4	-	GND (System Ground)

### Alternate Serial Communications

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When enabled (R41 must be populated with a 0 Ohm resistor), connector J13 provides access to a secondary UART port lines.

J7 Pin	Terminal	Description
1	+	VCCIO (3.3V)
2	TX	MCU Transmit Line (PF3 – requires 0 ohm resistor R41 to be populated)
3	RX	MCU Receive Line (PF2)
4	-	GND (System Ground)



### Hall Sensor / DAC Interface

Connector J10 offers access to the PAC5524 resources on PORTC utilized for hall sensor based commutation. These resources can be alternatively utilized as PWM DAC outputs for in real time debugging. Jumpers J14/15/16 are used to select the preferred function.

NOTE: 2 pin shunts must be placed on the J14/15/16 in order for the respective PORTC resources to be made available.

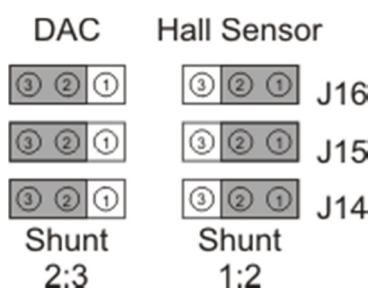


Figure 3 DAC / Hall Sensor Jumper Selection

Jumper JMP1/2/3	Description
1:2	Hall Sensor Functionality
2:3	DAC Functionality

NOTE: J10 functionality is only available when jumpers JMP1/2/3 have been shunted on the Hall Sensor respective position.

J10 Pin	Terminal	Description
1	+	VCCIO (3.3V)
2	Hall Sensor U	PORTC4
3	Hall Sensor V	PORTC5
4	Hall Sensor W	PORTC6
5	GND	GND (System Ground)

NOTE: Test stakes DAC1/2/3 are only available when jumpers JMP1/2/3 have been shunted on the DAC respective position

Test Stake	Description
DAC 1	PORTC4
DAC 2	PORTC5



DAC 3	PORTC6
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## PAC5524EVK1 Setup

The setup for the PAC5524EVK1 evaluation module requires up to four simple connections.

1. Connect the VIN power source via spade tab connectors VIN and GND. As VIN power is applied, the LED D7 will light up. Once VIN voltage goes above 8V, the PAC5524's Multi Mode Power Manager will be engaged and the VSYS (5V) regulator will be enabled. This event will result in LED D16 lighting up.
2. Connect the 3 Phase BLDC/PMSM motor via space tab connectors PHASE U, PHASE V and PHASE W.
3. If Serial Communications are desired, connect the USB to UART module 4 pin connection to J7.
4. For debugging/programming, connect a suitable USB SWD module to J1 by using a standard 4 wire cable.

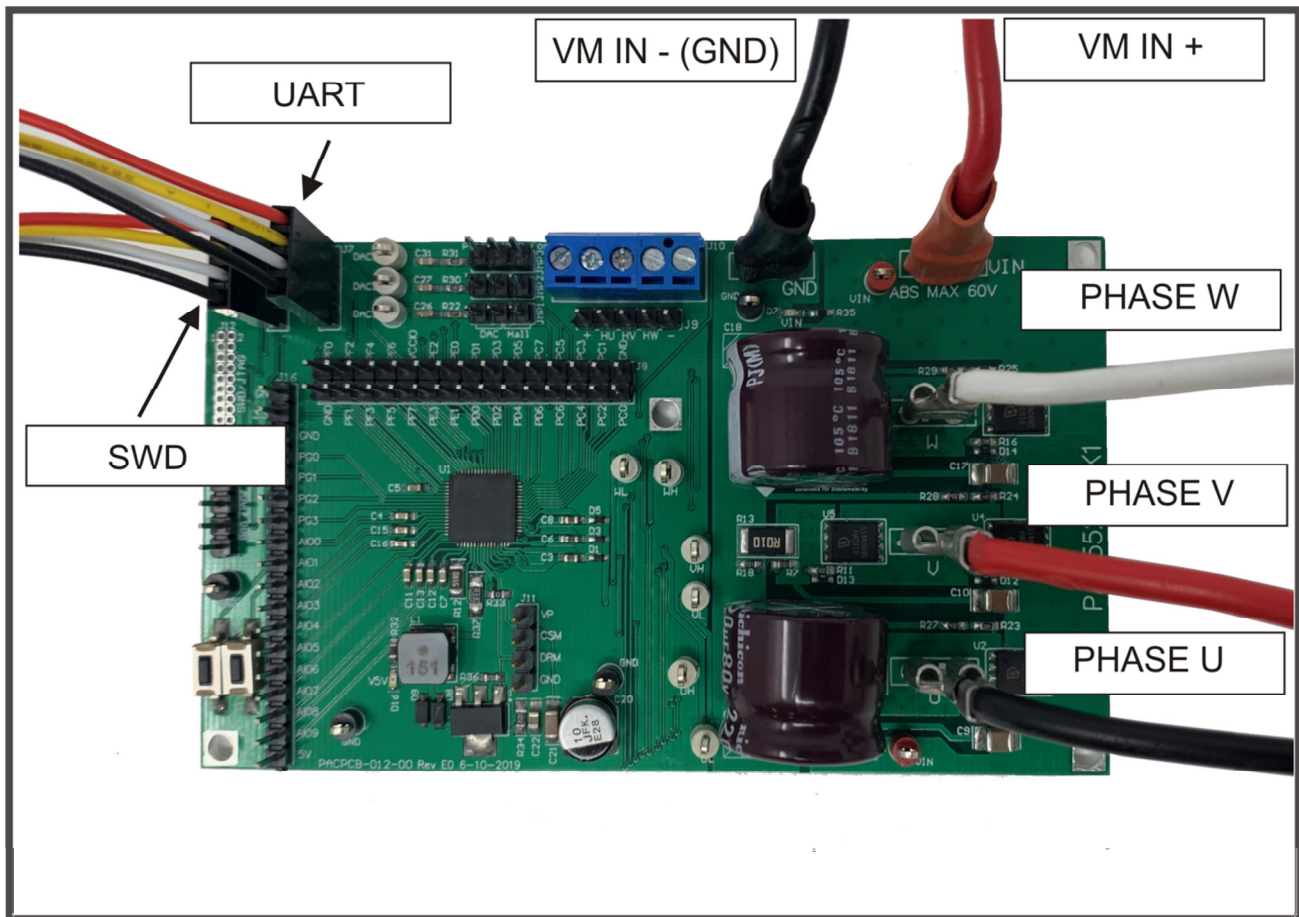


Figure 4: PAC5524EVK1 Evaluation Module Connections



## REVISION HISTORY

Revision	Description
UG270619	Initial draft

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Web:** [www.qorvo.com](http://www.qorvo.com)

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