PAC5523EVK1

Power Application Controllers

PAC5523EVK1 User's Guide

![active-semi logo]

Solutions for Sustainability

CONTENTS

OVERVIEW

Active-Semi's PAC5523EVK1 development platform is a complete hardware solution enabling users not only to evaluate the PAC5523 device, but also develop power applications revolving around this powerful and versatile ARM® Cortex®-M4F based microcontroller. The module contains a PAC5523 Power Application Controller® (MCU) and all the necessary circuitry to properly energize the MCU and its internal peripherals once power is applied.

To aid in the application development the PAC5523EVK1 offers access to each and every one of the PAC5523 device's signals by means of a series of male header connectors.

The PAC5523EVK1 also contains access to an external USB to UART module enabling users to connect the evaluation module to a PC computer through a conventional Virtual Comm Port which can then be used in the communication efforts by taking advantage of the PAC5523's UART interface. Graphical User Interface (GUI) software suites can be employed to externally control particular application's features.

Finally, the PAC5523EVK1 module gives access to the PAC5523's SWD and JTAG ports allowing users to both program the application into the device's FLASH memory, as well as debug the application in real time. The provided 4 pin connector is compatible with a decent variety of SWD based debugger/programmer modules, widely available. In parallel, a MIPI20 connector is made available to provide JTAG with TRACE functionality, greatly expanding the existent debugging capabilities.

Active-Semi's PAC5523EVK1 evaluation kit consists of the following:

- PAC5523EVK1 Body module
- PAC5523EVK1 User's Guide
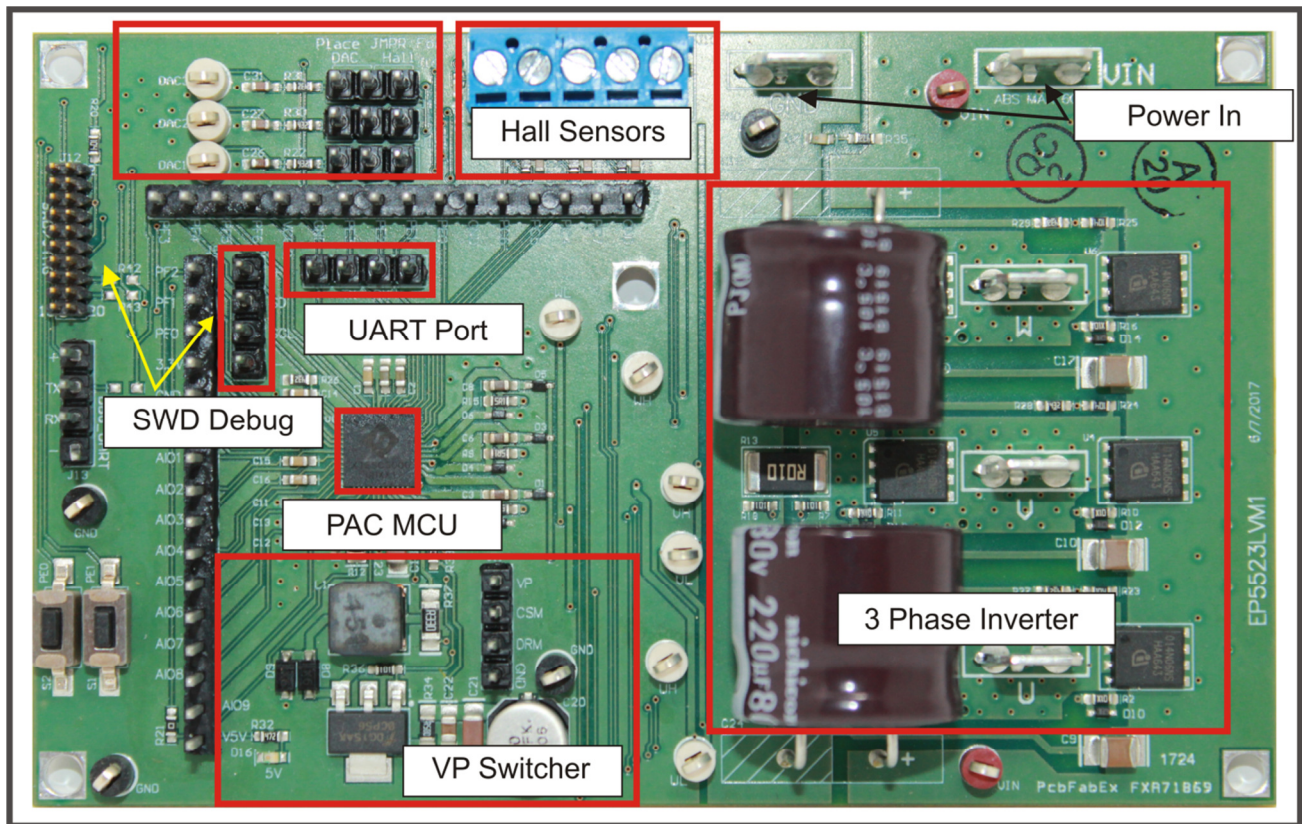- Schematics, BOM and Layout Drawings

Figure 1: PAC5523EVK1 Block Diagram

Solution Benefits:

- Ideal for high voltage (up to 60V Abs Max) general purpose power applications and controllers
- Single-IC PAC5523 with configurable PWM outputs, ADC inputs, I2C, UART, SPI communication ports and GPIO.
- Gate driving for up to three half H Bridge (tri phase) inverter.
- Schematics, BOM, Layout drawings available

The following sections provide information about the hardware features of Active-Semi's PAC5523EVK1 turnkey solution.

PAC5523EVK1 RESOURCES

Pinout and Signal Connectivity

The following diagram shows the male header pinout for the PAC5523EVK1 evaluation module, as seen from above:
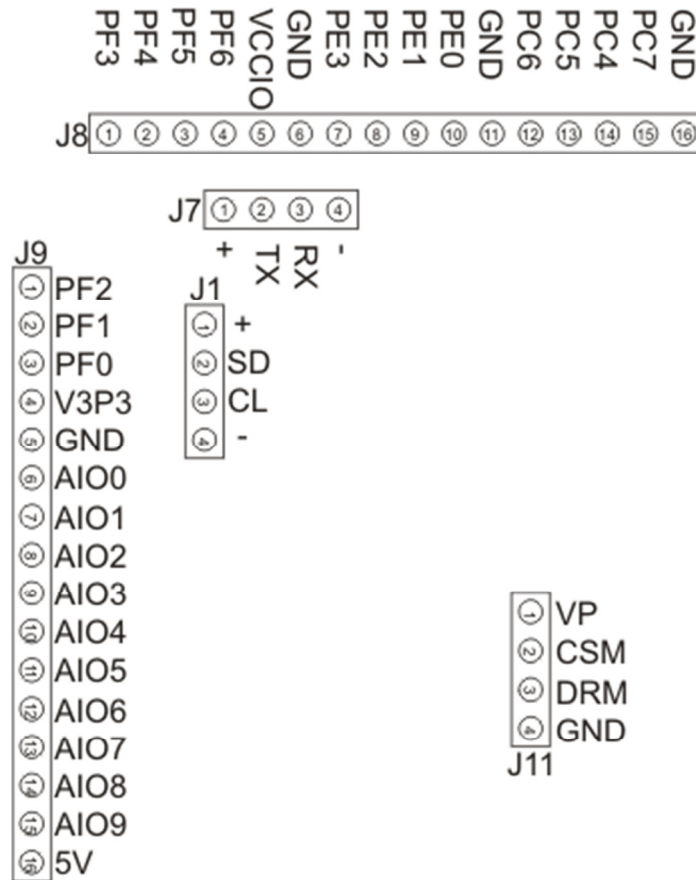

Figure 2 PAC5523EVK1 Headers and Test Stakes Pinout

Power Input

Power to the PAC5523EVK1 evaluation module can be applied to the VIN and GND spade connectors. Power to the PAC5523EVK1 evaluation module should not exceed 60V (Abs Max).

The PAC5523EVK1 is optimized to operate with voltages ranging from 14V to 36V Nominal (60V Abs Max). When the VIN input voltage goes above 8V, the system exits UVLO protection and all subsystems, including voltage regulators, analog front end and microcontroller, are enabled.

LED's

When an operational voltage is applied, LED D16 will light up. This is the LED which notifies VSYS (5V) rail is up and running. VP (12V gate drive), 3.3V (for analog circuitry) and 1.2V (for CPU core) regulators will also be operating at this point in time. Module is ready for use.

The following table shows the available LEDs and their associated diagnostic function.

LED	Description
D16	VSYS (5V). Light up when the PAC5523 device is successfully powered up by VIN.
D7	VIN. Lights up as VIN voltage is applied.

SWD Debugging

Connector J1 offers access to the PAC5523 SWD port lines.

J1 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	SD	SWD Serial Data
3	CL	SWD Serial Clock
4	-	GND (System Ground)

JTAG Debugging

Connector J12 is a standard MIPI20 offering access to the JTAG port as well as single data line TRACE debug.

J12 Pins	Terminal	Description
1	VCC	VCC Power
2	SWDIO/TMS	Serial Wire Debug Data Input Output / JTAG Test Mode Select
3	GND	GND (System GND)
4	SWCLK/TCK	Serial Wire Debug Clock / JTAG Clock
5	GND	GND (System GND)
6	SWO/TDO	Serial Wire Debug Output / JTAG Data Output
7	NC	Not Connected
8	TDI	JTAG Data Input
9	GND	GND (System GND)
10	NC	Not Connected
11	GND	GND (System GND)
12	TRACE CLK	ETM Trace Clock
13	GND	GND (System GND)
14	TRACE DATA 0	ETM Trace Data 0
15	GND	GND (System GND)
16	TRACE DATA 1	ETM Trace Data 1
17	GND	GND (System GND)
18	TRACE DATA 2	ETM Trace Data 2
19	GND	GND (System GND)
20	TRACE DATA 3	ETM Trace Data 3

Serial Communications

Connector J7 offers access to the PAC5523 UART port lines.

J7 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	TX	MCU Transmit Line (PE3)
3	RX	MCU Receive Line (PE2)
4	-	GND (System Ground)

Alternate Serial Communications

When enabled, connector J13 provides access to a secondary UART port lines.

J7 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	TX	MCU Transmit Line (PF3 – requires 0 ohm resistor R41 to be populated)
3	RX	MCU Receive Line (PF2)
4	-	GND (System Ground)

Hall Sensor / DAC Interface

Connector J10 offers access to the PAC5523 resources on PORTC utilized for hall sensor based commutation. These resources can be alternatively utilized as PWM DAC outputs for in real time debugging. Jumpers J14/15/16 are used to select the preferred function.

NOTE: 2 pin shunts must be placed on the J14/15/16 in order for the respective PORTC resources to be made available.
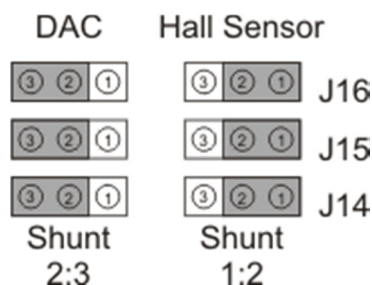
Figure 3 DAC / Hall Sensor Jumper Selection

Jumper J14/15/16	Description
1:2	Hall Sensor Functionality
2:3	DAC Functionality

NOTE: J10 functionality is only available when jumpers J14/15/16 have been shunted on the Hall Sensor respective position.

J10 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	Hall Sensor U	PORTC4
3	Hall Sensor V	PORTC5
4	Hall Sensor W	PORTC6
5	GND	GND (System Ground)

NOTE: Test stakes DAC1/2/3 are only available when jumpers J14/15/16 have been shunted on the DAC respective position

Test Stake	Description
DAC 1	PORTC4
DAC 2	PORTC5
DAC 3	PORTC6

PAC5523EVK1 SETUP

The setup for the PAC5523EVK1 evaluation module requires up to four simple connections.

1. Connect the VIN power source via spade tab connectors VIN and GND. As VIN power is applied, the LED D7 will light up. Once VIN voltage goes above 8V, the PAC5523's Multi Mode Power Manager will be engaged and the VSYS (5V) regulator will be enabled. This event will result in LED D16 lighting up.
2. Connect the 3 Phase BLDC/PMSM motor via space tab connectors PHASE U, PHASE V and PHASE W.
3. If Serial Communications are desired, connect the USB to UART module 4 pin connection to J7.
4. For debugging/programming, connect a suitable USB SWD module to J1 by using a standard 4 wire cable.
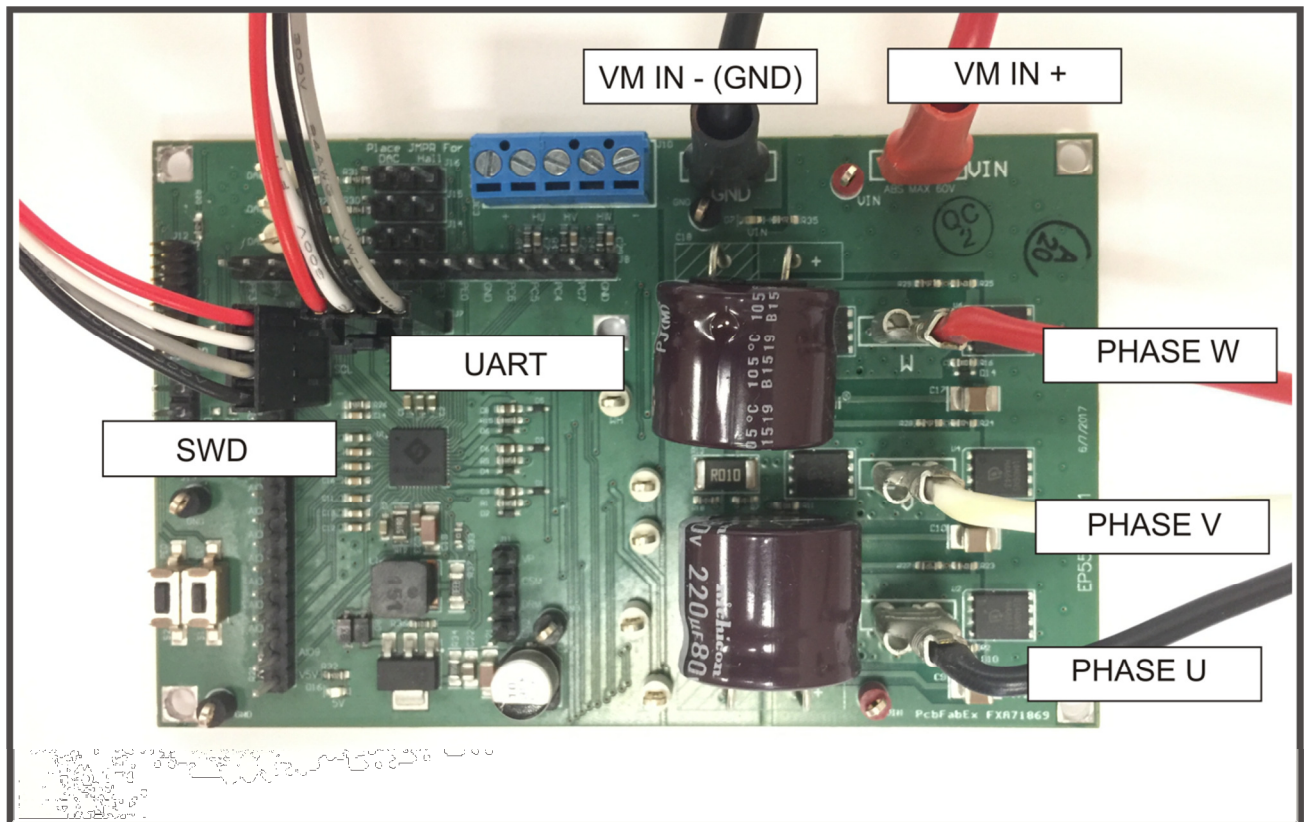
Figure 4: PAC5523EVK1 Evaluation Module Connections

ABOUT ACTIVE-SEMI

Founded in 2004 in Silicon Valley and headquartered in Allen, Texas, Active-Semi is a rapidly emerging leader in the multi-billion dollar power management IC and intelligent digital motor drive IC markets. The company's portfolio of analog and mixed signal SoCs (systems-on-chips) are scalable core platforms used in charging, powering and embedded digital control systems for end applications such as industrial, commercial and consumer equipment. The company offers power application microcontrollers, DC/DC, AC/DC, PMU and LED drivers that significantly reduce solution size and cost while improving system-level reliability. Active-Semi's turnkey solutions deliver energy-saving power conversion architectures that minimize energy usage and compress system development cycle-time by greater than 50 percent. Active-Semi ships 50 million power ICs per quarter and reached the "one billion units shipped" milestone in May 2012. The multi-national company focuses on commercializing industry leading power management IC solution platforms and has developed broad intellectual property with over 150 patents granted and pending. For more information visit: http://active-semi.com/

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Qorvo](#):
  [PAC5523EVK1](#)