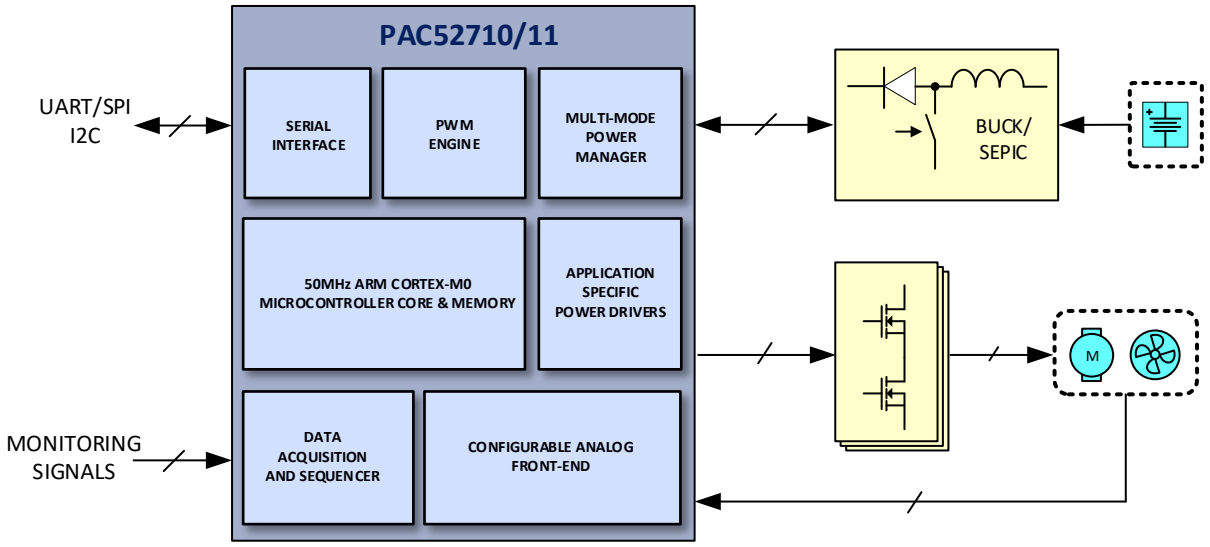
1 PRODUCT OVERVIEW

The PAC52710 belongs to Qorvo's broad portfolio of full-featured Power Application Controller® (PAC) products that are highly optimized for controlling and powering next generation smart energy appliances, devices, and equipment. These application controllers integrate a 50MHz Arm© Cortex®-M0 32-bit microcontroller core with Qorvo's proprietary and patent-pending Multi-Mode Power Manager™, Configurable Analog Front End™, and Application Specific Power Drivers™ to form the most compact microcontroller-based power and general purpose application systems ranging from digital power supply to motor control. The PAC52710/11 microcontroller features up to 32kB of embedded FLASH and 8kB of SRAM memory, a high-speed 10-bit 1µs analog-to-digital converter (ADC) with dual auto-sampling sequencers, 5V/3.3V I/Os, flexible clock sources, timers, a versatile 14-channel PWM engine, and several serial interfaces.

The Multi-Mode Power Manager (MMPM) provides “all-in-one” efficient power management solution for multiple types of power sources. It features a configurable multi-mode switching supply controller capable of operating in buck or SEPIC mode, and up to four linear regulated voltage supplies. The Application Specific Power Drivers (ASPD) are high-voltage power drivers designed for each target set of control applications, including half bridge, H-bridge, 3-phase, intelligent power module (IPM), and general purpose driving. The Configurable Analog Front End (CAFE) comprises differential programmable gain amplifiers, single-ended programmable gain amplifiers, comparators, digital-to-analog converters, and I/Os for programmable and inter-connectible signal sampling, feedback amplification, and sensor monitoring of multiple analog input signals. Together, these modules and microcontroller enable a wide range of compact applications with highly integrated power management, driving, feedback, and control for DC supply up to 70V.

APPLICATIONS

Power and Garden Tools
Electronic Speed Controllers (ESC)
e-Mobility – scooters, wheelchairs
Warehouse and Industrial Robotics



The PAC52710/11 is available in a 48-pin, 6x6 mm TQFN package. The PAC family includes a range of part numbers optimized to work with different targeted primary applications.

KEY FEATURES

- 50MHz Arm Cortex-M0 32-bit microcontroller core
  - Fast single cycle 32-bit x 32-bit multiplier
  - 24-bit SysTick timer
  - Nested vectored interrupt controller (NVIC) with 20 external interrupts
  - Wake-up interrupt controller allowing power-saving sleep modes
  - Clock-gating allowing low power operation
- 32kB FLASH and 8kB SRAM memory
- 10-bit 1µs ADC with multi-input/multi-sample control engine
  - 9 ADC inputs including input from configurable analog front end
- Proprietary Multi-Mode Power Manager
  - Multi-mode switching supply controller configurable for high-voltage buck SEPIC or AC/DC Flyback topologies
  - DC supply up to 70V or line AC input
  - 4 linear regulators with power and hibernate management
  - Power and temperature monitor, warning, and fault detection
- Proprietary Configurable Analog Front End
  - 10 analog front end I/O pins
  - 3 differential programmable gain amplifiers
  - 4 single-ended programmable gain amplifiers (PAC52710)
  - 1 single-ended programmable gain amplifier (PAC52711)
  - 10 comparators
  - 2 DACs (10-bit and 8-bit)
  - nBrake and nDRVDis for safety purposes (PAC52711)
- Proprietary Application Specific Power Drivers
  - 3 low-side and 3 high-side gate drivers with 1A gate driving capability
  - Configurable delays and fast fault protection
- Fully Programmable Over Current Protection Modes
  - 2 Over Current Protection Modes using SENSE resistor current sensing
  - Over Current Protection Mode using VDS Sensing
  - 2 modes of Cycle by Cycle PWM truncation for current regulation
- 3.3V I/Os
  - 3 general purpose I/Os with tri-state and dedicated analog input to ADC
- True 5V I/Os
  - 12 general purpose I/Os with tri-state, pull-up and pull-down and dedicated I/O supply
  - Configurable as true 5V or 3.3V I/Os
- Flexible clock and PLL from internal 2% oscillator, ring oscillator, external clock, or crystal
- 9 timing generators
  - Four 16-bit timers with up to 16 PWM/CC blocks and 7 independent dead-time controllers
  - 24-bit watchdog timer
  - 4s or 8s watchdog timer
  - 24-bit real time clock
  - 24-bit SysTick timer
  - Wake-up timer for sleep modes from 0.125s to 8s
- VDS Sensing for over current protection
- Configurable Cycle By Cycle (CBC) PWM truncation engine
- SPI, I^2C, and UART communication interfaces
- SWD debug interface with interface disable function

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2 PRODUCT SELECTION SUMMARY

Table 2-1 Product Selection Summary

PART NUMBER	PIN PKG	POWER MANAGER		CONFIGURABLE ANALOG FRONT END					APPLICATION SPECIFIC POWER DRIVERS			MICROCONTROLLER						PRIMARY APPLICATION
		INPUT VOLTAGE	MULTI-MODE SW	DIFF-PGA	PGA	COMPARATOR	DAC	ADC CHANNEL	POWER DRIVER	PWM CHANNEL	FAULT PROTECT	SPEED (MHz)	FLASH (kB)	SRAM (kB)	GPIO	INTERFACE	XTAL	
PAC52710	48-pin 6x6 TQFN	5.2-70V	Y	3	4	10	2	10	3 LS (1.2A/ 1.8A) 3 HS (1.2A/ 1.8A)	6	Int	50	32	8	25	SPI I^2C UART SWD	N	3 half bridge, 3-phase control
PAC52711	48-pin 6x6 TQFN	5.2-70V	Y	1	4	10	2	10	3 LS (1.2A/ 1.8A) 3 HS (1.2A/ 1.8A)	6	Int	50	32	8	25	SPI I^2C UART SWD	N	3 half bridge, 3-phase control

Notes: DIFF-PGA = differential programmable gain amplifier, GD = gate driver, HS = high-side , LS = low-side, OD = open-drain driver, PGA = programmable gain amplifier, UHV = ultra-high-voltage.

3 ORDERING INFORMATION

Table 3-1 Ordering Information

PART NUMBER[1]	TEMPERATURE RANGE	PACKAGE	PINS	PACKING
PAC52710QM-T	-40°C to 105°C	TQFN66-48	48 + Exposed Pad	Tape & Reel
PAC52710QMSR	-40°C to 105°C	TQFN66-48	48 + Exposed Pad	Tape & Reel
PAC52711QM-T	-40°C to 105°C	TQFN66-48	48 + Exposed Pad	Tape & Reel
PAC52711QMSR	-40°C to 105°C	TQFN66-48	48 + Exposed Pad	Tape & Reel

[1] See Product Selection Summary for product features for each part number.

4 ABSOLUTE MAXIMUM RATINGS

Table 4-1 Absolute Maximum Ratings

(Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

PARAMETER		VALUE	UNIT
VBUS, VHM, DRM to VSSP		-0.3 to 72	V
VP to VSS		-0.3 to 20	V
CSM, REGO to VSS		-0.3 to V_P + 0.3	V
VSYS, AIO6/.. to VSS		-0.3 to 6	V
VCC33 to VSS		-0.3 to 4.1	V
VCC18 to VSS		-0.3 to 2.5	V
AIOx/.. (except AIO6/..), VCCIO to VSS		-0.3 to V_{SYS} + 0.3	V
nDRVDIS, nBRAKE to VSS (PAC52711)		-0.3 to V_{SYS} + 0.3	V
PDx/.., PEx/.. to VSS		-0.3 to V_{CCIO} + 0.3	V
PCx/.. to VSSA		-0.3 to V_{CC33} + 0.3	V
PAx/.., PBx/.., PCx/.., PDx/.., PEx/.. pin injection current		7.5	mA
PAx/.., PBx/.., PCx/.., PDx/.., PEx/.. sum of all pin injection current		25	mA
DRLx to VSSP		-0.3 to V_P + 0.3	V
DRBx to VSSP		-0.3 to 84	V
DRSx to VSSP		-6 to 72	V
DRSx allowable offset slew rate (dV_{DRSx}/dt)		5	V/ns
DRBx, DRHx to respective DRSx		-0.3 to 20	V
VSSP, VSSA to VSS		-0.3 to 0.3	V
VSS, VSYS, DRM, DRLx, DRHx, REGO RMS current[1]		0.2	A_{RMS}
VSSP RMS current[1]		0.4	A_{RMS}
VP RMS current[1]		0.6	A_{RMS}
Operating temperature range		-40 to 105	°C
Electrostatic discharge (ESD)	Human body model (JEDEC)	2	kV
	Charge device model (JEDEC)	1	kV
	Machine model (JEDEC)	200	V

[1]Peak current can be 10 times higher than RMS value for pulses shorter than 10µs.

5 ARCHITECTURAL BLOCK DIAGRAM

Figure 5-1 PAC52710 Architectural Block Diagram

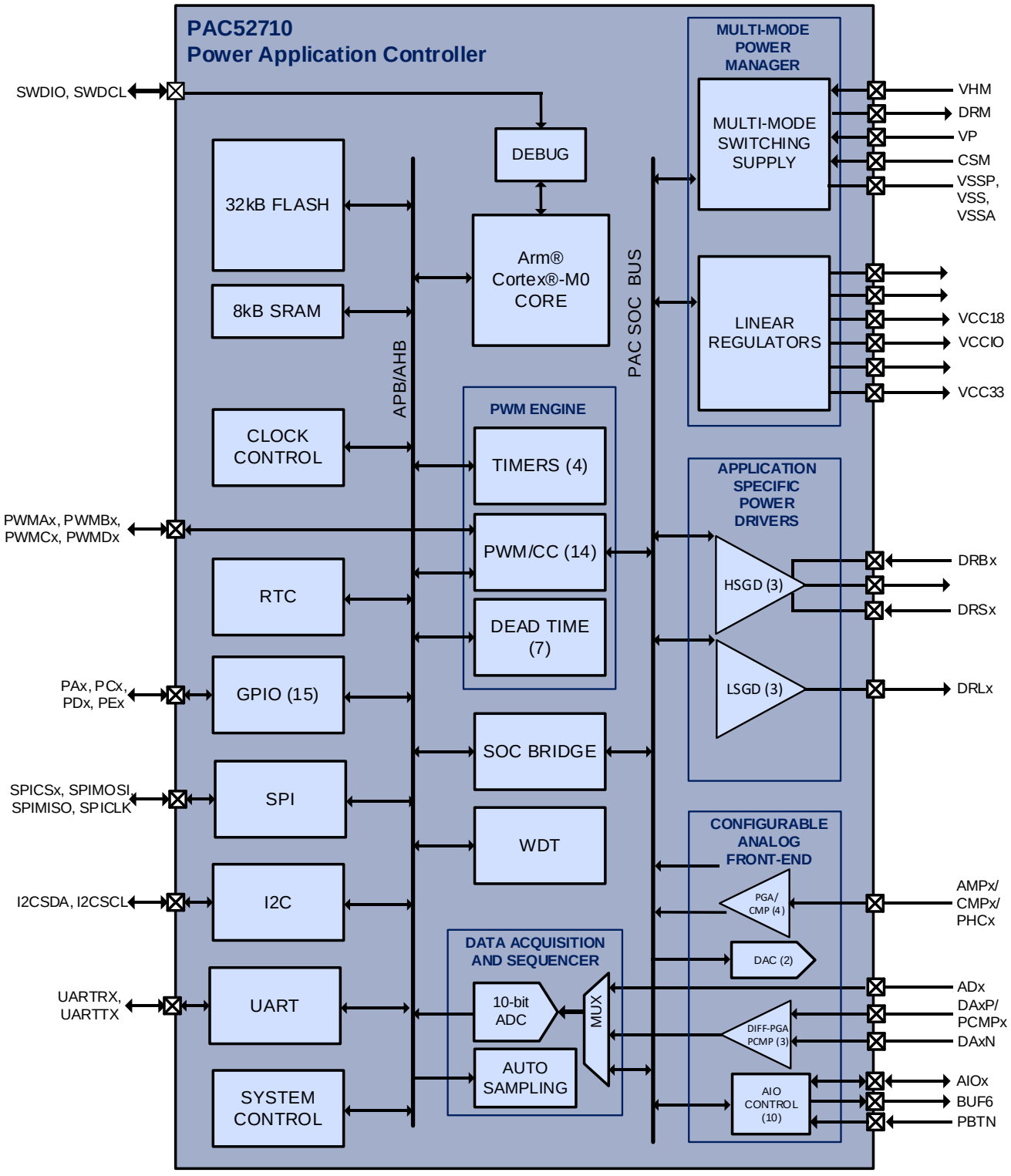
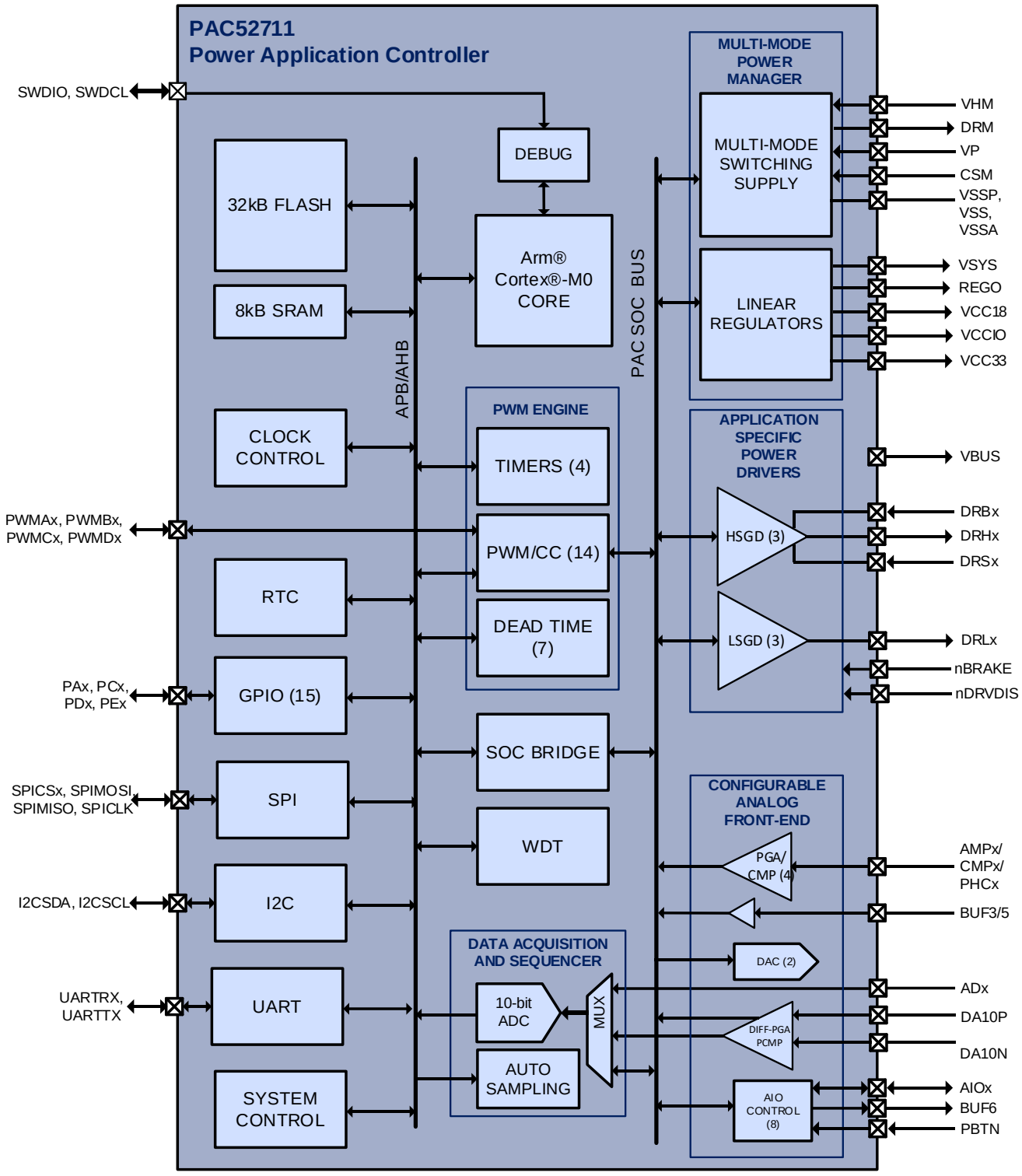


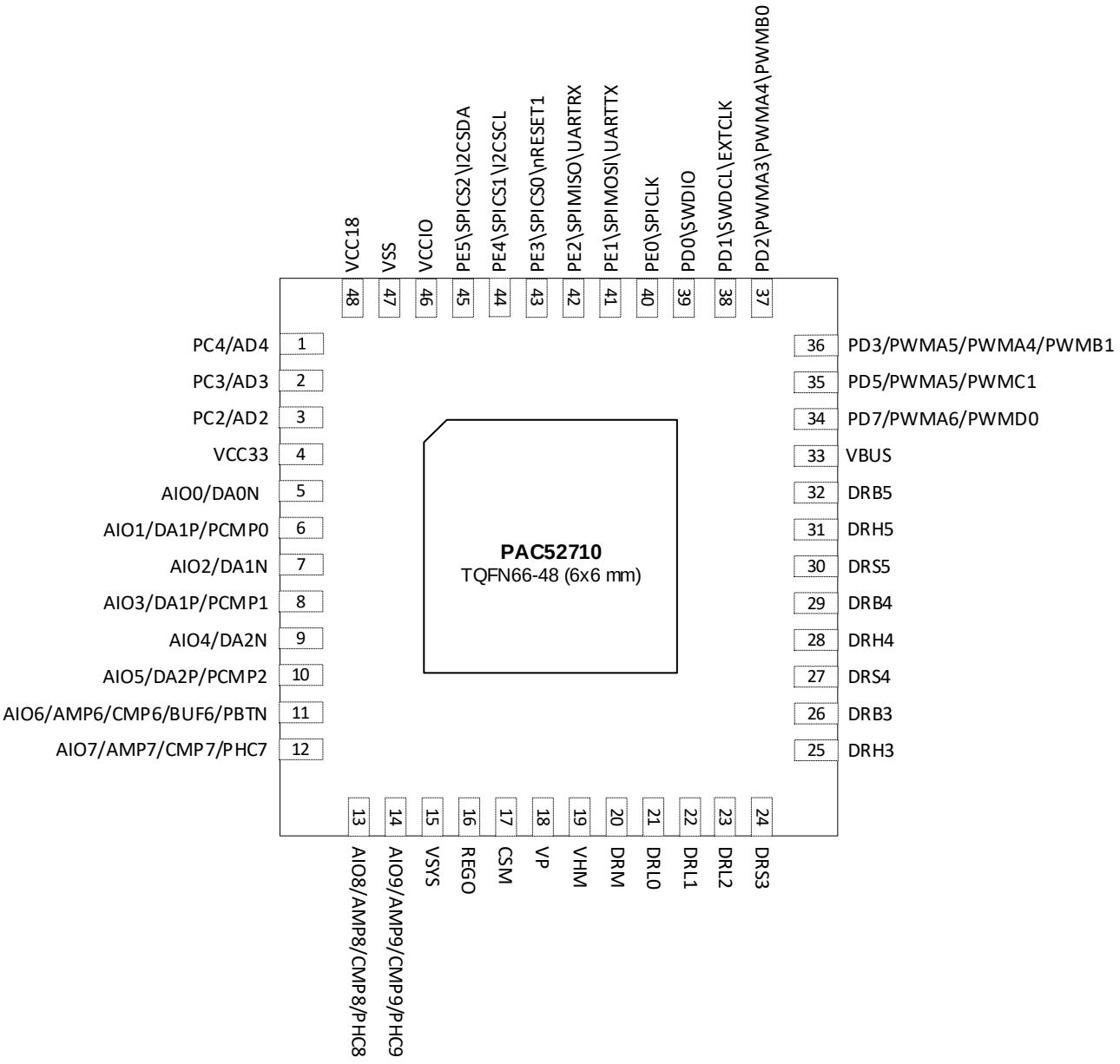
Figure 5-2 PAC52711 Architectural Block Diagram



6 PIN CONFIGURATION

6.1 PAC52710QM

Figure 6-1 PAC52710QM Pin Configuration (TQFN66-48 Package)



6.2 PAC52711QM

Figure 6-2 PAC52711QM Pin Configuration (TQFN66-48 Package)

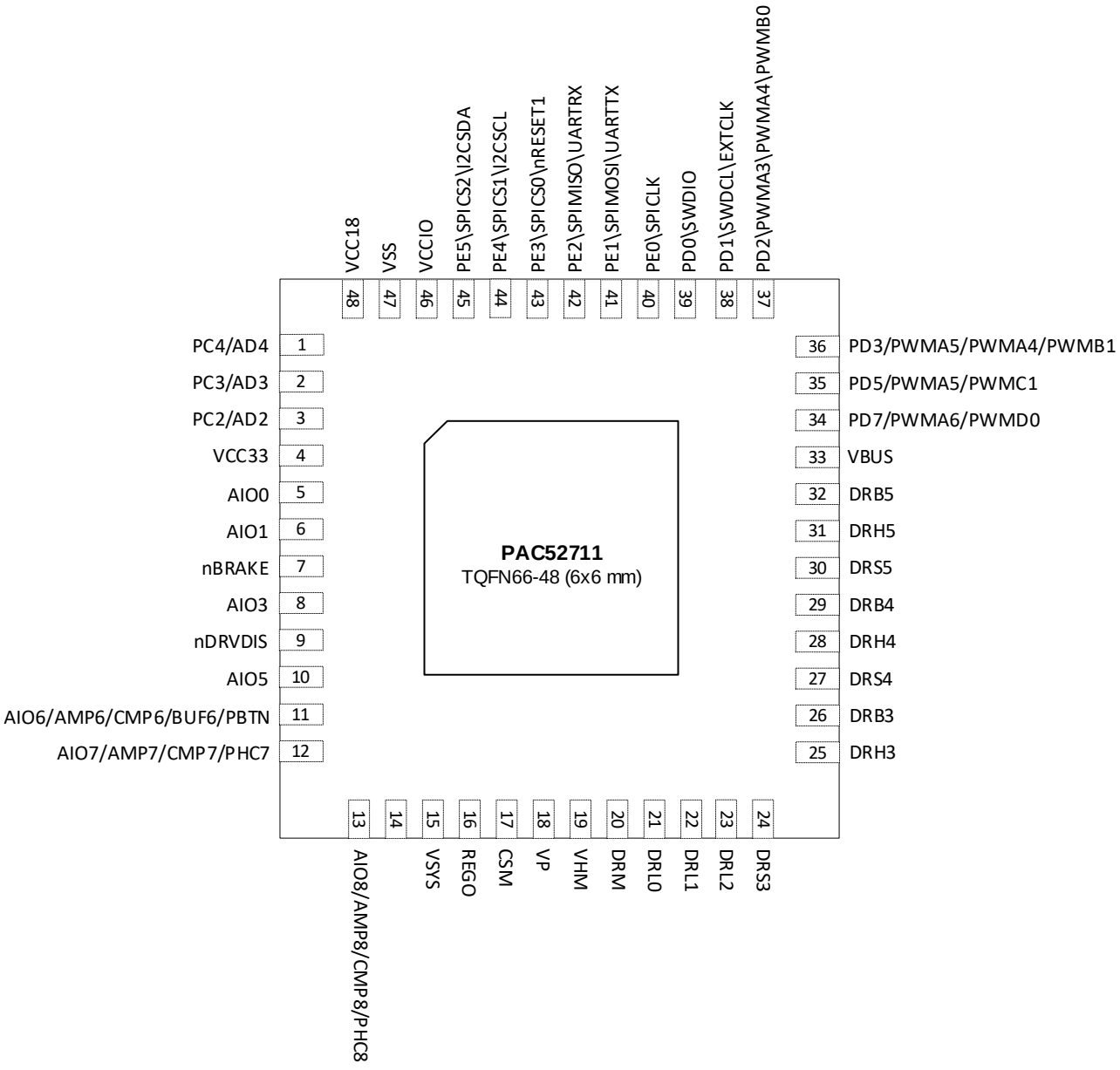
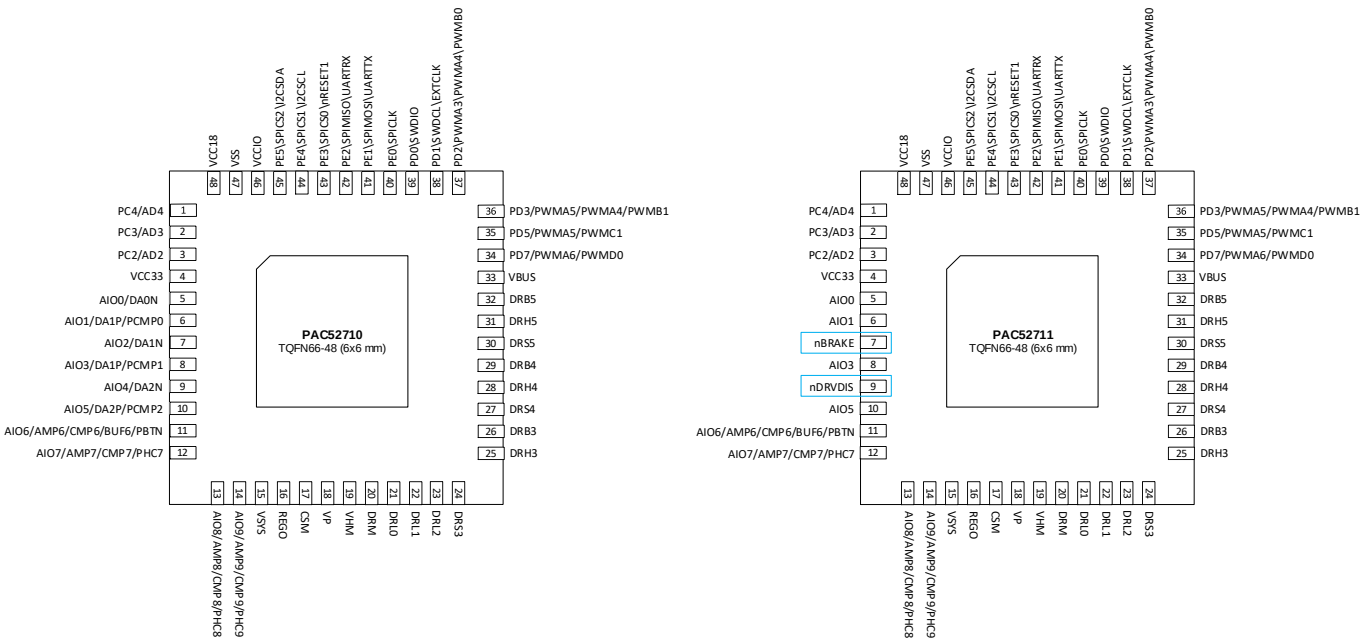


Figure 6-3 PAC52710QM and PAC52711QM Function Differences (pin comparison)



The differences between the PAC52710 and the PAC52711 devices are as detailed below:

1. Differential Amplifier 32 (AIO3 + AIO2) becomes analog input AIO3 and nBRAKE (formerly AIO2)
2. Differential Amplifier 54 (AIO5 + AIO4) becomes analog input AIO5 and nDRVDIS (formerly AIO4)

7 PIN DESCRIPTION

Table 7-1 Multi-Mode Power Manager and System Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
CSM	17	Analog	Switching supply current sense input. Connect to the positive side of the current sense resistor.
DRM	20	Analog	Switching supply driver output. Connect to the base or gate of the external power NPN or n-channel MOSFET. See PAC User Guide and application notes.
EP (VSS)	EP	Power	Exposed pad. Must be connected to V_{SS} in a star ground configuration. Connect to a large PCB copper area for power dissipation heat sinking.
VBUS	33	Power	High Side FET VDS Sensing connection. For RC filter from three phase inverter VBUS, connect a 1 Ohm series resistor with a 0.01µF value ceramic capacitor from V_{BUS} to V_{SSA}. See Figure 9-2. VBUS RC Filter Connections below.
VSS	47	Power	Ground.
REGO	16	Power	System regulator output. Connect to V_{SYS} directly or through an external power-dissipating resistor.
VCC18	48	Power	Internally generated 1.8V core power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CC18} to V_{SSA}. See Figure 9-1. Power Supply Bypass Capacitor Routing below.
VCC33	4	Power	Internally generated 3.3V power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CC33} to V_{SSA}. See PCB layout note below.
VCCIO	46	Power	Internally generated digital I/O power supply. Connect a 4.7µF or higher value ceramic capacitor from V_{CCIO} to V_{SSA}. See Figure 9-1. Power Supply Bypass Capacitor Routing below.
VHM	19	Power	Switching supply controller supply input. Connect a 1µF or higher value ceramic capacitor, or a 0.1µF ceramic capacitor in parallel with a 10µF or higher electrolytic capacitor from V_{HM} to V_{SSP}. This pin requires good capacitive bypassing to V_{SSP}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin. See Figure 9-1. Power Supply Bypass Capacitor Routing below.
VP	18	Power	Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 0.1µF ceramic capacitor from V_P pin to V_{SS} for voltage loop stabilization. This pin requires good capacitive bypassing to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin. See Figure 9-1. Power Supply Bypass Capacitor Routing below.
VSYS	15	Power	5V system power supply. Connect a 4.7µF or higher value ceramic capacitor from V_{SYS} to V_{SSP}. See Figure 9-1. Power Supply Bypass Capacitor Routing below.

Table 7-2 Configurable Analog Front End Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
AIO0/DA0N	5	AIO0	I/O	Analog front end I/O 0.
		DA0N	Analog	Differential PGA 0 negative input.
AIO1/DA0P/PCMP0	6	AIO1	I/O	Analog front end I/O 1.
		DA0P	Analog	Differential PGA 0 positive input.
		PCMP0	Analog	Protection comparator input 0.
PAC52710 (pins 7 through 10)				
AIO2/DA1N	7	AIO2	I/O	Analog front end I/O 2.
		DA1N	Analog	Differential PGA 1 negative input.
AIO3/DA1P/PCMP1	8	AIO3	I/O	Analog front end I/O 3.
		DA1P	Analog	Differential PGA 1 positive input.
		PCMP1	Analog	Protection comparator input 1.
AIO4/DA2N	9	AIO4	I/O	Analog front end I/O 4.
		DA2N	Analog	Differential PGA 2 negative input.
AIO5/DA2P/PCMP2	10	AIO5	I/O	Analog front end I/O 5.
		DA2P	Analog	Differential PGA 2 positive input.
		PCMP2	Analog	Protection comparator input 2.
PAC52711 (pins 7 through 10)				
nBrake	7	nBrake	Input	Provides braking support. Pull low to enter Braking Mode
AIO3	8	AIO3	I/O	Analog front end I/O 3.
nDRVDIS	9	nDRVDIS	Input	Disables the tri phase inverter power stage.
AIO5	10	AIO5	I/O	Analog front end I/O 5.
AIO6/AMP6/CMP6/BUF6/PBTN	11	AIO6	I/O	Analog front end I/O 6.
		AMP6	Analog	PGA input 6.
		CMP6	Analog	Comparator input 6.
		BUF6	Analog	Buffer output 6.
		PBTN	Analog	Push button input.
AIO7/AMP7/CMP7/PHC7	12	AIO7	I/O	Analog front end I/O 7.
		AMP7	Analog	PGA input 7.
		CMP7	Analog	Comparator input 7.
		PHC7	Analog	Phase comparator input 7.
AIO8/AMP8/CMP8/PHC8	13	AIO8	I/O	Analog front end I/O 8.
		AMP8	Analog	PGA input 8.
		CMP8	Analog	Comparator input 8.
		PHC8	Analog	Phase comparator input 8.
AIO9/AMP9/CMP9/PHC9	14	AIO9	I/O	Analog front end I/O 9.
		AMP9	Analog	PGA input 9.
		CMP9	Analog	Comparator input 9.
		PHC9	Analog	Phase comparator input 9.

Table 7-3 Application Specific Power Drivers Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DRB3	26	Analog	High-side gate driver bootstrap 3.
DRB4	29	Analog	High-side gate driver bootstrap 4.
DRB5	32	Analog	High-side gate driver bootstrap 5.
DRH3	25	Analog	High-side gate driver 3.
DRH4	28	Analog	High-side gate driver 4.
DRH5	31	Analog	High-side gate driver 5.
DRL0	21	Analog	Low-side gate driver 0.
DRL1	22	Analog	Low-side gate driver 1.
DRL2	23	Analog	Low-side gate driver 2.
DRS3	24	Analog	High-side gate driver source 3.
DRS4	27	Analog	High-side gate driver source 4.
DRS5	30	Analog	High-side gate driver source 5.

Table 7-4 I/O Ports Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
PC2/AD2	3	PC2	I/O	I/O port C2.
		AD2	Analog	ADC input 2.
PC3/AD3	2	PC3	I/O	I/O port C3.
		AD3	Analog	ADC input 3.
PC4/AD4	1	PC4	I/O	I/O port C4.
		AD4	Analog	ADC input 4.

Table 7-5 I/O Ports Pin Description (Continued)

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
PD0/SWDIO	39	PD0	I/O	I/O port D0.
		SWDIO	I/O	Serial wire debug I/O.
PD1/SWDCL/EXTCLK	38	PD1	I/O	I/O port D1.
		SWDCL	I	Serial wire debug clock.
		EXTCLK	I	External clock.
PD2/PWMA3/PWMA4/PWMB0	37	PD2	I/O	I/O port D2.
		PWMA3	I/O	Timer A PWM/capture 3.
		PWMA4	I/O	Timer A PWM/capture 4.
		PWMB0	I/O	Timer B PWM/capture 0.
PD3/PWMA5/PWMA7/PWMB1	36	PD3	I/O	I/O port D3.
		PWMA5	I/O	Timer A PWM/capture 5.
		PWMA7	I/O	Timer A PWM/capture 7.
		PWMB1	I/O	Timer B PWM/capture 1.
PD5/PWMA5/PWMC1	35	PD5	I/O	I/O port D5.
		PWMA5	I/O	Timer A PWM/capture 5.
		PWMC1	I/O	Timer C PWM/capture 1.
PD7/PWMA6/PWMD0	34	PD7	I/O	I/O port D7.
		PWMA6	I/O	Timer A PWM/capture 6.
		PWMD0	I/O	Timer D PWM/capture 0.
PE0/SPICLK	40	PE0	I/O	I/O port E0.
		SPICLK	I/O	SPI clock.
PE1/SPIMOSI/UARTTX	41	PE1	I/O	I/O port E1.
		SPIMOSI	I/O	SPI master out slave in (MOSI).
		UARTTX	O	UART transmit output.
PE2/SPIMISO/UARTRX	42	PE2	I/O	I/O port E2.
		SPIMISO	I/O	SPI master in slave out (MISO).
		UARTRX	I	UART receive input.

Table 7-6 I/O Ports Pin Description (Continued)

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
PE3/SPICS0/nRESET1	43	PE3	I/O	I/O port E3.
		SPICS0	O	SPI chip select 0.
		nRESET1	I	Reset input 1 (active low).
PE4/SPICS1/I2CSCL	44	PE4	I/O	I/O port E4.
		SPICS1	O	SPI chip select 1.
		I2CSCL	I/O	I2C clock.
PE5/SPICS2/I2CSDA	45	PE5	I/O	I/O port E5.
		SPICS2	O	SPI chip select 2.
		I2CSDA	I/O	I2C data.

Figure 7-1 Power Supply Bypass Capacitor Routing

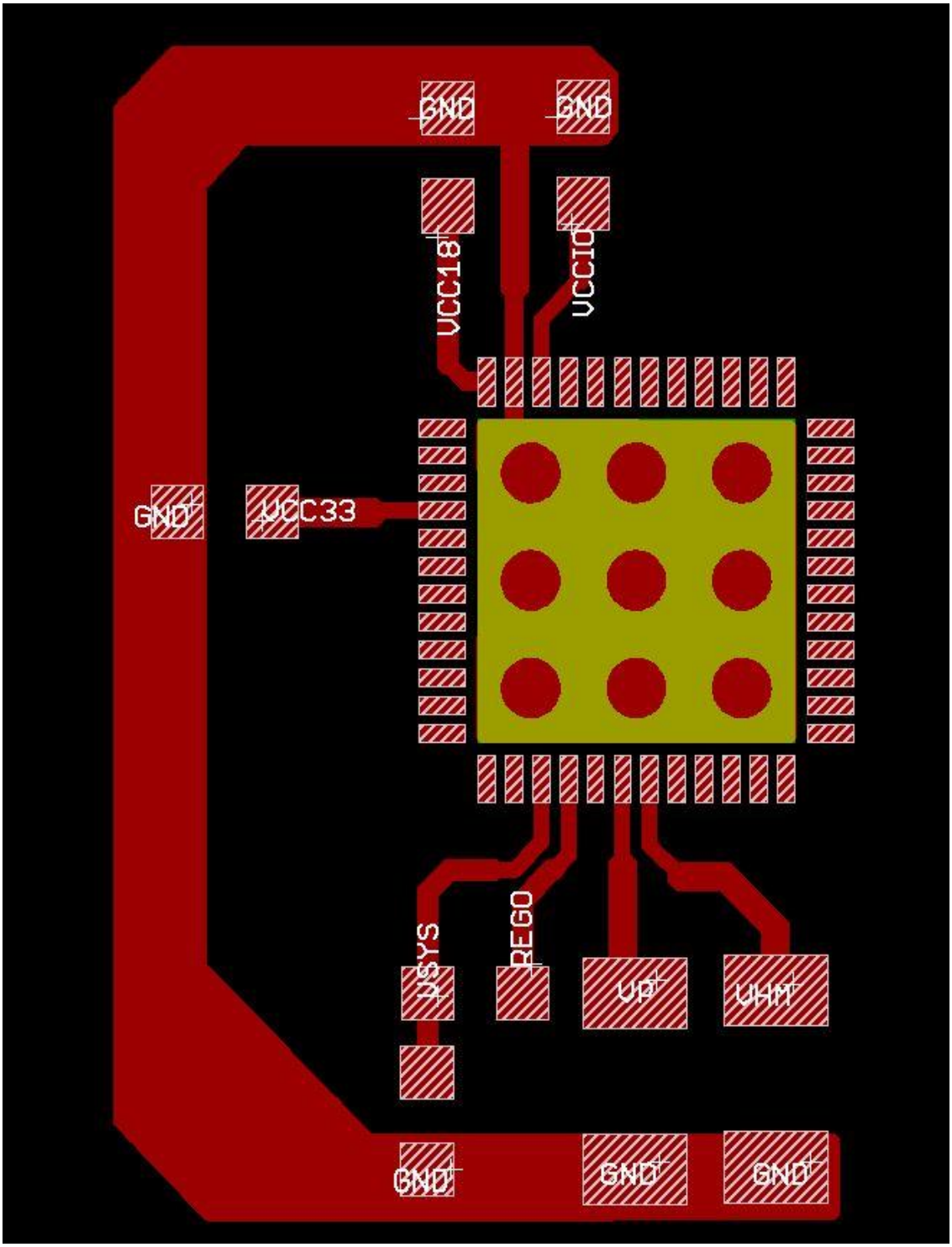
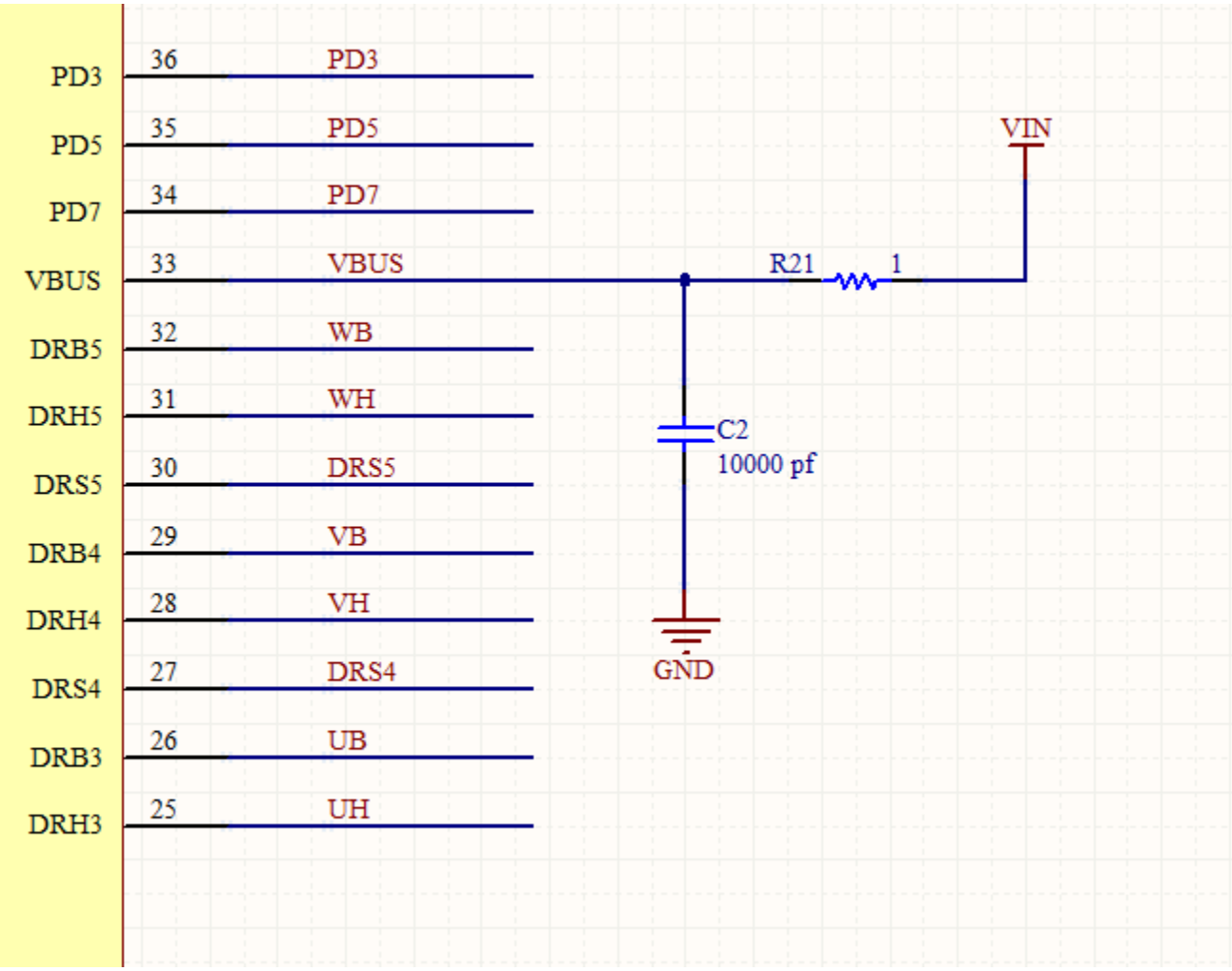


Figure 7-2 VBUS RC Filter Connections



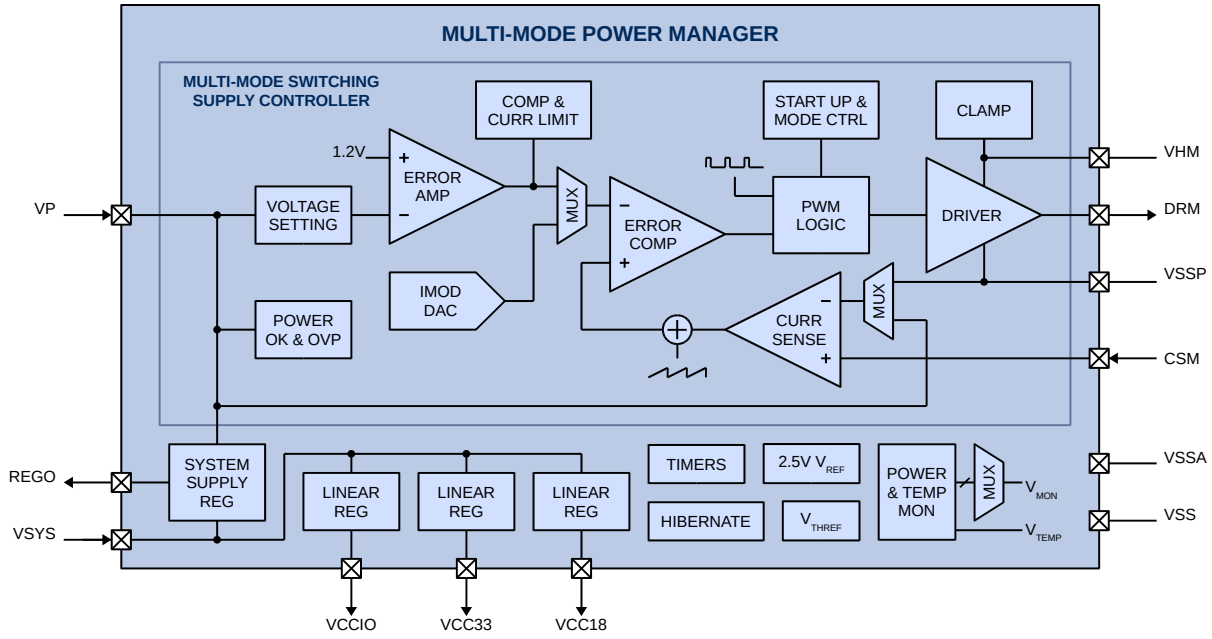
8 MULTI-MODE POWER MANAGER (MMPM)

8.1 Features

- Direct DC supply up to 20V (VP = VHM)
- Multi-mode switching supply controller configurable as Buck or SEPIC DC/DC controller up to 72V
- 4 linear regulators with power and hibernate management
- Power and temperature monitor, warning, and fault detection

8.2 Block Diagram

Figure 8-1 Multi-Mode Power Manager



8.3 Functional Description

The Multi-Mode Power Manager (Figure 10-1) is optimized to efficiently provide "all-in-one" power management required by the PAC and associated application circuitry from a wide range of input power sources. It incorporates a dedicated multi-mode switching supply (MMSS) controller operable as a buck or SEPIC DC/DC to efficiently convert power from a DC input source to generate a main supply output V_P. Four linear regulators provide V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CC18} supplies for 5V system, 5V or 3.3V I/O, 3.3V mixed signal, and 1.8V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

8.3.1 Multi-Mode Switching Supply (MMSS) Controller

The MMSS controller drives an external power transistor for pulse-width modulation switching of an inductor or transformer for power conversion. The DRM output drives the gate of the n-channel MOSFET or the base of the NPN between the V_{HM} on state and V_{SSP} off state at proper duty cycle and switching frequency to ensure that the main supply voltage V_P is regulated. The V_P regulation voltage is initially set to 15V during start up, and can be reconfigured to be 9V or 12V by the microcontroller after initialization. When V_P is lower than the target regulation voltage, the internal feedback control circuitry causes the inductor current to increase to raise V_P. Conversely, when V_P is higher than the regulation voltage, the feedback loop control causes the inductor current to decrease to lower V_P. The feedback loop is internally stabilized. The output current capability of the switching supply is determined by the external current sense resistor. In the high-side current sense buck or SEPIC mode, the inductor current signal is sensed differentially between the CSM pin and V_P, and has a peak current limit threshold of 0.26V. In the low-side current sense flyback mode, the inductor current signal is sensed differentially between the CSM pin and V_{SSP}, and has a peak current limit threshold of 1V.

The MMSS controller is flexible and configurable as a buck or SEPIC DC/DC converter. Input sources include battery supply for buck mode (Figure 10-2) or SEPIC mode (Figure 10-3), and Direct Mode (Figure 10-4). The MMSS controller operational mode is determined by external configuration and register settings from the microcontroller after power up. It can operate in either high-side or low-side current sense mode, and does not require external feedback loop compensation circuitry. For optional extended application range, the MMSS also incorporates additional digital control by the microcontroller to add accurate computations for outer feedback loop control such as power factor correction and accurate current control.

Figure 8-2 Buck Mode

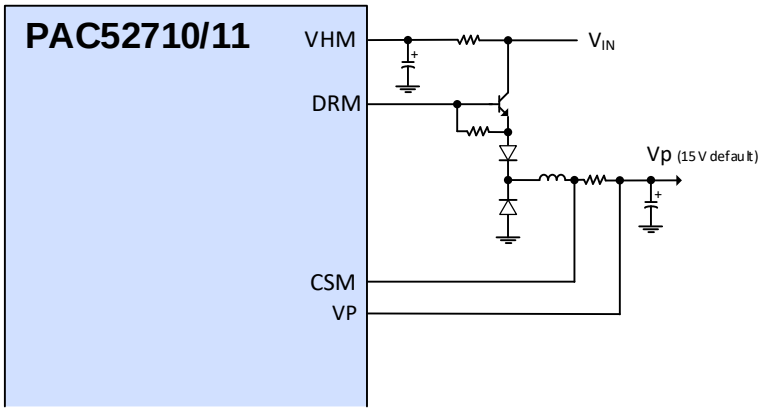


Figure 8-3 SEPIC Mode

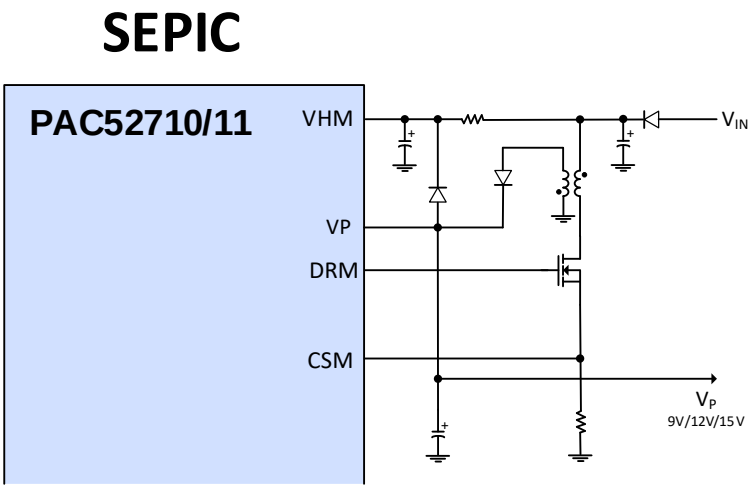
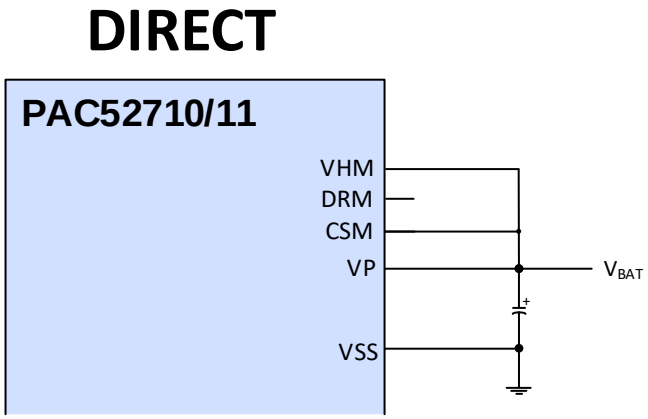


Figure 8-4 Direct Mode



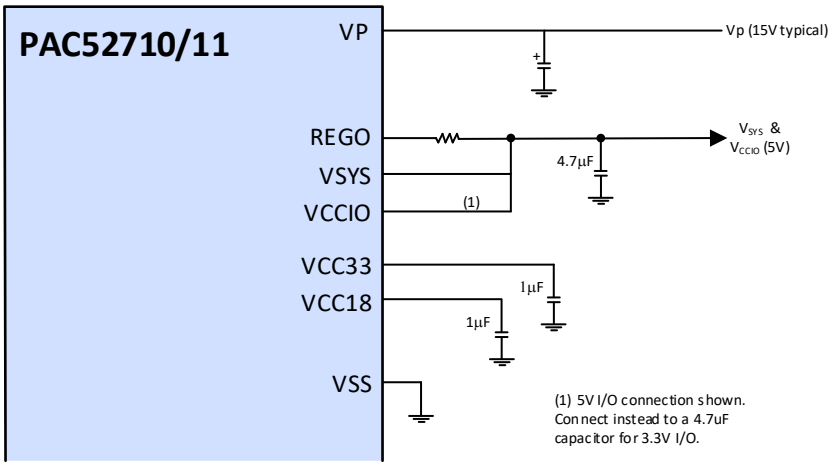
The MMSS detects and selects between high-side and low-side mode during start up based on the placement of the current sense resistor and the CSM pin voltage. It employs a safe start up mode with a 9.5kHz switching frequency until V_P exceeds 4.3V under-voltage-lockout threshold, then transitions to the 45kHz default switching frequency for at least 6ms to bring V_P close to the target voltage, before enabling the linear regulators. Any extra load should only be applied after the supplies are available and the microprocessor has initialized. The switching frequency can be reconfigured by the microprocessor to be 181kHz to 500kHz in the high switching frequency mode for battery-based applications, and to be 45kHz to 125kHz in the low switching frequency mode for AC applications. Upon initialization, the microcontroller must reconfigure the MMSS to the desired settings for V_P regulation voltage, switching mode, switching frequency, and V_{HM} clamp. Refer to the PAC application notes and user guide for MMSS controller design and programming.

If a stable external 5V to 18V power source is available, it can power the V_P main supply and all the linear regulators directly without requiring the MMSS controller to operate. In such applications, V_{HM} can be connected directly to V_P and the microcontroller should disable the MMSS upon initialization to reduce power loss.

8.3.2 Linear Regulators

The MMPM includes up to four linear regulators. The system supply regulator is a medium voltage regulator that takes the V_P supply and sources up to 200mA at REGO until V_{SYS}, externally coupled to REGO, reaches 5V. This allows a properly rated external resistor to be connected from REGO to V_{SYS} to close the current loop and offload power dissipation between V_P and V_{SYS}. Once V_{SYS} is above 4V, the three additional 40mA linear regulators for V_{CCIO}, $V_{CC3}3$, and V_{CC18} supplies sequentially power up. Figure 10-5 shows typical circuit connections for the linear regulators. For 5V I/O systems, short the V_{CCIO} pin to V_{SYS} to bypass the V_{CCIO} regulator. For 3.3V I/O systems, the V_{CCIO} regulator generates 3.3V. The V_{CC33} and V_{CC18} regulators generate 3.3V and 1.8V, respectively. When V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CC18} are all above their respective power good thresholds, and the configurable power on reset duration has expired, the microcontroller is initialized.

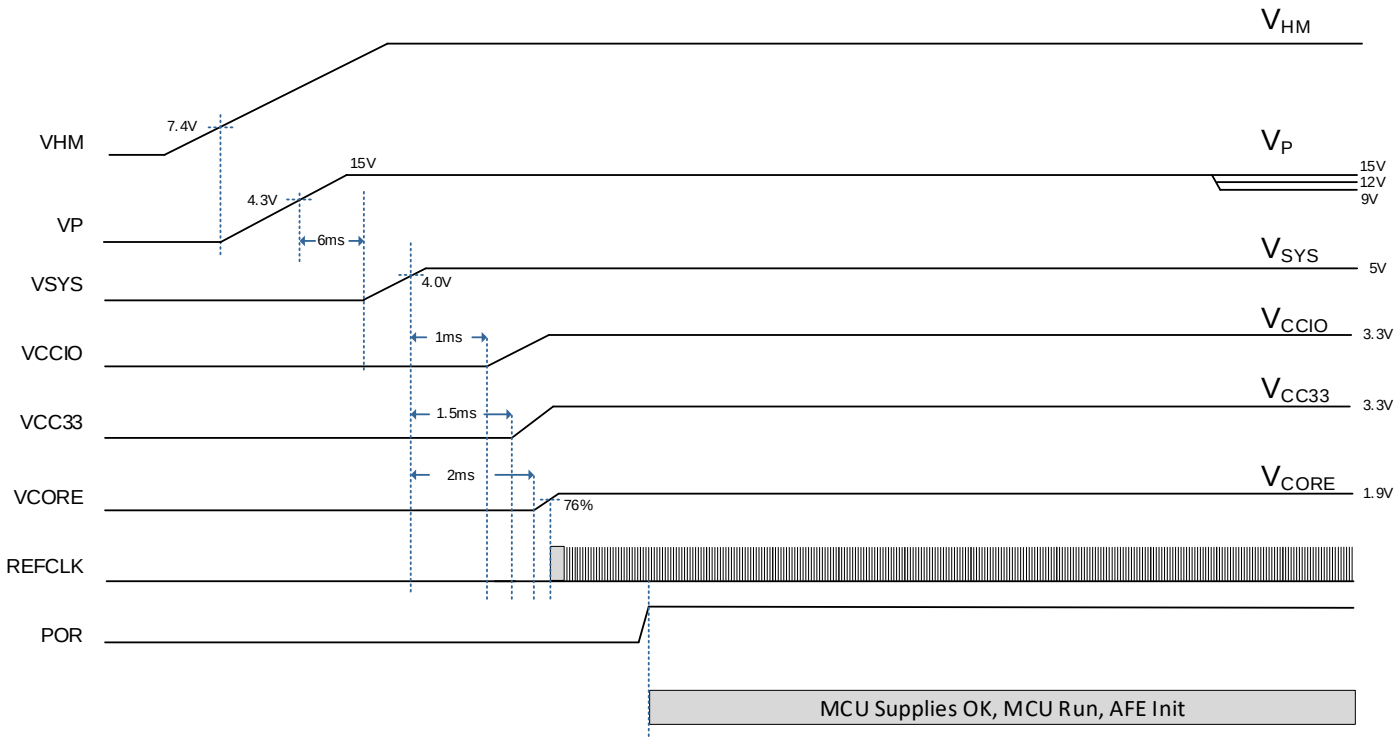
Figure 8-5 Linear Regulators



8.3.3 Power Up Sequence

The MMPM follows a typical power up sequence as in the Figure 10-6 below. A typical sequence begins with input power supply being applied, followed by the safe start up and start up durations to bring the switching supply output V_P to 15V, before the linear regulators are enabled. When all the supplies are ready, the internal clocks become available, and the microcontroller starts executing from the program memory. During initialization, the microcontroller can reconfigure the switching supply to a different V_P regulation voltage such as 15V and to an appropriate switching frequency and switching mode. The total loading on the switching supply must be kept below 25% of the maximum output current until after the reconfiguration of the switching supply is complete. For AC input supply applications, the start up sequence includes an additional charging time for V_{HM} depending on the start-up resistor and capacitor values.

Figure 8-6 Power Up Sequence



8.3.4 Hibernate Mode

On PAC52710, the IC can go into an ultra-low power hibernate mode via the microcontroller firmware or via the optional push button (PBTN, see Push Button description in Configurable Analog Front End). On PAC52711, the IC can go into hibernate only by following a specific hardware based sequence . In hibernate mode, only a minimal amount (typically 18µA) of current is used by V_{HM}, and the MMSS controller and all internal regulators are shut down to eliminate power drain from the output supplies. The system exits hibernate mode after a wake-up timer duration (configurable from 125ms to 8s or infinite) has expired or, if push button enabled, after an additional push button event has been detected. When exiting the hibernate mode, the power manager goes through the start up cycle and the microcontroller is reinitialized. Only the persistent power manager status bits (resets and faults) are retained during hibernation.

8.3.5 Power and Temperature Monitor

Whenever any of the V_{SYS}, V_{CCIO}, V_{CC33}, or V_{CC18} power supplies falls below their respective power good threshold voltage, a fault event is detected and the microcontroller is reset. The microcontroller stays in the reset state until V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CC18} supply rails are all good again and the reset time has expired. A microcontroller reset can also be initiated by a maskable temperature fault event that occurs when the IC temperature reaches 170°C. The fault status bits are persistent during reset, and can be read by the microcontroller upon re-initialization to determine the cause of previous reset.

A power monitoring signal V_{MON} is provided onto the ADC pre-multiplexer for monitoring various internal power supplies. V_{MON} can be set to be V_{CC18}, 0.4•V_{CC33}, 0.4•V_{CCIO}, 0.4•V_{SYS}, 0.1•V_{REGO}, 0.1•V_P, 0.0333•V_{HM}, or the internal compensation voltage V_{COMP} for switching supply power monitoring.

For power and temperature warning, a V_P low event at 77% of the regulation voltage and an IC temperature warning event at 140°C are provided as maskable interrupts to the microcontroller. These warnings allow the microcontroller to safely power down the system.

In addition to the temperature warning interrupt and fault reset, a temperature monitor signal V_{TEMP} = 1.5 + 5.04e-3 • (T - 25°C) (V) is provided onto the ADC pre-multiplexer for IC temperature measurement.

8.3.6 Voltage Reference

The reference block includes a 2.5V high precision reference voltage that provides the 2.5V reference voltage for the ADC, the DACs, and the 4-level programmable threshold voltage V_{THREF} (0.1V, 0.2V, 0.5V, and 1.25V).

8.4 Electrical Characteristics

Table 8-1 Multi-Mode Switching Supply Controller Electrical Characteristics

(V_{HM} = 24V, V_P = 12V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply (V_{HM})						
$I_{HIB;VHM}$	V_{HM} hibernate mode supply current	V_{HM}, hibernate mode		13	26	µA
$I_{SU;VHM}$	V_{HM} start up supply current	V_{HM} < $V_{UVLOR;VHM}$		75	120	µA
$I_{OP;VHM}$	V_{HM} operating supply current	DRM floating		0.3	0.5	mA
$V_{OP:VHM}$	V_{HM} operating voltage range		5.0		70	V
$V_{UVLOR;VHM}$	V_{HM} under-voltage lockout rising		7	7.5	8	V
$V_{UVLOF;VHM}$	V_{HM} under-voltage lockout falling		6	6.5	7	V
$V_{CLAMP;VHM}$	V_{HM} clamp voltage	Clamp enabled, sink current = 100µA	12.9	15.5	17.5	V
$I_{CLAMP;VHM}$	V_{HM} clamp sink current limit	Clamp enabled		4		mA
Output Supply and Feedback (V_P)						
$V_{REG;VP}$	V_P output regulation voltage	Programmable to 9V, 12V, or 15V Load = 0 to 500mA	-7	-1	5	%
$k_{POK;VP}$	V_P power OK threshold	V_P rising, hysteresis = 10%	82	87	92	%
$k_{OVP;VP}$	V_P over voltage protection threshold	V_P rising, hysteresis = 15% MMPM Controller enabled		136		%
Switching Control						
$f_{SWMACC;DRM}$	Switching frequency accuracy		-10		10	%
$f_{SWM;DRM}$	Switching frequency programmable range	High frequency mode, 8 settings	181		500	kHz
		Low frequency mode, 8 settings	45		125	
$f_{SSU;DRM}$	Safe start up switching frequency			11.4		kHz
$t_{ONMIN;DRM}$	Minimum on time			440		ns
$t_{OFFMIN;DRM}$	Minimum off time	Low duty-cycle & Low-frequency mode		25		%
		Low duty-cycle & High frequency mode		440		ns
		High duty-cycle mode		820		ns

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Current Sense (CSM Pin)						
$V_{DET;CSM}$	CSM mode detection threshold	Rising, hysteresis = 50mV	0.35	0.55	0.75	V
$V_{HSLIM;CSM}$	High-side current limit threshold	181kHz, duty = 25%, relative to V_P	0.17	0.26	0.35	V
$V_{LSLIM;CSM}$	Low-side current limit threshold	45kHz, duty = 25%	0.7	1	1.48	V
$t_{BLANK;CSM}$	Current sense blanking time			200		ns
$V_{PROT;CSM}$	Low-side abnormal current sense protection threshold	V_P < 4.3V		0.8		V
		V_P > 4.3V		1.9		
Gate Driver Output (DRM Pin)						
$V_{OH;DRM}$	High-level output voltage	I_{DRM} = -20mA	V_{HM}−1			V
$V_{OL;DRM}$	Low-level output voltage	I_{DRM} = 20mA			0.6	V
$I_{OH;DRM}$	High-level output source current	V_{DRM} = V_{HM} - 5V		-0.30		A
$I_{OL;DRM}$	Low-level output sink current	V_{DRM} = 5V		0.50		A
$t_{PD;DRM}$	Strong pull down pulse width	High-side current sense mode		240		ns

Table 8-2 Linear Regulators Electrical Characteristics

(V_P = 12V and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OP;VP}$	V_P operating voltage range			4.7		18	V
$V_{UVLO;VP}$	V_P under-voltage-lockout threshold	V_P rising, hysteresis = 0.2V		4	4.3	4.7	V
$I_{Q;VP}$	V_P quiescent supply current	Power manager only, including $I_{Q;VSYS}$			400	750	µA
$I_{Q;VSYS}$	V_{SYS} quiescent supply current	V_{CCIO}, V_{CC33}, and V_{CC18} regulators only			350	600	µA
V_{SYS}	V_{SYS} output voltage	Load = 10µA to 200mA		4.8	5	5.18	V
V_{CCIO}	V_{CCIO} output voltage	Load = 10mA	V_{CCIO} shorted to V_{SYS}		V_{SYS}		V
			V_{CCIO} from regulator	3.152	3.3	3.398	
V_{CC33}	V_{CC33} output voltage	Load = 10mA		3.185	3.3	3.415	V
V_{CC18}	V_{CC18} output voltage	Load = 10mA		1.834	1.9	1.979	V
$I_{LIM;VSYS}$	V_{SYS} regulator current limit			220	330		mA
$I_{LIM;VCCIO}$	V_{CCIO} regulator current limit			45	80		mA
$I_{LIM;VCC33}$	V_{CC33} regulator current limit			45	80		mA
$I_{LIM;VCC18}$	V_{CC18} regulator current limit			45	80		mA
k_{SCFB}	Short circuit current fold back				50		%
$V_{DO;VSYS}$	V_{SYS} dropout voltage	V_P =5V, I_{SYS}=100mA			350	680	mV
$V_{UVLO;VSYS}$	V_{SYS} under-voltage-lockout threshold	V_{SYS} rising, hysteresis = 0.2V		4.1	4.3	4.5	V
k_{POKIO}	V_{CCIO} Power OK threshold	V_{CCIO} rising, hysteresis = 10%		80	86	92	%
k_{POK33}	V_{CC33} Power OK threshold	V_{CC33} rising, hysteresis = 10%		80	86	92	%
k_{POK18}	V_{CC18} Power OK threshold	V_{CC18} rising, hysteresis = 10%		80	86	92	%

Table 8-3 Power System Electrical Characteristics

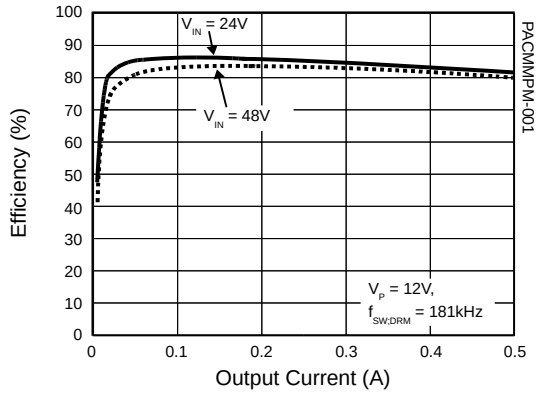
(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	T_A = 25°C	2.487	2.5	2.513	V
		T_A = -40°C to 105°C	2.463	2.5	2.537	
k_{MON}	Power monitoring voltage (V_{MON}) coefficient	V_{CC18}	0.92	1	1.02	V/V
		V_{SYS}, V_{CCIO}, V_{CC33}	0.36	0.4	0.43	
		V_P, V_{REGO}	0.09	0.1	0.11	
		V_{HM}	0.03	0.0333	0.038	
V_{TEMP}	Temperature monitor voltage at 25°C	T_A = 25°C, at ADC	1.475	1.5	1.540	V
k_{TEMP}	Temperature monitor coefficient	At ADC		6		mV/K
T_{WARN}	Over-temperature warning threshold	Hysteresis = 10°C		140		°C
T_{FAULT}	Over-temperature fault threshold	Hysteresis = 10°C		170		°C

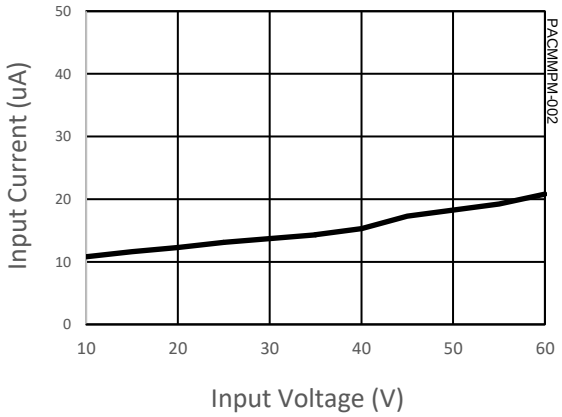
8.5 Typical Performance Characteristics

(V_P = 12V and T_A = 25°C unless otherwise specified.)

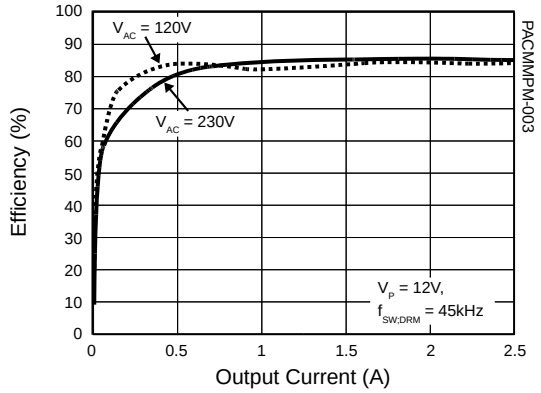
Buck Mode Efficiency vs. Output Current



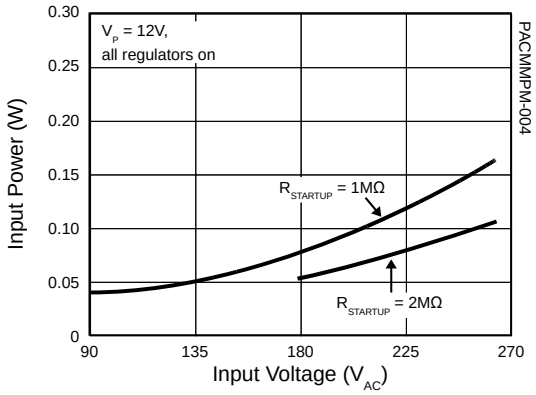
Buck Mode Hibernate Input Current vs. Input Voltage



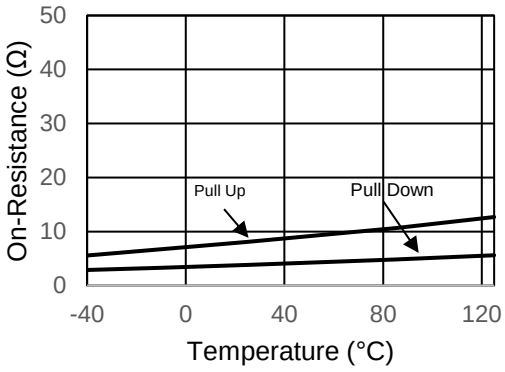
AC/DC Flyback Mode Efficiency vs. Output Current



AC/DC Flyback Mode Standby Power vs. Input Voltage



DRM Driver Output On Resistance vs. Temperature



9 CONFIGURABLE ANALOG FRONT END (CAFE)

9.1 Block Diagram

Figure 9-1 PAC52710 Configurable Analog Front End

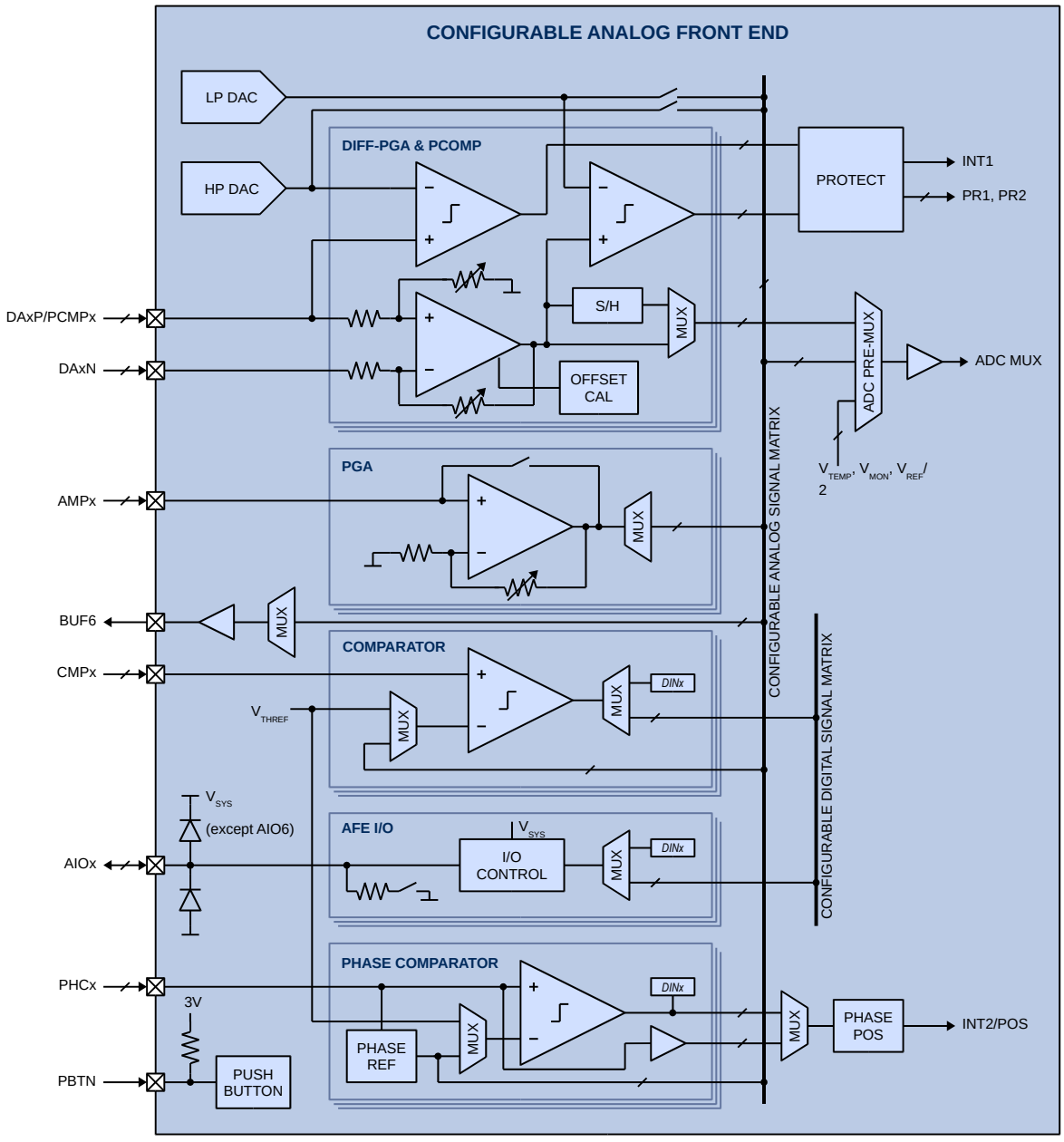
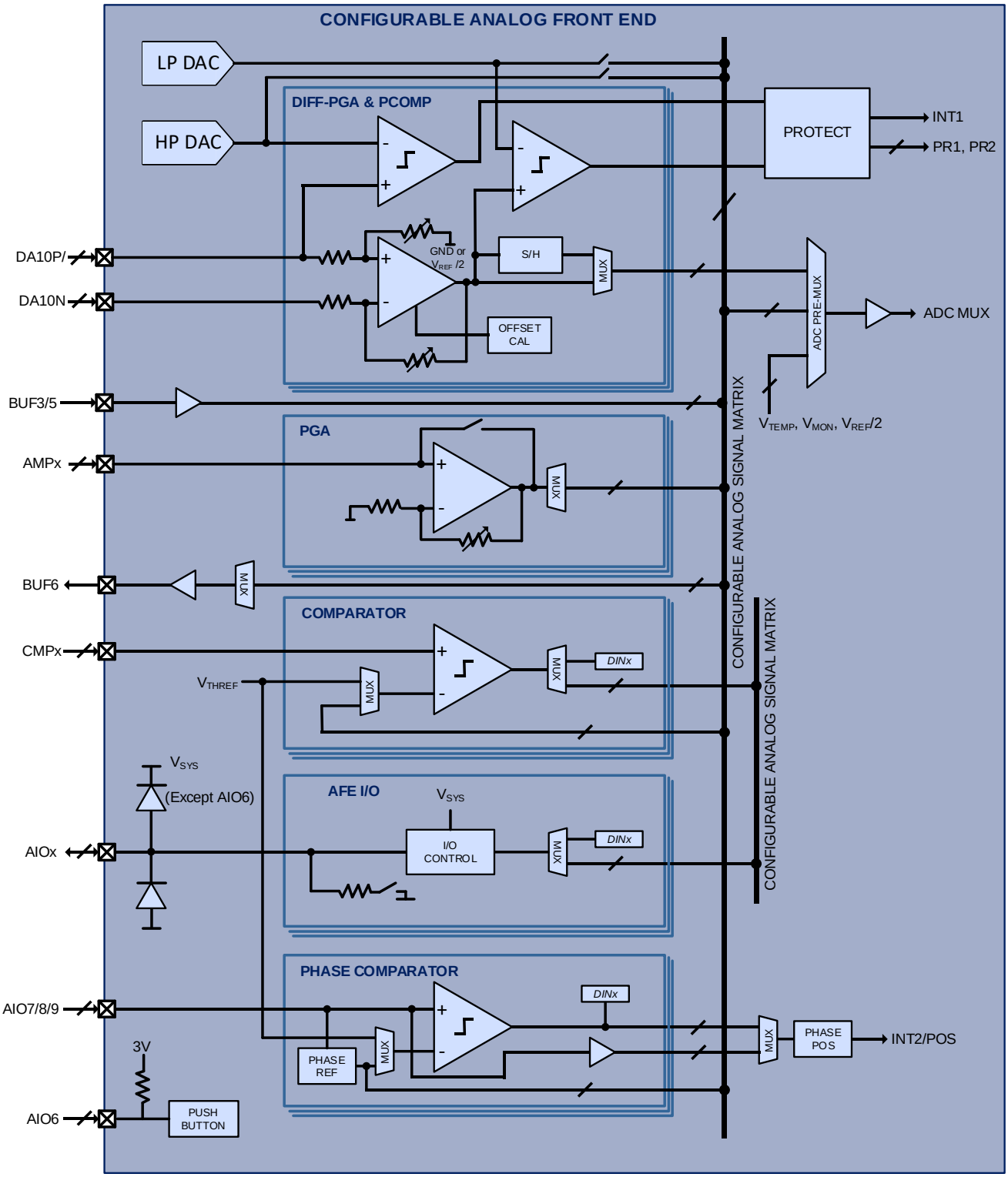


Figure 9-2 PAC52711 Configurable Analog Front End



9.2 Functional Description

The device includes a Configurable Analog Front End (CAFE, Figure 11-1 and Figure 11-2) accessible through up to 10 analog and I/O pins. These pins can be configured to form flexible interconnected circuitry made up of up to 3 differential programmable gain amplifiers, 4 single-ended programmable gain amplifiers, 4 general purpose comparators, 3 phase comparators, 10 protection comparators, and one buffer output. These pins can also be programmed as analog feed-through pins, or as analog front end I/O pins that can function as digital inputs or digital open-drain outputs. The PAC proprietary configurable analog signal matrix (CASM) and configurable digital signal matrix (CDSM) allow real time asynchronous analog and digital signals to be routed in flexible circuit connections for different applications. A push button function is provided for optional push button on, hibernate, and off power management function.

9.2.1 Differential Programmable Gain Amplifier (DA)

The DAxP and DAxN pin pair are positive and negative inputs, respectively, to a differential programmable gain amplifier. The differential gain can be programmable to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x for zero ohm signal source impedance. The differential programmable gain amplifier has -0.3V to 2.5V input common mode range, and its output can be configured for routing directly to the ADC pre-multiplexer, or through a sample-and-hold circuit synchronized with the ADC auto-sampling mechanism. Each differential amplifier is accompanied by offset calibration circuitry, and two protection comparators for protection event monitoring. The programmable gain differential amplifier is optimized for use with signal source impedance lower than 500Ω and with matched source impedance on both positive and negative inputs for minimal offset. The effective gain is scaled by 13.5k / (13.5k + R_{SOURCE}), where R_{SOURCE} is the matched source impedance of each input.

NOTE PAC52710 contains three differential amplifiers while PAC52711 contains one differential amplifier.

9.2.2 Single-Ended Programmable Gain Amplifier (AMP)

Each AMPx input goes to a single-ended programmable gain amplifier with signal relative to V_{SSA}. The amplifier gain can be programmed to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x, or as analog feed-through. The programmable gain amplifier output is routed via a multiplexer to the configurable analog signal matrix CASM.

9.2.3 Analog Output Buffer (BUF)

A subset of the signals from the configurable analog signal matrix CASM can be multiplexed to the BUF6 pin for external use. The buffer offset voltage can be minimized with the built-in swap function.

9.2.4 General Purpose Comparator (CMP)

The general purpose comparator takes the CMPx input and compares it to either the programmable threshold voltage (V_{THREF}) or a signal from the configurable analog signal matrix CASM. The comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed via a multiplexer to either a data input bit or the configurable digital signal matrix CDSM. Each general purpose comparator has two mask bits to prevent or allow rising or falling edge of its output to trigger second microcontroller interrupt INT2, where INT2 can be configured to active protection event PR1.

9.2.5 Phase Comparator (PHC)

The phase comparator takes the PHCx input and compares it to either the programmable threshold voltage (V_{THREF}) or a signal from the configurable analog signal matrix CASM. The comparison signal can be set to a phase reference signal generated by averaging the PHCx input voltages. In a three-phase motor control application, the phase reference signal acts as a virtual center tap for BEMF detection. The PHCx inputs are optionally fed through to the CASM. The phase comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed to a data input bit and to the phase/position multiplexer synchronized with the auto-sampling sequencers.

9.2.6 Protection Comparator (PCMP)

Two protection comparators are provided in association with each differential programmable gain amplifier, with outputs available to trigger protection events and accessible as read-back output bits. The high-speed protection (HP) comparator compares the PCMPx pin to the 8-bit HP DAC output voltage, with full scale voltage of 2.5V. The limit protection (LP) comparator compares the differential programmable gain amplifier output to the 10-bit LP DAC output voltage, with full scale voltage of 2.5V.

Each protection comparator has a mask bit to prevent or allow it to trigger the main microcontroller interrupt INT1. Each protection comparator also has one mask bit to prevent or allow it to activate protection event PR1, and another mask bit to prevent or allow it to activate protection event PR2. These two protection events can be used directly by protection circuitry in the Application Specific Power Drivers (ASPD) to protect devices being driven.

9.2.7 Analog Front End I/O (AIO)

Up to 10 AIOx pins are available in the device. In the analog front end I/O mode, the pin can be configured to be a digital input or digital open-drain output. The AIOx input or output signal can be set to a data input or output register bit, or multiplexed to one of the signals in the configurable digital signal matrix CDSM. The signal can be set to active high (default) or active low, with V_{SYS} supply rail. Where $AIO_{6,7,8,9}$ supports microcontroller interrupt for external signals. Each has two mask bits to prevent or allow rising or falling edge of its corresponding digital input to trigger second microcontroller interrupt INT2.

9.2.8 Push Button (PBTN)

The push button PBTN, when enabled, can be used by the microcontroller to detect a user active-low push button event and to put the system into an ultra-low-power hibernate mode. Once the system is in hibernate mode, PBTN can be used to wake up the system. In addition, PBTN can also be used as a hardware reset for the microcontroller when it is held low for longer than 8s during normal operation. The PBTN input is active low and has a 55kΩ pull-up resistor to 3V.

9.2.9 HP DAC and LP DAC

The 8-bit HP DAC can be used as the comparison voltage for the high-speed protection (HP) comparators, or routed for general purpose use via the AB2 signal in the CASM. The HP DAC output full scale voltage is 2.5V.

The 10-bit LP DAC can be used as the comparison voltage for the limit protection (LP) comparators, or routed for general purpose use via the AB3 signal in the CASM. The LP DAC output full scale voltage is 2.5V.

9.2.10 ADC Pre-Multiplexer

The ADC pre-multiplexer is a 16-to-1 multiplexer that selects between the 3 differential programmable gain amplifier outputs, AB1 through AB9, temperature monitor signal (V_{TEMP}), power monitor signal (V_{MON}), and offset calibration reference (V_{REF} / 2). The ADC pre-multiplexer can be directly controlled or automatically scanned by the auto-sampling sequencer.

When the ADC pre-multiplexer is automatically scanned, the unbuffered or sensitive signals should be masked by setting appropriate register bits.

9.2.11 Configurable Analog Signal Matrix (CASM)

The CASM has 9 general purpose analog signals labeled AB1 through AB9 that can be used for:

- Routing the single-ended programmable gain amplifier or analog feed-through output to AB1 through AB9
- Routing an analog signal via AB1, AB2, or AB3 to the negative input of a general purpose comparator or phase comparator
- Routing the 8-bit HP DAC output to AB2
- Routing the 10-bit LP DAC output to AB3
- Routing analog signals via AB1 through AB12 to the ADC pre-multiplexer
- Routing phase comparator feed-through signals to AB7, AB8, and AB9, and averaged voltage to AB1

9.2.12 Configurable Digital Signal Matrix (CDSM)

The CDSM has 7 general purpose bi-directional digital signals labeled DB1 through DB7 that can be used for:

- Routing the AIOx input to or output signals from DB1 through DB7
- Routing the general purpose comparator output signals to DB1 through DB7

9.2.13 Dual Single Ended Programmable Gain Amplifiers (BUF - PAC52711 only)

PAC52711 contains two single ended programmable gain amplifiers called BUF3 and BUF5. Each BUFx input goes to a programmable gain amplifier with signal relative to V_{SSA}. The buffer output is routed via a multiplexer to the configurable analog signal matrix CASM.

9.3 Electrical Characteristics

Table 9-1 Differential Programmable Gain Amplifier (DA) Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC;DA}$	Operating supply current	Each enabled amplifier		150	300	µA
$V_{ICMR;DA}$	Input common mode range		-0.3		2.5	V
$V_{OLR;DA}$	Output linear range		0.1		V_{SYS} – 0.1	V
$V_{SHR;DA}$	Sample and hold range		0.1		3.5	V
$V_{OS;DA}$	Input offset voltage	Gain = 48x, $V_{DAxP=}$ V_{DAxN} = 0V, T_A = 25°C	-8		8	mV
$A_{VZI;DA}$	Differential amplifier gain (zero ohm source impedance)	Gain = 1x		1		
		Gain = 2x		2		
		Gain = 4x		4		
		Gain = 8x, V_{DAxP} = 125mV, V_{DAxN} = 0V, T_A = 25°C	-2%	8	2%	
		Gain = 16x		16		
		Gain = 32x		32		
		Gain = 48x		48		
$k_{CMRR;DA}$	Common mode rejection ratio	Gain = 8x, $V_{DAxP=}$ V_{DAxN} = 0V, T_A = 25°C		55		dB
$R_{INDIF;DA}$	Differential input impedance			27		kΩ
	Slew rate (1)	Gain = 8x	7	10		V/µs
$t_{ST;DA}$	Settling time (1)	To 1% of final value		200	400	ns

(1) Guaranteed by design.

Table 9-2 Single-Ended Programmable Gain Amplifier (AMP) Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC;AMP}$	Operating supply current	Each enabled amplifier		80	140	µA
$V_{ICMR;AMP}$	Input common mode range		0		V_{SYS}	V
$V_{OLR;AMP}$	Output linear range		0.1		V_{SYS} – 0.1	V
$V_{OS;AMP}$	Input offset voltage	Gain = 1x, T_A = 25°C, V_{AMPX} = 2.5V	-10		10	mV
$A_{V;AMP}$	Amplifier gain	Gain = 1x		1		
		Gain = 2x		2		
		Gain = 4x		4		
		Gain = 8x, V_{AMPx} = 125mV, T_A = 25°C	-2%	8	2%	
		Gain = 16x		16		
		Gain = 32x		32		
		Gain = 48x		48		
$I_{IN;AMP}$	Input current			0	1	µA
	Slew rate (1)	Gain = 8x	8	12		V/µs
$t_{ST;AMP}$	Settling time (1)	To 1% of final value		150	300	ns

(1) Guaranteed by design.

Table 9-3 General Purpose Comparator (CMP) Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC;CMP}$	Operating supply current	Each enabled comparator		35	110	µA
$V_{ICMR;CMP}$	Input common mode range		0		V_{SYS}	V
$V_{OS;CMP}$	Input offset voltage	V_{CMPx} = 2.5V, T_A = 25°C	-10		10	mV
$V_{HYS;CMP}$	Hysteresis			23		mV
$I_{IN;CMP}$	Input current			0	1	µA
$t_{DEL;CMP}$	Comparator delay (1)				0.1	µs

(1) Guaranteed by design.

Table 9-4 Phase Comparator (PHC) Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC;PHC}$	Operating supply current	Each enabled comparator		35	110	µA
$V_{ICMR;PHC}$	Input common mode range		0		V_{SYS}	V
$V_{OS;PHC}$	Input offset voltage	V_{PHCx} = 2.5V, T_A = 25°C	-10		10	mV
$V_{HYS;PHC}$	Hysteresis			23		mV
$I_{IN;PHC}$	Input current			0	1	µA
$t_{DEL;PHC}$	Comparator delay (1)				0.1	µs

(1) Guaranteed by design.

Table 9-5 Protection Comparator (PCMP) Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC;PCMP}$	Operating supply current	Each enabled comparator		35	100	µA
$V_{ICMR;PCMP}$	Input common mode range		0.3		V_{SYS} -1	V
$V_{OS;PCMP}$	Input offset voltage	V_{PCMPx} = 2.5V, T_A = 25°C	-10		10	mV
$V_{HYS;PCMP}$	Hysteresis			20		mV
$I_{IN;PCMP}$	Input current			0	1	µA
$t_{DEL;PCMP}$	Comparator delay (1)				0.1	µs

(1) Guaranteed by design.

Table 9-6 Analog Output Buffer (BUF) Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC;BUF}$	Operating supply current	No load		35	100	µA
$V_{ICMR;BUF}$	Input common mode range		0.05		3.5	V
$V_{OLR;AMP}$	Output linear range		0.1		3.5	V
$V_{OS;BUF}$	Offset voltage	V_{BUF} = 2.5V, T_A = 25°C	-18		18	mV
I_{OMAX}	Maximum output current	C_L = 0.1nF	0.8	1.3		mA

Table 9-7 Analog Front End I/O (AIO) Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{AIO}	Pin voltage range		0		5	V
$V_{IH;AIO}$	High-level input voltage		2.2			V
$V_{IL;AIO}$	Low-level input voltage				0.8	V
$R_{PD;AIO}$	Pull-down resistance	Input mode	0.5	1	1.8	MΩ
$V_{OL;AIO}$	Low-level output voltage	I_{AIOx} = 7mA, open-drain output mode			0.4	V
$I_{OL;AIO}$	Low-level output sink current	V_{AIOx} = 0.4V, open-drain output mode	6	14		mA
$I_{LK;AIO}$	High-level output leakage current	V_{AIOx} = 5V, open-drain output mode		0	10	µA

Table 9-8 Push Button (PBTN) Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I;PBTN}$	Input voltage range		0		5	V
$V_{IH;PBTN}$	High-level input voltage		2			V
$V_{IL;PBTN}$	Low-level input voltage				0.35	V
$R_{PU;PBTN}$	Pull-up resistance	To 3V, push-button input mode	30	50	70	kΩ

Table 9-9 HP DAC and LP DAC Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DACREF}	DAC reference voltage	T_A = 25°C	2.480	2.5	2.520	V
		T_A = -40°C to 105°C	2.453	2.5	2.547	
	HP 8-bit DAC INL(1)		-1		1	LSB
	HP 8-bit DAC DNL(1)		-0.5		0.5	LSB
	LP 10-bit DAC INL(1)		-2		2	LSB
	LP 10-bit DAC DNL(1)		-1		1	LSB

(1) Guaranteed by design and characterization.

Table 9-10 Single Ended Programmable Gain Amplifier (BUF) Electrical Characteristics (PAC52711 only)

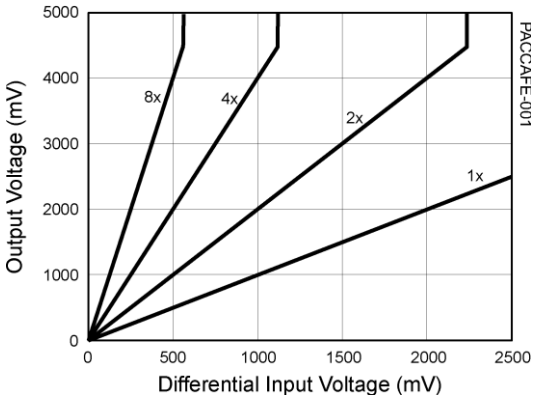
(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC;BUF}$	Operating supply current	No load		150	300	µA
$V_{ICMR;BUF}$	Input common mode range		0		2.5	V
$V_{OLR;AMP}$	Output linear range		0.1		VSYS-0.1	V
$V_{OS;BUF}$	Offset voltage	V_{BUF} = 2.5V, T_A = 25°C	-10		10	mV
$I_{IN;AMP}$	Input current			0	1	µA
$t_{ST;AMP}$	Settling time (1)	To 1% of final value		150	300	ns

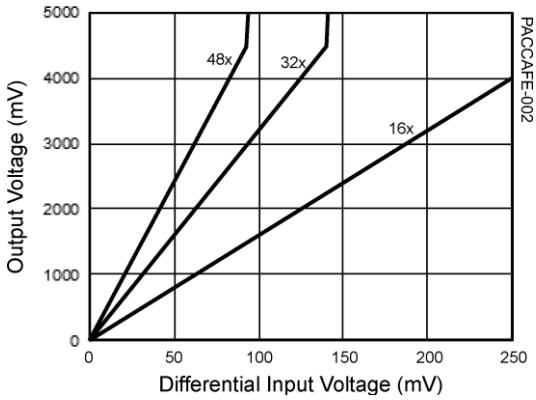
9.4 Typical Performance Characteristics

(V_{SYS} = 5V and T_A = 25°C unless otherwise specified.)

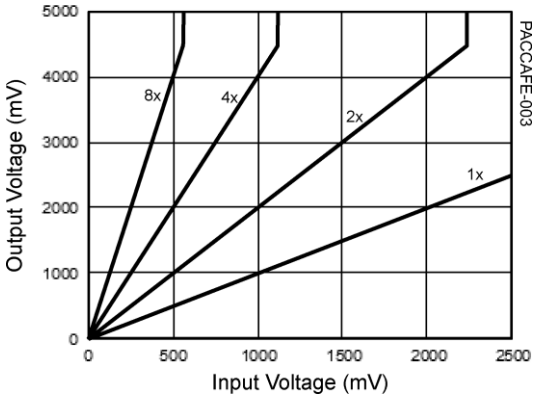
Differential PGA (DAx) Gain Characteristics at 1x, 2x, 4x, and 8x Settings



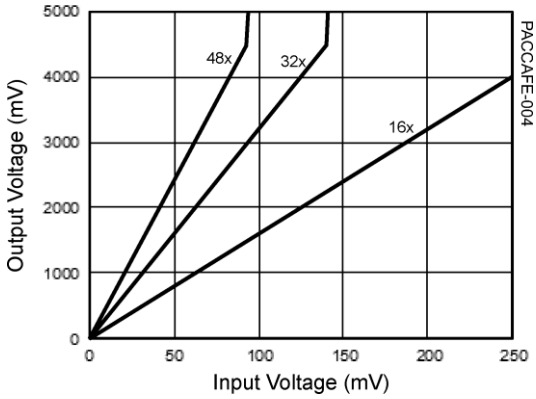
Differential PGA (DAx) Gain Characteristics at 16x, 32x, and 48x Settings



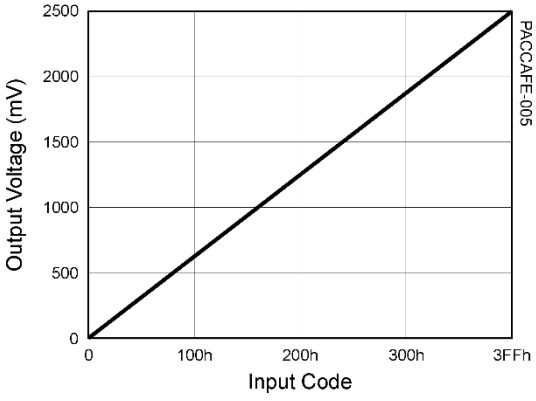
PGA (AMPx) Gain Characteristics at 1x, 2x, 4x, and 8x Settings



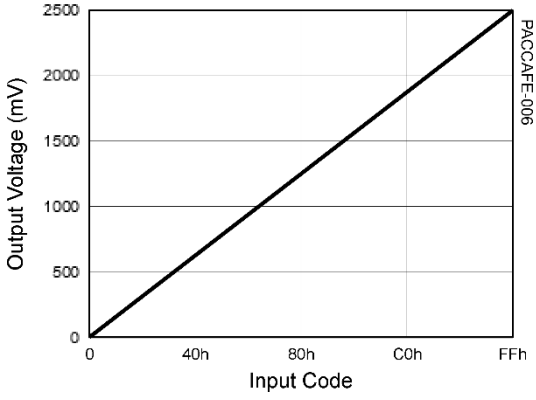
PGA (AMPx) Gain Characteristics at 16x, 32x, and 48x Settings

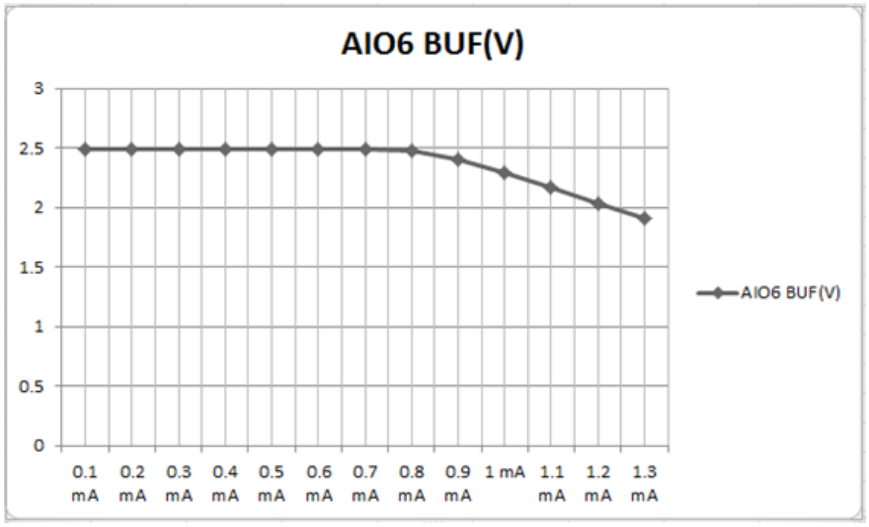


LP DAC Output Voltage vs. Input Code



HP DAC Output Voltage vs. Input Code




AIO6 BUF(V)
3
2.5
2
1.5
1
0.5
0
0.1 mA
0.2 mA
0.3 mA
0.4 mA
0.5 mA
0.6 mA
0.7 mA
0.8 mA
0.9 mA
1 mA
1.1 mA
1.2 mA
1.3 mA
AIO6 BUF(V)

10 APPLICATION SPECIFIC POWER DRIVERS (ASPD)

10.1 Features

- 3 low-side and 3 high-side gate drivers
- 1A gate driving capability
- Configurable delays and fast fault protection
- VDS Sensing for Over Current and Cycle By Cycle protection

10.2 Block Diagram

Figure 10-1 PAC52710 Application Specific Power Drivers

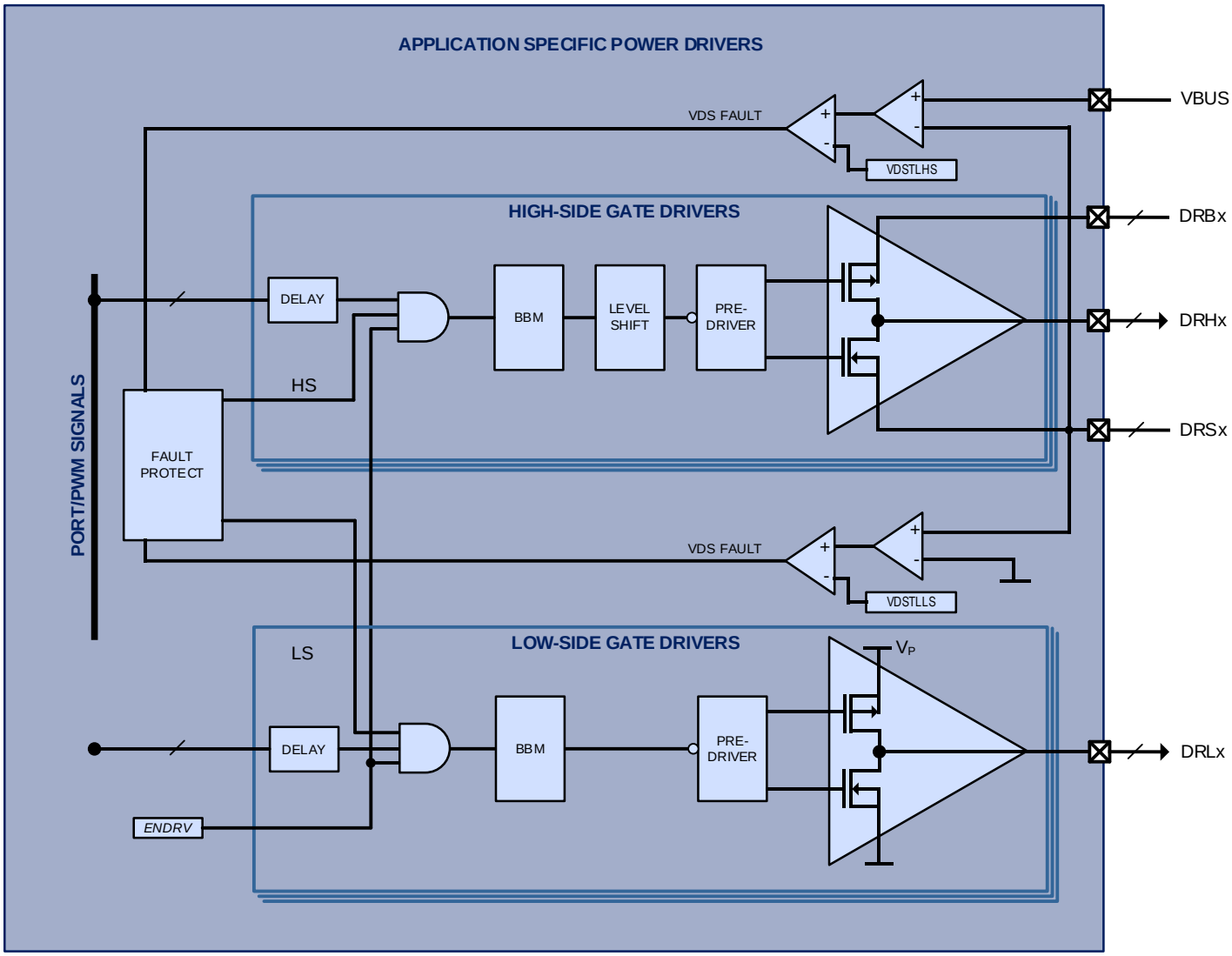
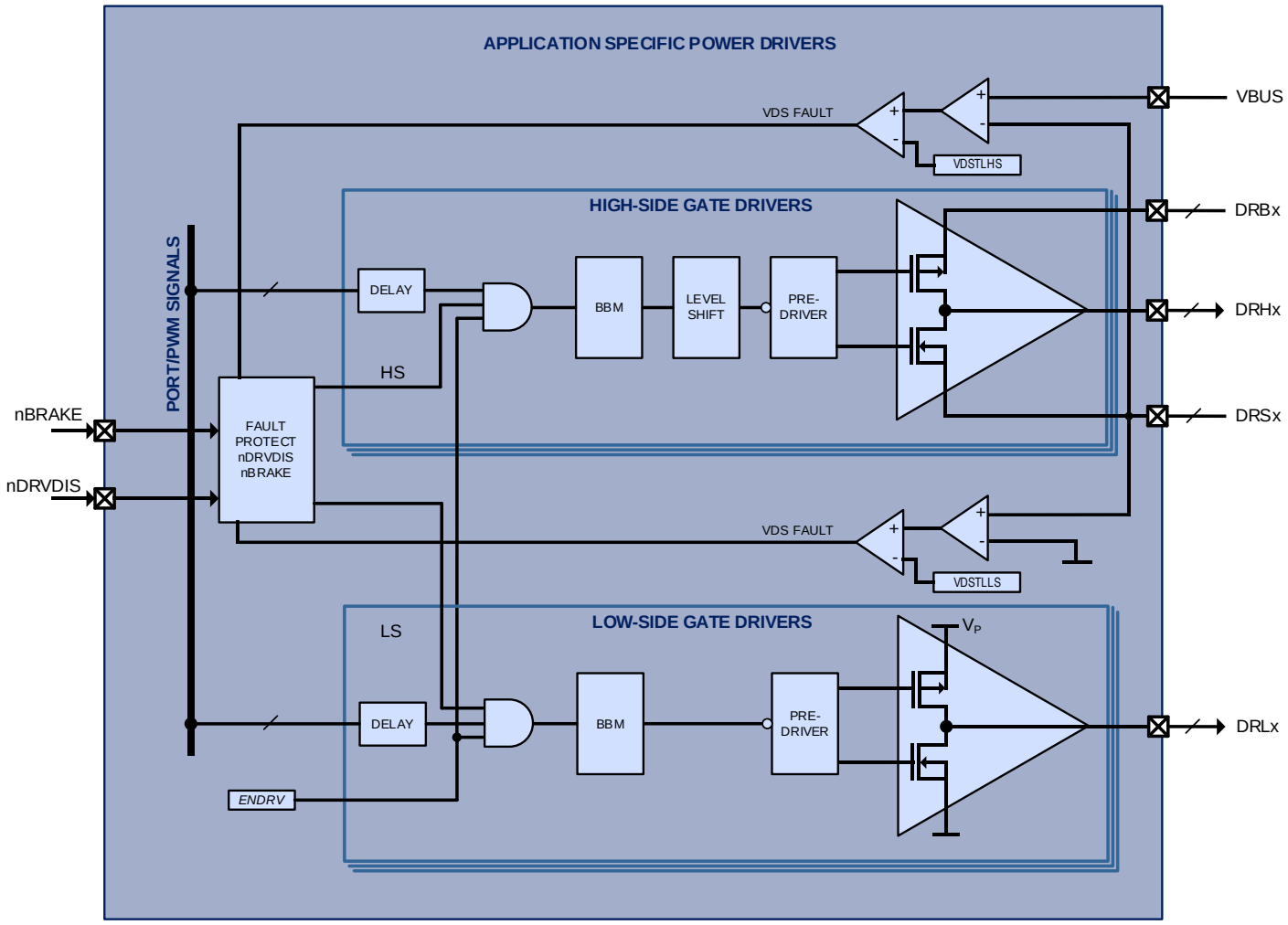


Figure 10-2 PAC52711 Application Specific Power Drivers



10.3 Functional Description

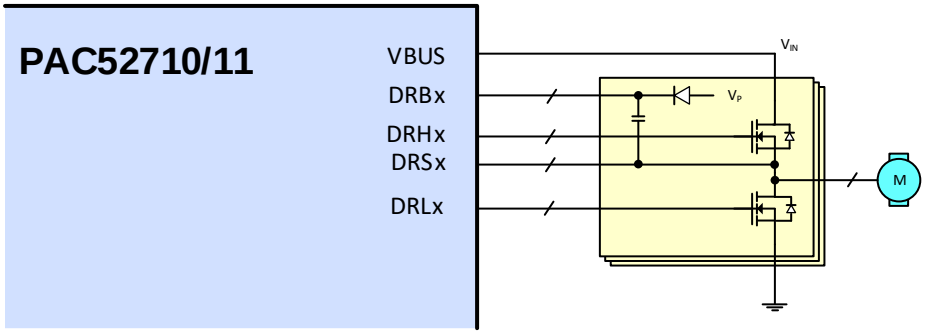
The Application Specific Power Drivers (ASPD, Figure 12-1) module handles power driving for power control applications. The PAC52710/11 has three low-side gate drivers (DRLx), three high-side gate drivers (DRHx). Each gate driver can drive an external MOSFET or IGBT switch in response to high-speed control signals from the microcontroller ports, and a pair of high-side and low-side gate drivers can form a half-bridge driver.

Figure 12-2 below shows typical gate driver connections and Table 12-1 shows the ASPD available resources. The PAC52710/11 gate drivers support up to a 70V supply.

Table 10-1 Power Driver Resources by Part Numbers

PART NUMBER	LOW-SIDE GATE DRIVER		HIGH-SIDE GATE DRIVER		
	DRLx	SOURCE /SINK CURRENT	DRHx	MAX SUPPLY	SOURCE/ SINK CURRENT
PAC52710/11	3	1A/1A	3	70V	1A/1A

Figure 10-3 Typical Gate Driver Connections



The ASPD includes built-in configurable fault protection for the internal gate drivers.

10.3.1 Low-Side Gate Driver

The DRLx low-side gate driver drives the gate of an external MOSFET or IGBT switch between the low-level V_{SSP} power ground rail and high-level V_P supply rail. The DRLx output pin has sink and source output current capability of 1A. Each low-side gate driver is controlled by a microcontroller port signal with 4 configurable levels of propagation delay.

10.3.2 High-Side Gate Driver

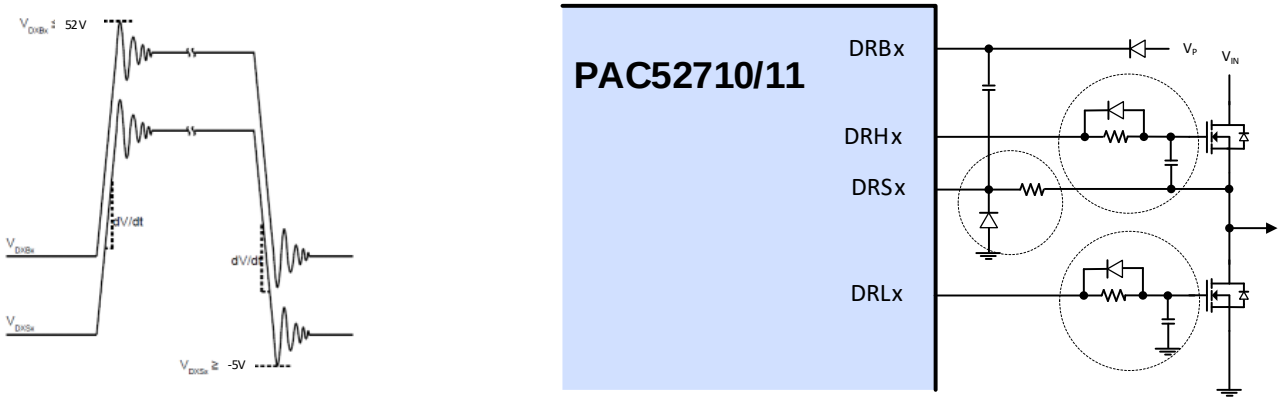
The DRHx high-side gate driver drives the gate of an external MOSFET or IGBT switch between its low-level DRSx driver source rail and its high-level DRBx bootstrap rail. The DRSx pin can go up to 70V steady state. The DRHx output pin has sink and source output current capability of 1A. The DRBx bootstrap pin can have a maximum operating voltage of 16V relative to the DRSx pin, and up to 82V steady state. The DRSx pin is designed to tolerate momentary switching negative spikes down to -5V without affecting the DRHx output state. Each high-side gate driver is controlled by a microcontroller port signal with 4 configurable levels of propagation delay.

For bootstrapped high-side operation, connect an appropriate capacitor between DRBx and DRSx and a properly rated bootstrap diode from V_P to DRBx. To operate the DRHx output as a low-side gate driver, connect its DRBx pin to V_P and its DRSx pin to V_{SSP}.

10.3.3 High-Side Switching Transients

Typical high-side switching transients are shown in Figure 12-3(a). To ensure functionality and reliability, the DRSx and DRBx pins must not exceed the peak and undershoot limit values shown. This should be verified by probing the DRBx and DRSx pins directly relative to VSS pin. A small resistor and diode clamp for the DRSx pin can be used to make sure that the pin voltage stays within the negative limit value. In addition, the high-side slew rate dV/dt must be kept within ±5V/ns for DRSx. This can be achieved by adding a resistor-diode pair in series, and an optional capacitor in parallel with the power switch gate. The parallel capacitor also provides a low impedance and close gate shunt against coupling from the switch drain. These optional protection and slew rate control are shown in Figure 12-3(b).

Figure 10-4 High-Side Switching Transients and Optional Circuitry



(a) High-Side Switching Transients

(b) Optional Transient Protection and Slew Rate Control

10.3.4 Power Drivers Control

On PAC52710, all power drivers are initially disabled from power-on-reset. To enable the power drivers, the microprocessor must first set the driver enable bit to '1'. On PAC52711, the power drivers are controlled by the nDRVDIS signal. To enable the power drivers, the external microprocessor must pull the nDRVDIS signal to a logic high, while the nDRVDIS signal is pulled up to logic high. There is no FW control for power driver enable/disable on PAC52711.

The gate drivers are controlled by the microcontroller ports and/or PWM signals according to Table 12-2, with configurable delays as shown in Table 12-3. Refer to the PAC application notes and user guide for additional information on power drivers control programming.

Table 10-2 Microcontroller Port and PWM to Power Driver Mapping

PART NUMBER	PWMA0	PWMA1	PWMA2	PWMA3/PWMA4/ PWMB0	PWMA5/PWMC0	PWMA6/PWMD0
PAC52710/11	DRL0	DRL1	DRL2	DRH3	DRH4	DRH5

Table 10-3 Power Driver Propagation Delay

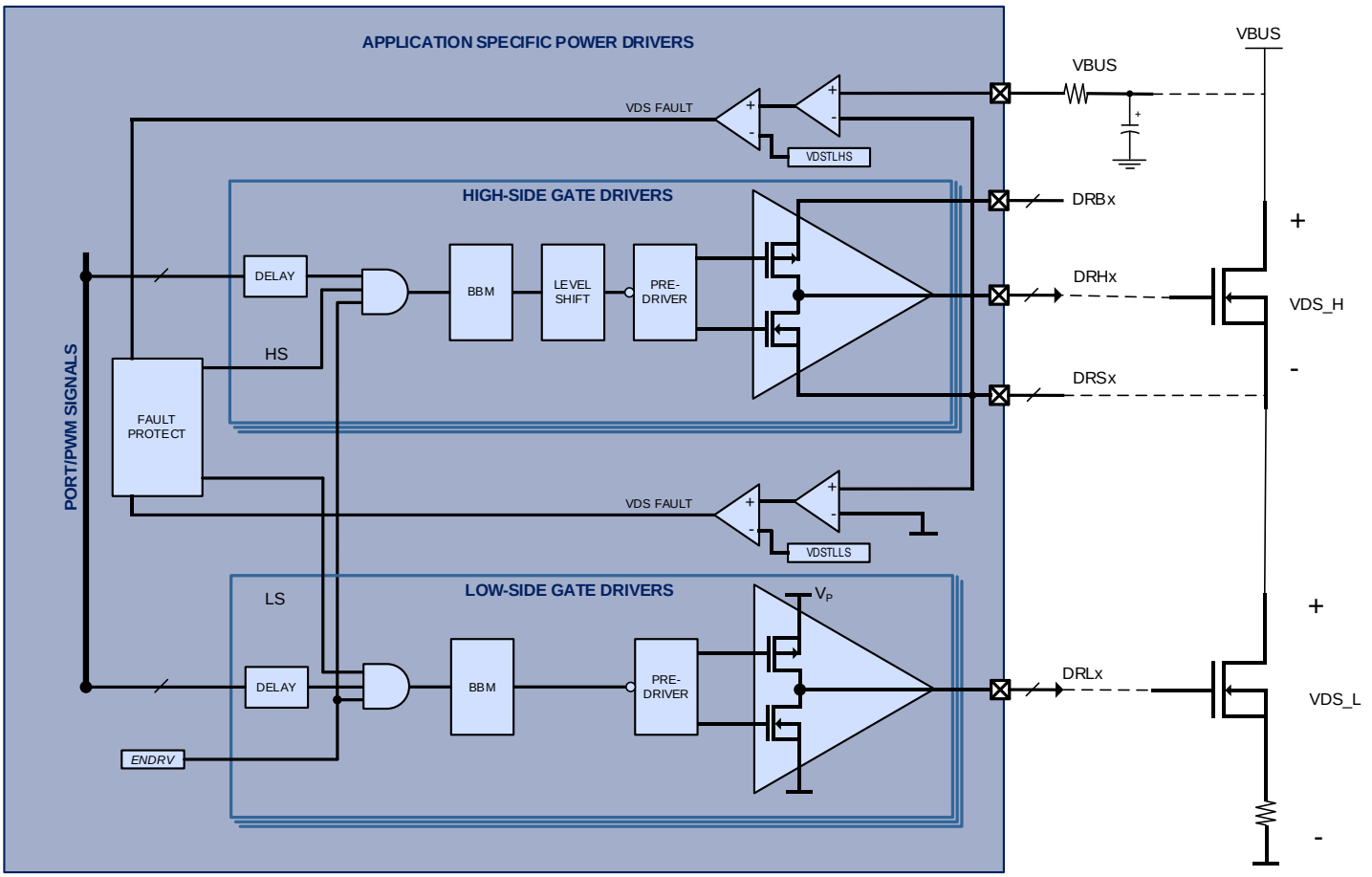
DRLx		DRHx	
RISING	FALLING	RISING	FALLING
130ns	140ns	160ns	140ns

10.3.5 Gate Driver Fault Protection

The ASPD incorporates a series of configurable fault protection mechanisms using protection signal from the Configurable Analog Front End (CAFE), designated as protection event 1 (PR1) signal. The DRL0/DRL1/DRL2 drivers are designated as low-side group 1. The DRH3/DRH4/DRH5 gate drivers are designated as high-side group 1. The PR1 signal from the CAFE can be used to disable low-side group 1, high-side group 1, or both depending on the PR1 mask bit settings.

10.3.6 VDS Sensing Protection

The ASPD adds a parallel protection mode which operates by sampling the external power switch's Drain To Source Resistance (RDSON). The VDS sensing block continuously monitors the FET's or IGBT's drain to source voltage, and compares it against one of the eight selectable internal reference voltages, or trip levels. When the external switch's voltage exceed the trip level voltage, a VDS Sensing event is issued. VDS Sense triggers can be used to generate interrupts or disable the tri phase inverter throughout a cycle by cycle mechanism.

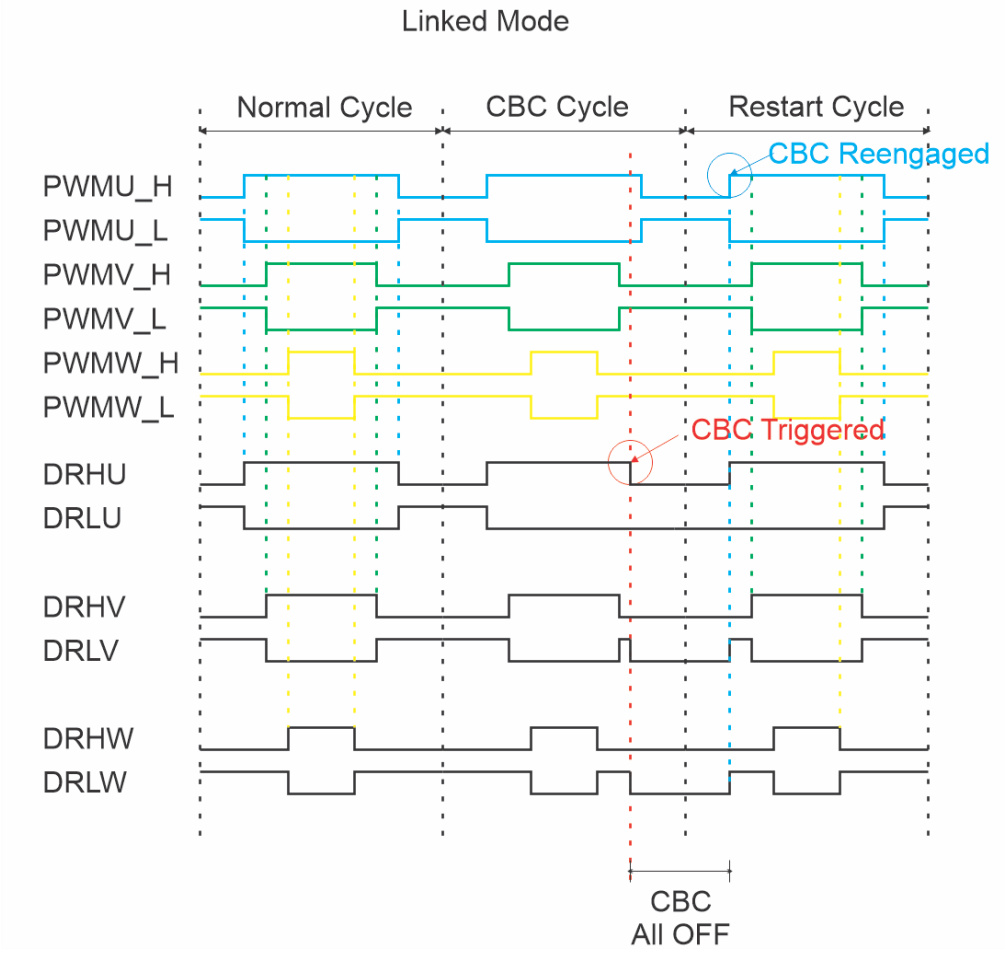


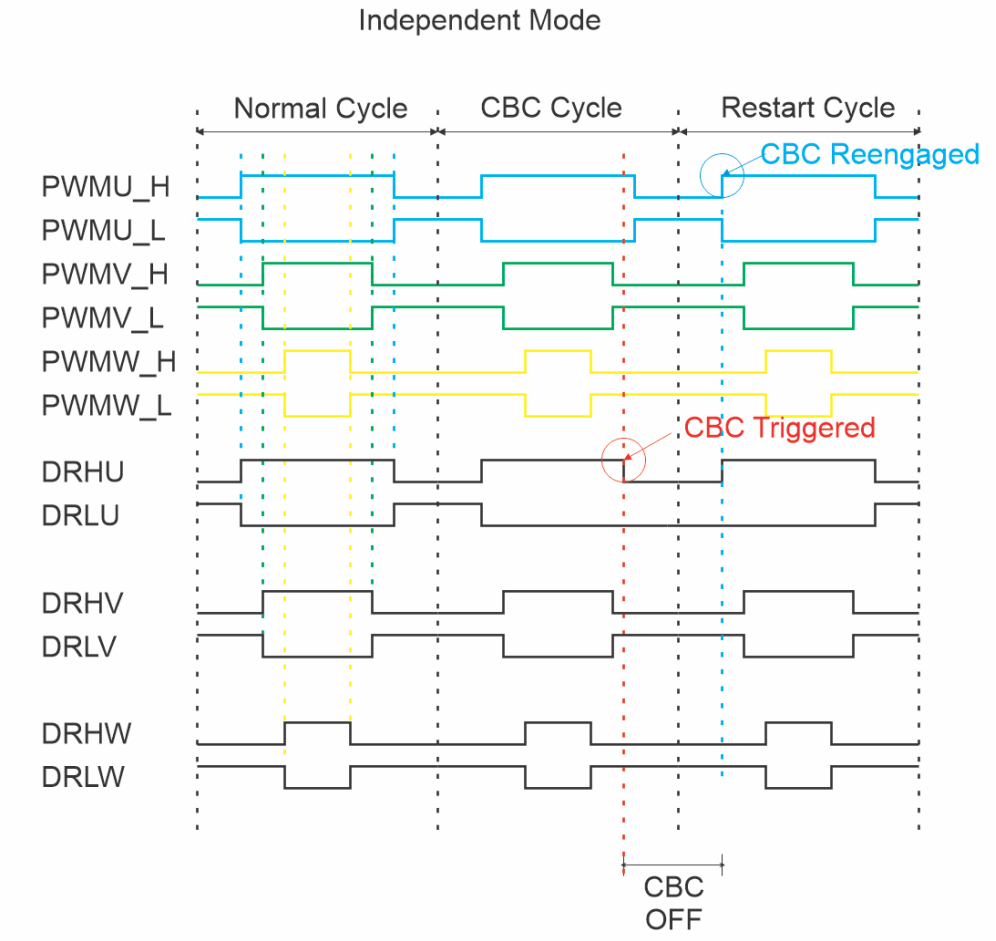
10.3.7 Cycle By Cycle Regulation

The ASPD VDS Sensing block can be used to regulate current by setting the trip level at the drain to source voltage at which the tri phase inverter is to be disabled. The tri phase inverter is disabled on a cycle by cycle basis (CBC) as soon as any of the high side or low side VDS sensors are triggered. The tri phase inverter will remain in disabled mode until a new PWM edge is detected in any of the three Half H Bridge legs. Four modes of operation are provided: Disable All FETs, Recirculate Through Low Side FETs, Recirculate Through High Side FETs, and Alternate Recirculation. In the Alternate Recirculation mode, the recirculation alternates between high side FETs and low side FETs on a per cycle basis.

10.3.8 Cycle By Cycle Operation Modes

CBC operation can occur in one of two modes: Linked Mode and Independent Mode. In Linked mode, a CBC event in any of the three Half H Bridges will result in the entire tri phase inverter being disable for the remainder of the PWM cycle. Any High Side PWM rising edge will re enable the three phase inverter. In Independent Mode, only the Half H Bridge experiencing a CBC event is disabled for the remainder of the PWM cycle. Next rising on edge on the respective Half H Bridge PWM input will commence a new cycle.

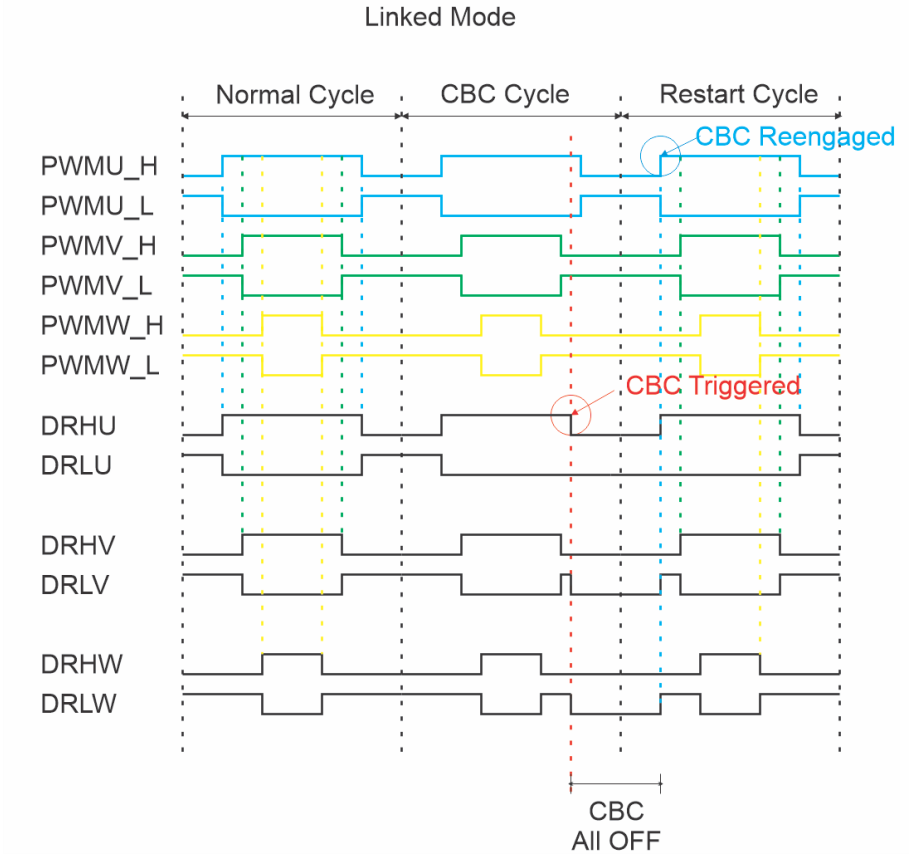



Independent Mode
Normal Cycle
CBC Cycle
Restart Cycle
CBC Reengaged
PWMU_H
PWMU_L
PWMV_H
PWMV_L
PWMW_H
PWMW_L
CBC Triggered
DRHU
DRLU
DRHV
DRLV
DRHW
DRLW
CBC
OFF

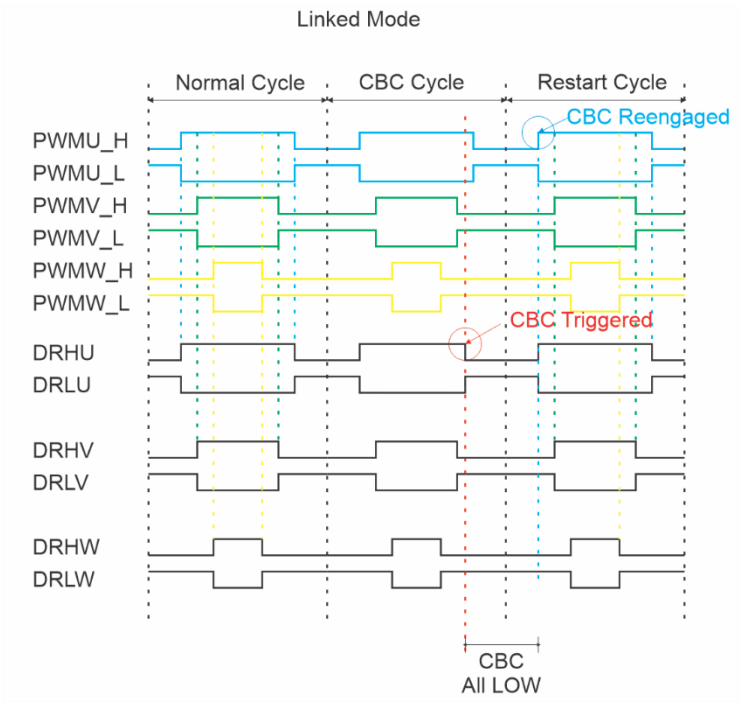
10.3.9 Cycle By Cycle Styles

When a CBC event is registered, current recirculation can happen in one of three ways:

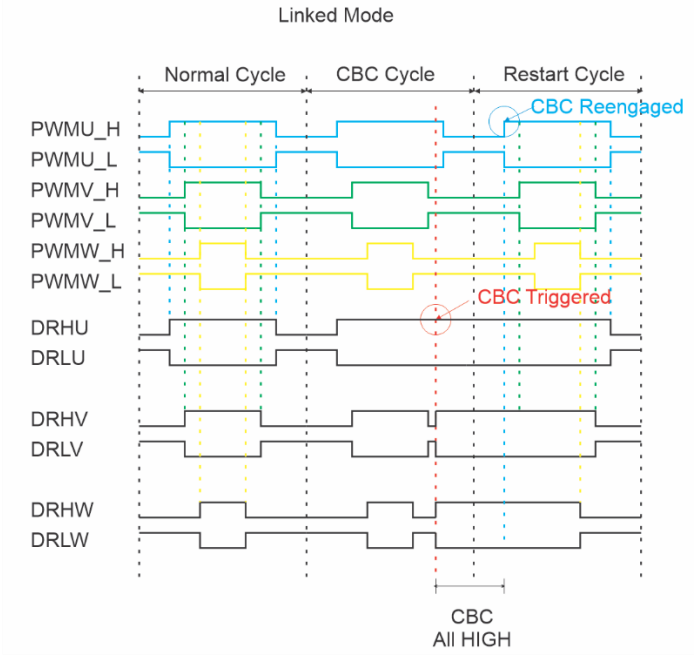
1. All outputs off (asynchronous fast rectification). In this CBC style, the corresponding output is disabled with both the high side and low side FETs being driven OFF. Current recirculates through the body diode. This mode applied to both Linked and Independent Mode.
2. All outputs low (synchronous slow rectification). In this CBC style, the corresponding output is driven low by disabling the high side FET and enabling the low side FET. Current recirculates through all enabled low side FETs. This mode applied to both Linked and Independent Mode.
1. All outputs high (synchronous slow rectification). In this CBC style, the corresponding output is driven high by disabling the low side FET and enabling the high side FET. Current recirculates through all enabled high side FETs. This mode only applies to Linked Mode.



All FETs are disabled during CBC event



High side FETs are disabled and low side FETs are enabled



Low side FETs are disabled and high side FETs are enabled

10.3.1 Drive Disable (nDRVDIS - PAC52711 only)

The nDRVDIS signal provides access to externally driven tri phase inverter power stage disable. This feature has been put in place to allow a secondary and redundant external control unit, to determine when the system is to be allowed to function, while following safety guidelines. Pulling the nDRVDIS line low disables the pre drive power stage. nDRVDIS is also employed to exit Brake Mode. The gate drivers cannot be enabled/disabled in FW.

When an nDRVDIS transition to low assertion is registered, the three phase inverters are immediately disabled. An interrupt at nIRQ1 can be generated if enabled. (For more information refer to the PROTINTEN and PROTSTAT registers detailed within the PAC52710/11 Users Guide document)

10.3.2 Brake (nBRAKE - PAC52711 only)

The nBRAKE signal provides access to externally driven tri phase inverter braking operation. This function has been put in place to allow a secondary and redundant external controller unit, to determine when the system must supply a braking force into the motor drive, to safely stop a motor. Pulling the nBRAKE line low enters Brake Mode. Once in brake mode, the tri phase inverter disables all high side gate drive outputs and only allows low side gate driving. A low level at the nBRAKE input signals that all low side gate drivers must enable their corresponding FETs (slow decay synchronous rectification across the low side FETs).

Every time the nBRAKE signal becomes asserted low, the system can generate an nIRQ1 interrupt, if enabled. (For more information refer to the PROTINTEN and PROTSTAT registers detailed within the PAC52710/11 Users Guide document)

10.3.1 nDRVDIS, nBRAKE - Hibernate Mode (PAC52711 only)

On PAC52711 it is not possible to enter Hibernate mode in firmware, by writing to the HIB bit as with the PAC52710 and other PAC52xx devices. This feature has been put in place to ensure the braking mechanism is preserved under all circumstances. Hibernate mode is still available, but in order to enter this mode, a special hardware based sequence has been introduced. In order to enter hibernate mode, both the nDRVDIS and nBRAKE signal must be pulled low for the blanking period. Once this time is met, the device enters hibernate mode with the AIO6 push button feature enabled. Alternatively, the firmware can enable the Wake Up Timer to have periodic wake up events.

Figure 10-5 Entering/exiting Brake Mode

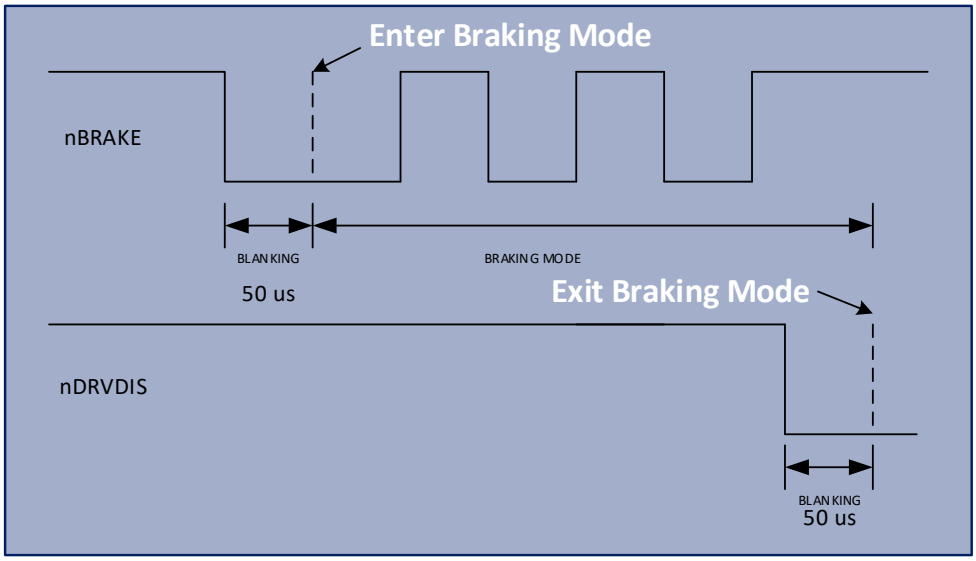


Figure 10-6 External Power Stage Disablement

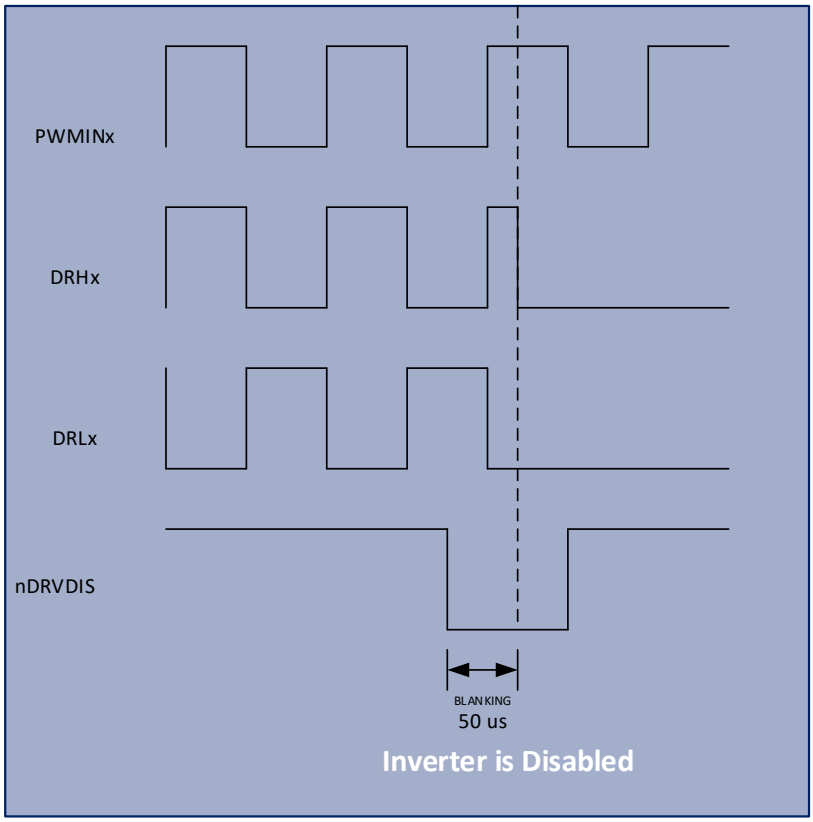


Figure 10-7 Braking Force With PWM Action

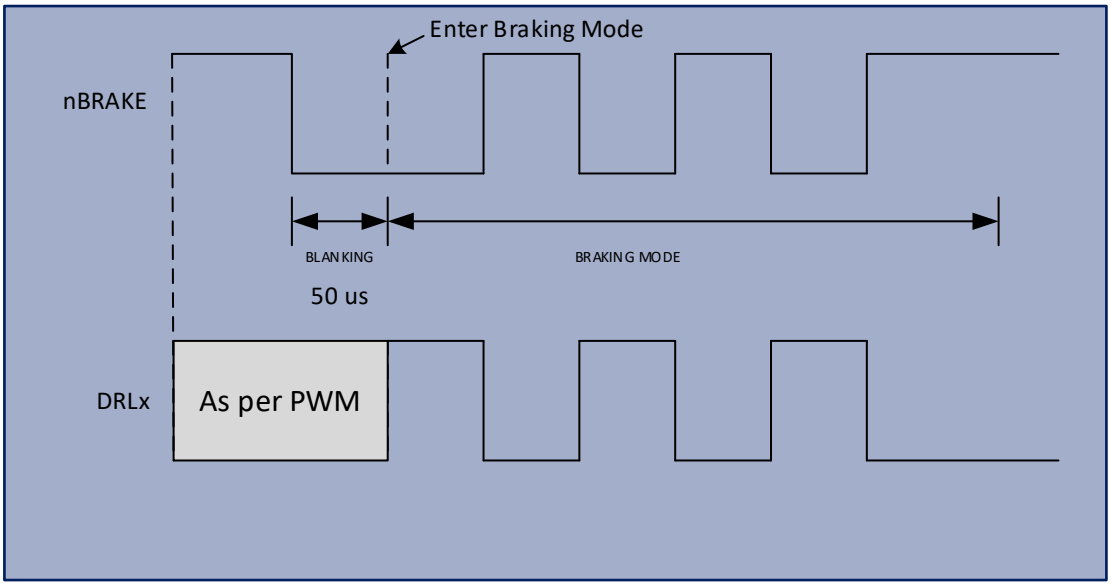
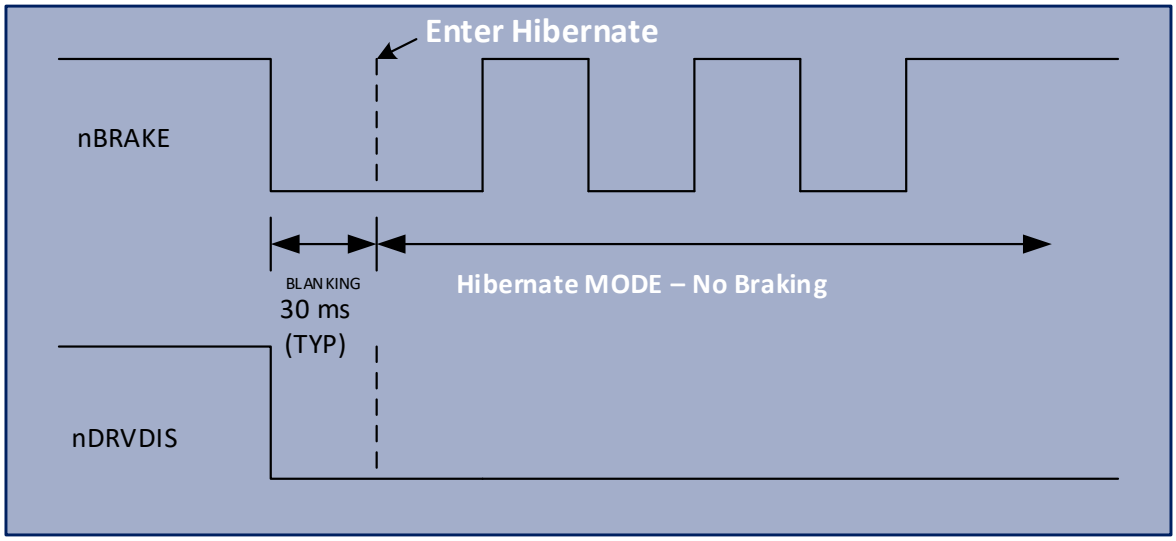


Figure 10-8 Entering Hibernate Mode (PAC52711 only)



10.4 Electrical Characteristics

Table 10-4 Gate Drivers Electrical Characteristics

(V_P = 12V, V_{SYS} = 5V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Low-Side Gate Drivers (DRLx Pins)						
$V_{OH,DRL}$	High-level output voltage	I_{DRLx} = -50mA	V_P−0.3			V
$V_{OL,DRL}$	Low-level output voltage	I_{DRLx} = 50mA			0.2	V
$I_{OHPK,DRL}$	High-level pulsed peak source current	10µs pulse		-1.0		A
$I_{OLPK,DRL}$	Low-level pulsed peak sink current	10µs pulse		1.8		A
High-Side Gate Drivers (DRHx, DRBx and DRSx Pins)						
V_{DRS}	Level-shift driver source voltage range	Repetitive, 10µs pulse	-5		71	V
		Steady state	0		70	
V_{DRB}	Bootstrap pin voltage range	Repetitive, 10µs pulse	3		83	V
		Steady state	5.2		82	
$V_{BS;DRB}$	Bootstrap supply voltage range	V_{DRBx}, relative to respective V_{DRSx}	5.2		16	V
$V_{UVLO;DRB}$	Bootstrap UVLO threshold	V_{DRBx} rising, relative to respective V_{DRSx} ,hysteresis= 0.5V		3.5	4.6	V
$I_{BS;DRB}$	Bootstrap circuit supply current	Gate Driver Disabled		27	50	µA
		Gate Driver Enabled		38	60	
$I_{OS;DRB}$	Offset supply current	Gate Driver Disabled		0.5	10	µA
		Gate Driver Enabled		0.5	10	
$V_{OH;DRH}$	High-level output voltage	I_{DRHx} = -50mA	V_{DRBx}−0.3			V
$V_{OL;DRH}$	Low-level output voltage	I_{DRHx} = 50mA			V_{DRSx} +0.2	V
$I_{OHPK;DRH}$	High-level pulsed peak source current	10µs pulse		-1.2		A
$I_{OLPK;DRH}$	Low-level pulsed peak sink current	10µs pulse		1.8		A
High-Side and Low-Side Gate Driver Propagation Delay						
tPD	Propagation Delay1	Delay setting 00		Delay + 0		ns
		Delay setting 01		Delay + 50		ns
		Delay setting 10		Delay + 100		ns
		Delay setting 11		Delay + 200		ns

[1] Delay from Power Driver Propagation Delay

Table 10-5 VDS Comparator Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OFFSET}	Input Offset Voltage	Ta = 25C	-10	0	10	mV
T_{RESP}	Response Time	+/- 100 mV		100		nS
CMRR	Common Mode Rejection Ratio			70		dB
PSRR	Power Supply Rejection Ratio			75		dB
$V_{DS\ BLNK}$	VDS Blanking Time	VDSBLNK = 0x00		250		nS
		VDSBLNK = 0x01		500		nS
		VDSBLNK = 0x02		750		nS
		VDSBLNK = 0x03		1000		nS
		VDSBLNK = 0x04		1250		nS
		VDSBLNK = 0x05		1500		nS
		VDSBLNK = 0x06		1750		nS
		VDSBLNK = 0x07		2000		nS
		VDSBLNK = 0x08		2250		nS
		VDSBLNK = 0x09		2500		nS
		VDSBLNK = 0x0A		2750		nS
		VDSBLNK = 0x0B		3000		nS
		VDSBLNK = 0x0C		3250		nS
		VDSBLNK = 0x0D		3500		nS
		VDSBLNK = 0x0E		3750		nS
		VDSBLNK = 0x0F		4000		nS
$V_{DS\ TLL}$	VDS Trip Voltage Low Side	VDSTTL = 0x00	64	80	96	mV
		VDSTTL = 0x01	96	120	144	mV
		VDSTTL = 0x02	128	160	192	mV
		VDSTTL = 0x03	170	200	230	mV
		VDSTTL = 0x04	204	240	276	mV
		VDSTTL = 0x05	238	280	322	mV
		VDSTTL = 0x06	272	320	368	mV
		VDSTTL = 0x07	306	360	414	mV
		VDSTTL = 0x08	340	400	460	mV
		VDSTTL = 0x09	450	500	550	mV
		VDSTTL = 0x0A	540	600	660	mV
		VDSTTL = 0x0B	630	700	770	mV

		VDSTTL = 0x0c	720	800	880	mV
		VDSTTL = 0x0D	810	900	990	mV
		VDSTTL = 0x0E	900	1000	1100	mV
		VDSTTL = 0x0F	990	1100	1210	mV
$V_{DS\ TLH}$	VDS Trip Voltage Level High side	VDSTLH = 0x00	60	80	100	mV
		VDSTLH = 0x01	90	120	150	mV
		VDSTLH = 0x02	120	160	200	mV
		VDSTLH = 0x03	160	200	240	mV
		VDSTLH = 0x04	192	240	288	mV
		VDSTLH = 0x05	224	280	336	mV
		VDSTLH = 0x06	256	320	384	mV
		VDSTLH = 0x07	288	360	432	mV
		VDSTLH = 0x08	320	400	480	mV
		VDSTLH = 0x09	425	500	575	mV
		VDSTLH = 0x0A	510	600	690	mV
		VDSTLH = 0x0B	595	700	805	mV
		VDSTLH = 0x0C	680	800	920	mV
		VDSTLH = 0x0D	765	900	1035	mV
		VDSTLH = 0x0E	850	1000	1150	mV
		VDSTLH = 0x0F	935	1100	1265	mV

(1) Guaranteed by design.

Table 10-6 nDRVDIS and nBRAKE Electrical Characteristics (PAC52711 only)

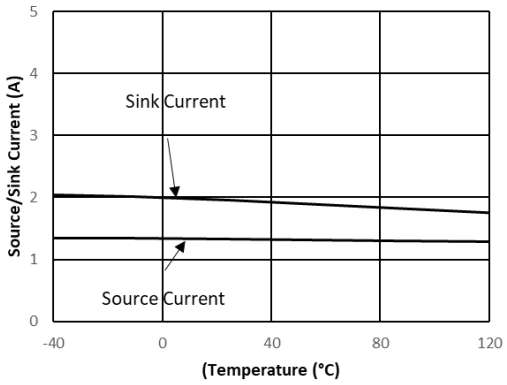
(V_{SYS} = V_{CCIO} = 5V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{AIO}	Pin voltage range		0		5	V
$V_{IH;AIO}$	High-level input voltage		2.2			V
$V_{IL;AIO}$	Low-level input voltage				0.8	V
$t_{BLANK;nBRAKE}$	nBRAKE blanking time		20	50	80	µs
$t_{BLANK;nDRVDIS}$	nDRVDIS blanking time		20	50	80	µs

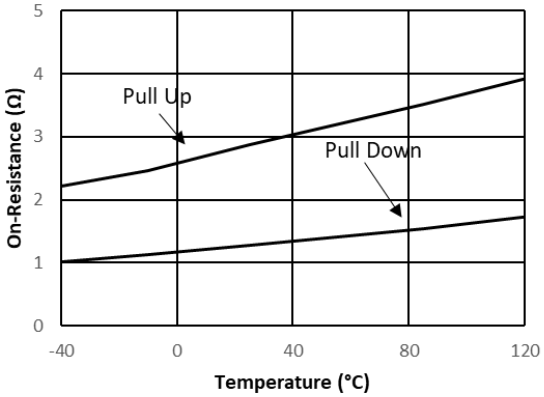
10.5 Typical Performance Characteristics

(V_P = 12V, V_{SYS} = 5V and T_A = 25°C unless otherwise specified.)

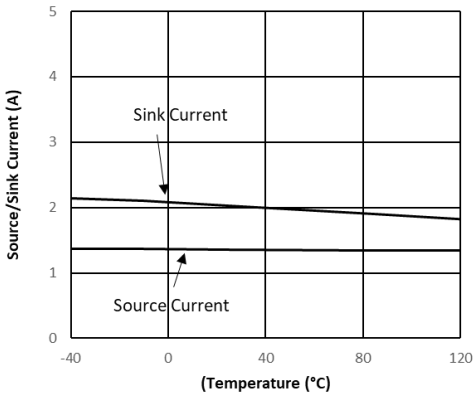
Low-Side Gate Driver (DRLx)
Source/Sink Current vs. Temperature



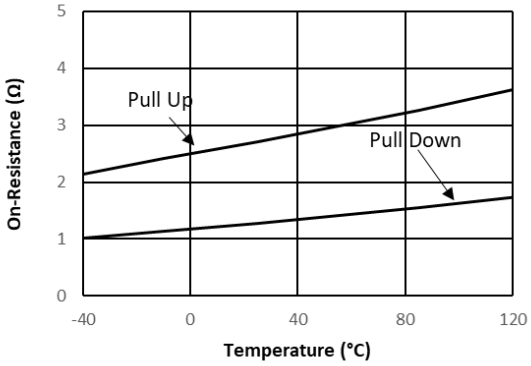
Low-Side Gate Driver (DRLx)
On Resistance vs. Temperature



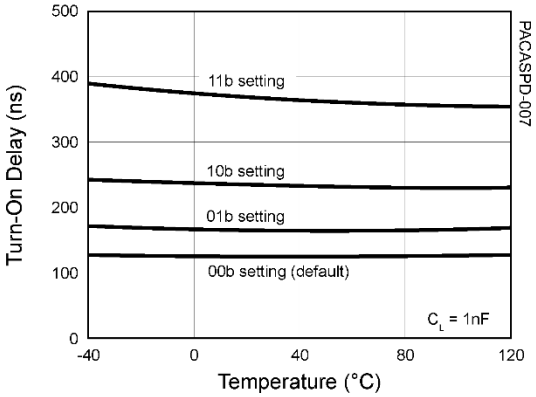
High-Side Gate Driver (DRHx)
Source/Sink Current vs. Temperature



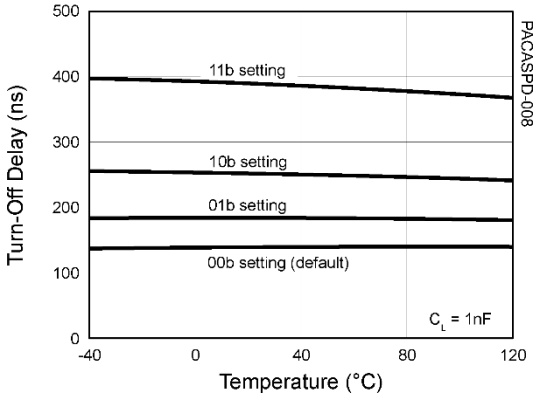
High-Side Gate Driver (DRHx)
On Resistance vs. Temperature



Low-Side Gate Driver (DRLx)
Turn-On Delay vs. Temperature

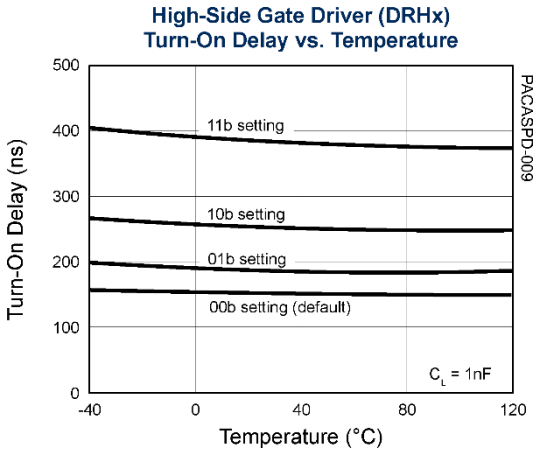


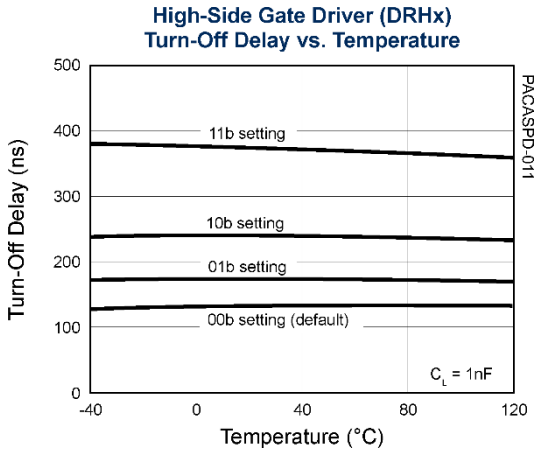
Low-Side Gate Driver (DRLx)
Turn-Off Delay vs. Temperature



Typical Performance Characteristics (Continued)

(V_P = 12V, V_{SYS} = 5V and T_A = 25°C unless otherwise specified.)

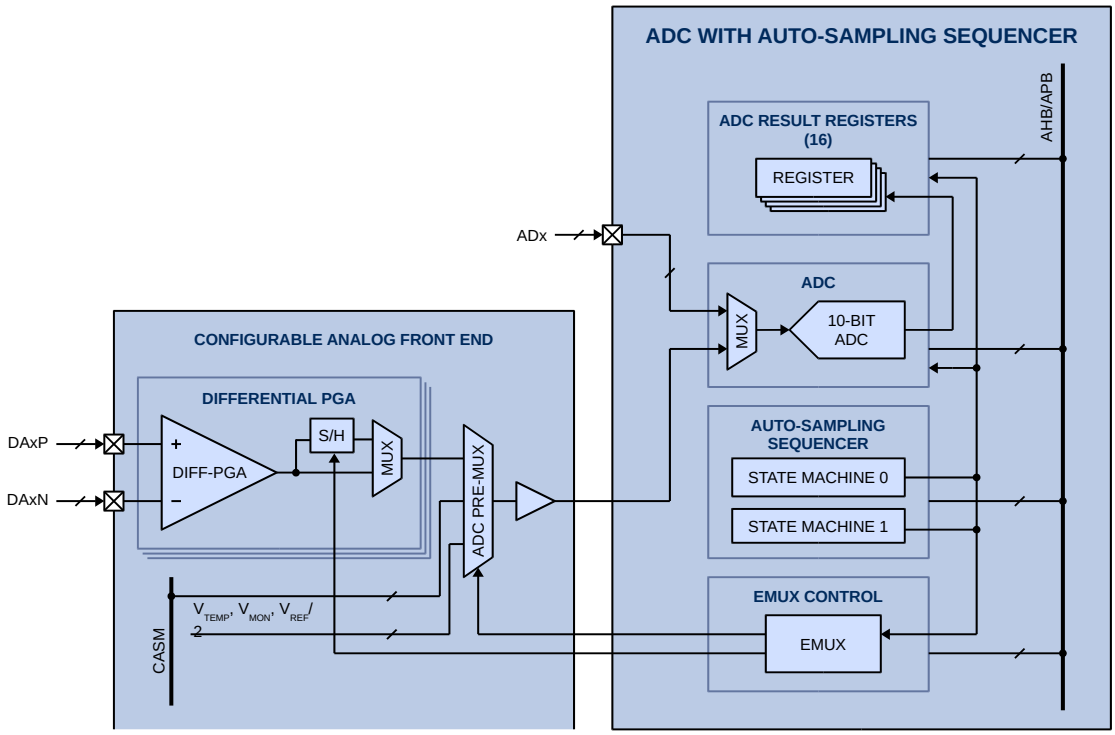




11 ADC WITH AUTO-SAMPLING SEQUENCER

11.1 Block Diagram

Figure 11-1 ADC with Auto-Sampling Sequencer



11.2 Functional Description

11.2.1 ADC

The analog-to-digital converter (ADC) is a 10-bit succesive approximation register (SAR) ADC with 1 µs conversion time and up to 1MSPS capability. The ADC input clock has a user-configurable divider from /1 to /8 of the system clock. The integrated analog multiplexer allows selection from up to 6 direct ADx inputs, and from up to 10 analog inputs signals in the Configurable Analog Front End (CAFE), including up to 3 differential input pairs. The ADC can be configured for repeating or non-repeating conversions and can interrupt the microcontroller when a conversion is finished.

11.2.2 Auto-Sampling Sequencer

Two independent and flexible auto-sampling sequencer state machines allow signal sampling using the ADC without interaction from microcontroller core. Each auto-sampling sequencer state machine can be programmed to take and store up to 8 samples each in the ADC result register from different analog inputs, able to control the ADC MUX and ADC Premux as well as the precise timing of the S/H in the Configurable analog front end. The sampling start of the auto-sampling sequencer can be precisely triggered using timers A, B, C, or D or any of their associated PWM edges (high-to-low or low-to-high). It also supports manual start or a ping-pong-scheme, where one auto-sampling sequencer state machine triggers the other when it finishes sampling.

The auto-sampling sequencer can interrupt the microcontroller when either conversion sequence is finished.

11.2.3 EMUX Control

A dedicated low latency interface controllable by the auto-sampling sequencer or register control allows changing the ADC premultiplexer and asserting/deasserting the S/H circuit in the configurable analog front end, allowing back to back conversions of multiple analog inputs without microcontroller interaction.

11.3 Electrical Characteristics

Table 11-1 ADC and Auto-Sampling Sequencer Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
ADC						
f_{ADCLK}	ADC conversion clock input				16	MHz
t_{ADCONV}	ADC conversion time	f_{ADCLK} = 16MHz			1	µs
	ADC resolution			10		bits
	ADC effective resolution		9.2			bits
	ADC differential non-linearity (DNL)			±0.5		LSB
	ADC integral non-linearity (INL)			±1		LSB
	ADC offset error			0.6		%FS
	ADC gain error			0.12		%FS
Reference Voltage						
V_{REFADC}	ADC reference voltage input			2.5		V
Sample and Hold						
t_{ADCSH}	ADC sample and hold time	f_{ADCLK} = 16MHz		188		ns
C_{ADCIC}	ADC input capacitance			1.3		pF
Input Voltage Range						
V_{ADCIN}	ADC input voltage range	ADC multiplexer input	0		V_{REFADC}	V
EMUX Clock Speed						
$f_{EMUXCLK}$	EMUX engine clock input				50	MHz
PLL Clock Speed						
f_{OUTPLL}	PLL output frequency	T_A = -40°C to 85°C	3.5		100	MHz
		T_A = 85°C to 105°C	3.5		80	MHz

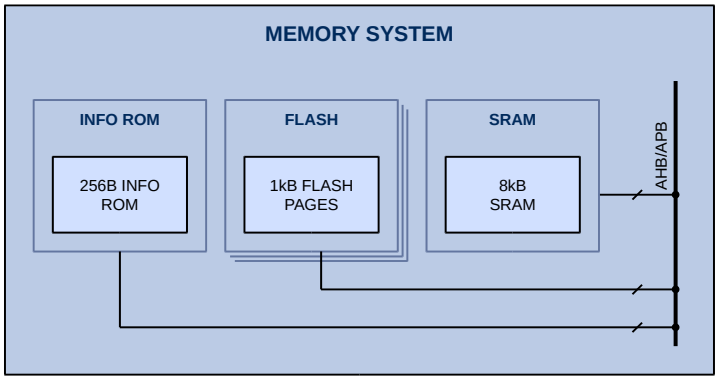
12 MEMORY SYSTEM

12.1 Features

- 32kB embedded FLASH
  - 100,000 program/erase cycles
  - 10 years data retention
- 8kB SRAM

12.2 Block Diagram

Figure 12-1 Memory System



12.3 Functional Description

The device has multiple banks of embedded FLASH memory, SRAM memory, as well as peripheral control registers that are all program-accessible in a flat memory map.

12.3.1 Program and Data FLASH

32kB in 32 pages of 1kB each is available for program or data memory. Each of them can be individually erased or written to while the microcontroller is executing a program from SRAM.

12.3.2 SRAM

Up to 8kB contiguous array of SRAM is available for non-persistent data storage. The SRAM memory supports word (4-byte), half-word (2-byte) and byte address aligned access. The microcontroller may execute code out of SRAM for time-critical applications, or when modifying the contents of FLASH memory.

12.4 Electrical Characteristics

Table 12-1 Memory System Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Embedded FLASH						
$t_{READ;FLASH}$	FLASH read time		40			ns
$t_{WRITE;FLASH}$	FLASH write time		20			µs
$t_{PERASE;FLASH}$	FLASH page erase time				10	ms
$N_{PERASE;FLASH}$	FLASH program/erase cycles			100k		cycles
$t_{DR;FLASH}$	FLASH data retention		10			years
SRAM						
t_{SRAM}	SRAM access cycle time		20			ns

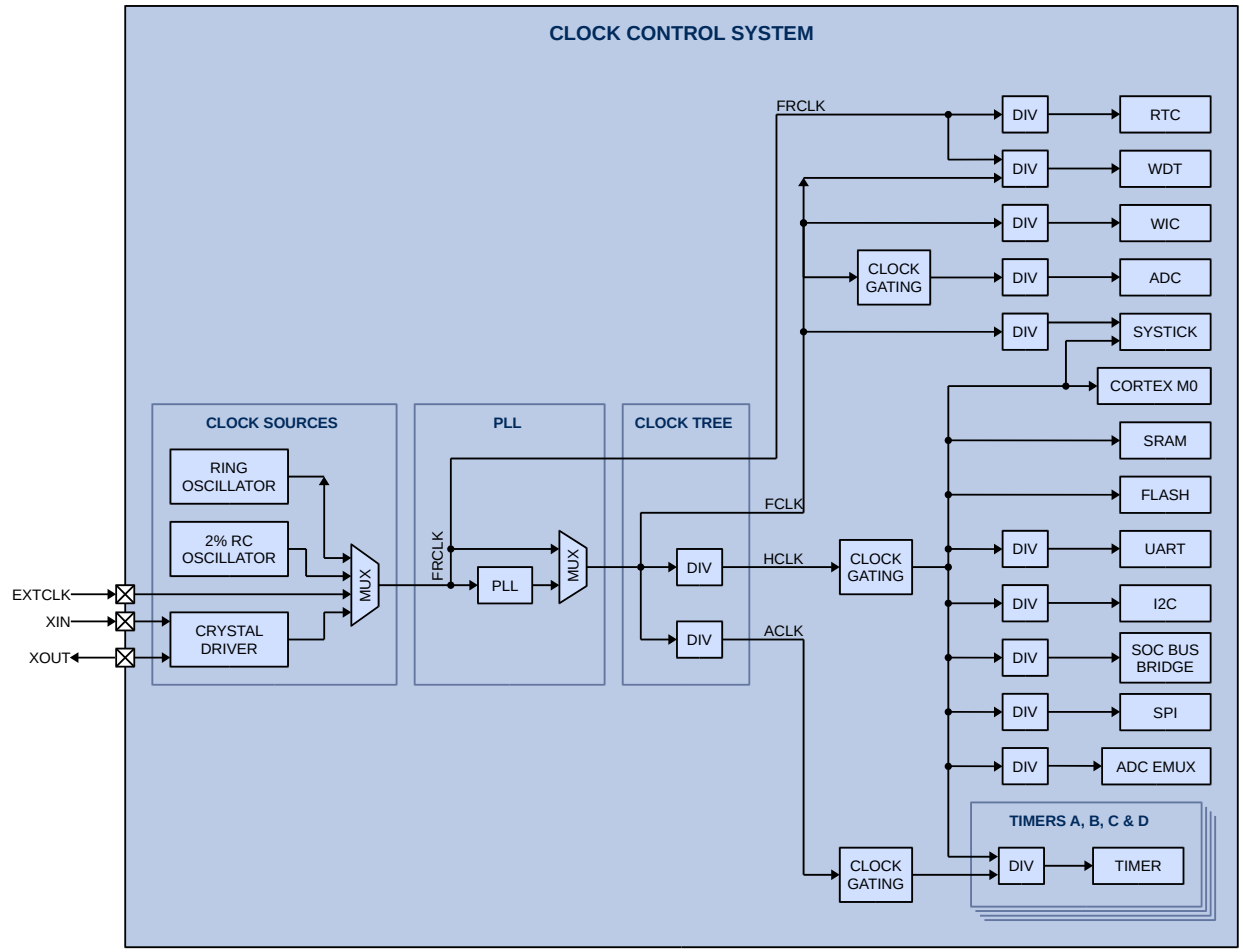
13 CLOCK CONTROL SYSTEM

13.1 Features

- Ring oscillator with 7.5MHz, 9.6MHz, 13.8MHz, and 25.7MHz settings
- High accuracy 2% trimmed 4MHz RC oscillator
- Crystal oscillator driver supporting 2MHz to 10MHz crystals
- External clock input up to 40MHz
- PLL with 1MHz to 25MHz input, and 3.5MHz to 100MHz output
- /1 to /8 clock divider for HCLK
- /1 to /128 clock divider for ACLK

13.2 Block Diagram

Figure 13-1 Clock Control System



13.3 Functional Description

The PAC clock control system covers a wide range of applications.

13.3.1 Free Running Clock (FRCLK)

The free running clock (FRCLK) is generated from one of the 4 clock sources: ring oscillator, trimmed RC oscillator, crystal driver or external clock input. The FRCLK is used for the real-time clock (RTC), watchdog timer (WDT), input to the PLL, or FCLK source to clock the system in low power and sleep mode.

13.3.2 Fast Clock (FCLK)

The fast clock (FCLK) is generated from the PLL or supplied by the FRCLK directly. The FCLK supplies the watchdog timer (WDT), ADC, wake-up interrupt controller (WIC), SysTick timer, Arm® Cortex®-M0 peripheral high speed clock (HCLK) and low speed clock (LSCLK).

13.3.3 High-Speed Clock (HCLK)

The high-speed clock (HCLK) is derived from the FCLK with a /1, /2, /4 or /8 divider. It supplies the peripheral AHB/APB bus, Timers A to D, dead-time controllers, SPI interface, I^2C interface, UART interface, EMUX interface, SOC bus bridge and memory subsystem, and can go as high as 50MHz.

13.3.4 Auxiliary Clock (ACLK)

The auxiliary clock (ACLK) is derived from FCLK with a /1, /2, to /128 divider, and supplies the timer and dead-time blocks. It can be clocked faster or slower than HCLK and can go as high as 100MHz.

13.3.5 Clock Gating

The clock tree supports clock gating in deep-sleep mode for the timer block, ADC, SPI interface, I^2C interface, UART interface, memory subsystem and the Arm® Cortex®-M0 itself.

13.3.6 Ring Oscillator (ROSC)

The integrated ring oscillator provides 4 different clocks with 7.5MHz, 9.6MHz, 13.8MHz, and 25.7MHz settings. After reset, the clock tree always defaults to this clock input with the lowest frequency setting.

13.3.7 Trimmed 4MHz RC Oscillator

The 2% trimmed 4MHz RC oscillator provides an accurate clock suitable for many applications. It is also used to derive the clock for the Multi-Mode Power Manager.

13.3.8 Internal Slow RC Oscillator

An internal 32kHz RC oscillator is used during start up to provide an initial clock to analog circuitry. It is not used as a clock input to the clock tree.

13.3.9 Crystal Oscillator Driver

The optional crystal oscillator driver can drive crystals from 2MHz to 10MHz to provide a highly accurate and stable clock into the system.

13.3.10 External Clock Input

The clock tree can be supplied with an external clock up to 10MHz.

13.3.11 PLL

The integrated PLL input clock is supplied by the FRCLK with an input frequency range of 1MHz to 25MHz. The PLL output frequency is adjustable from 3.5MHz to 100MHz.

13.4 Electrical Characteristics

Table 13-1 Clock Control System Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Clock Tree (FRCLK, FCLK, HCLK, and ACLK)						
f_{FRCLK}	Free running clock frequency				50	MHz
f_{FCLK}	Fast clock frequency				100	MHz
f_{HCLK}	High-speed clock frequency				50	MHz
f_{ACLK}	Auxiliary clock frequency				100	MHz
Internal Oscillators						
f_{ROSC}	Ring oscillator frequency	Frequency setting = 11b		7.5		MHz
		Frequency setting = 10b		9.6		
		Frequency setting = 01b		13.8		
		Frequency setting = 00b		25.7		
f_{TRIM}	Trimmed RC oscillator frequency	T_A = 25°C	-2%	4	2%	MHz
		T_A = -40°C to 105°C	-3%	4	3%	
	Trimmed RC oscillator clock jitter	T_A = -40°C to 85°C		0.5		%
Crystal Oscillator Driver						
$V_{IH;XIN}$	XIN high-level input voltage		0.65•V_{CC18}			V
$V_{IL;XIN}$	XIN low-level input voltage				0.35•V_{CC18}	V
f_{XTAL}	Crystal oscillator frequency range		2		10	MHz
	Recommended capacitive load	f_{XTAL} = 2MHz to 3MHz		25		pF
		f_{XTAL} = 3MHz to 6MHz		20		
		f_{XTAL} = 6MHz to 10MHz		16		
	External circuit ESR	f_{XTAL} = 2MHz to 3MHz			1000	Ω
		f_{XTAL} = 3MHz to 6MHz			400	
		f_{XTAL} = 6MHz to 10MHz			100	
External Clock Input						
f_{EXTCLK}	External clock input frequency range				40	MHz
$t_{HIGH;EXTCLK}$	External clock high time		10			ns
$t_{LOW;EXTCLK}$	External clock low time		10			ns
PLL						
f_{INPLL}	PLL input frequency range		2		25	MHz
f_{OUTPLL}	PLL output frequency range		3.5		100	MHz
	PLL settling time			0.5		ms
	PLL period jitter	RMS		30		ps
		Peak to peak		±150		

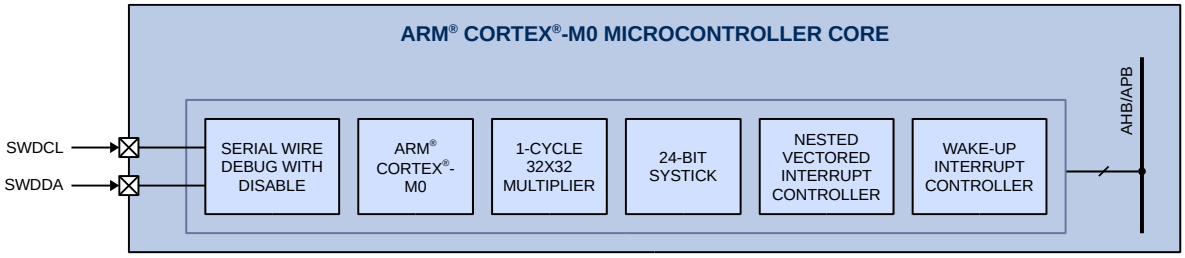
14 ARM® CORTEX®-M0 MICROCONTROLLER CORE

14.1 Features

- Arm® Cortex®-M0 core
- Fast single-cycle 32-bit x 32-bit multiplier
- 24-bit SysTick timer
- Up to 50MHz operation
- Serial wire debug (SWD), with 4 break-point and 2 watch-point unit comparators
- Nested vectored interrupt controller (NVIC) with 25 external interrupts
- Wake-up interrupt controller (WIC) with GPIO, real-time clock (RTC) and watchdog timer (WDT) interrupts enabled
- Sleep and deep-sleep mode with clock gating

14.2 Block Diagram

Figure 14-1 Arm Cortex-M0 Microcontroller Core



14.3 Functional Description

The Arm® Cortex®-M0 microcontroller core is configured for little endian operation and includes the fast single-cycle 32-bit multiplier and 24-bit SysTick timer and can operate at a frequency of up to 50MHz.

The microcontroller nested vectored interrupt controller (NVIC) supports 25 external interrupts for the device's peripherals and sub-systems. For low-latency interrupt processing, the NVIC also supports interrupt tail-chaining. The wake-up interrupt controller (WIC) is able to wake up the device from low-power modes using any GPIO interrupt, as well as from the RTC or WDT. The Arm® Cortex®-M0 supports both sleep and deep-sleep low-power modes. The deep-sleep mode supports clock gating to limit standby power even further.

Firmware debug support includes 4 break-point and 2 watch-point unit comparators using the serial wire debug (SWD) protocol. The serial wire debug mechanism can be disabled to prevent device access to the firmware in the field.

14.4 Electrical Characteristics

Table 14-1 Microcontroller and Clock Control System Electrical Characteristics

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

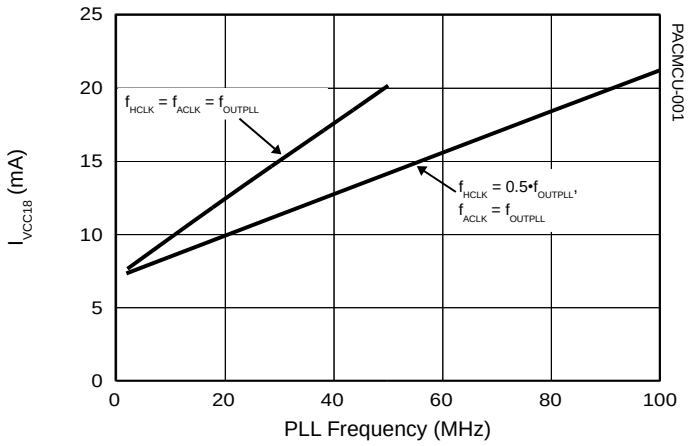
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{HCLK}	Microcontroller clock	HCLK			50	MHz
$I_{OP;VSYS}$	V_{SYS} operating supply current	f_{FRCLK} = f_{HCLK} = f_{ACLK} = ROSC 11b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	2.5(1)	3.4	7	mA
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = ROSC 10, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	3.0(1)	4	7.8	
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = ROSC 01, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	4.1(1)	5.3	9.5	
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = ROSC 00, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	7.4(1)	9	15	
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = CLKREF, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	1.5(1)	2.3	4.4	
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = 10MHz XTAL, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	3.6(1)	4.5	6.7	
		f_{FRCLK} = 4MHz CLKREF, f_{HCLK} = 50MHz, f_{ACLK} = f_{OUTPLL} = 100MHz, CPU halt; other clock sources, ADC, timers, and serial interface disabled	20.9(1)	23.3	26.5	

(1)All minimum operating supply current values are for room temperature only

14.5 Typical Performance Characteristics

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = 25°C unless otherwise specified.)

I_{VCC18} vs. PLL Frequency



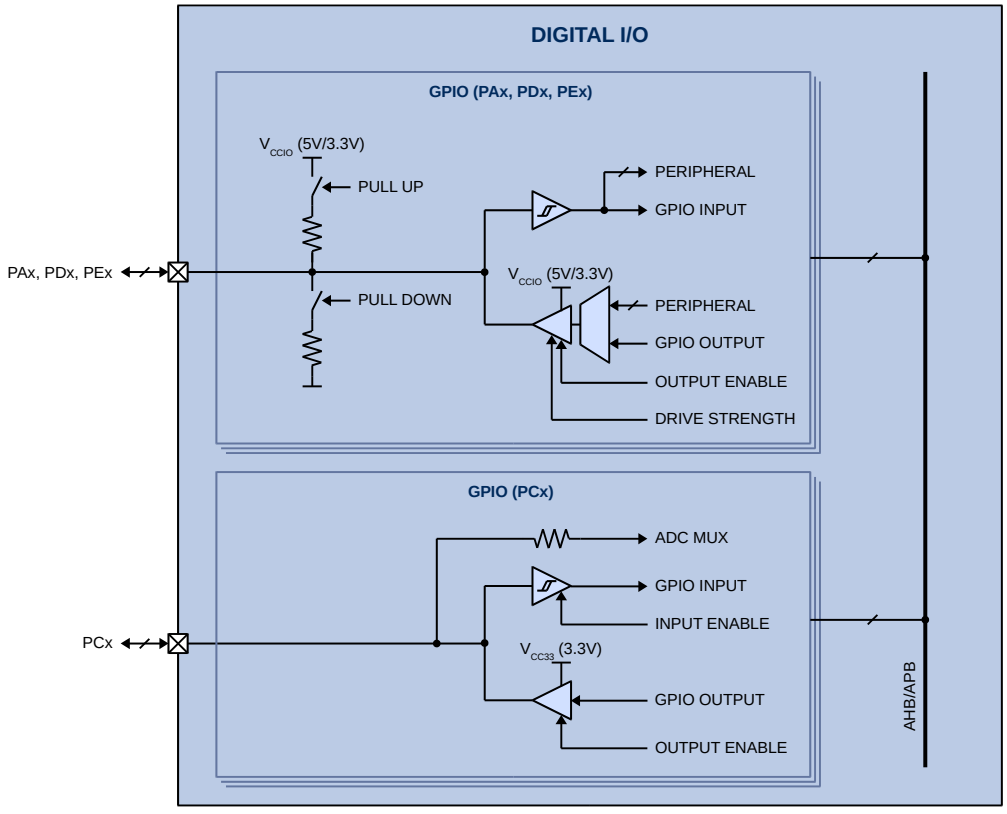
15 I/O CONTROLLER

15.1 Features

- 5V-compliant I/O PAx, PDx, PEx
- 3.3V-compliant I/O PCx
- Configurable drive strength on PAx, PDx, PEx
- Configurable pull-up or pull-down on PAx, PDx, PEx

15.2 Block Diagram

Figure 15-1 I/O controller



15.3 Functional Description

The PAC can support up to 4 ports with 8 I/Os each from PAx, PCx, PDx, and PEx, in addition to the I/Os on the analog front end. All PAx, PCx, PDx, and PEx ports have interrupt capability with configurable interrupt edge.

PAx, PDx, and PEx I/Os use V_{CCIO} as the I/O supply voltage that is 5V on default parts (and 3.3V available from factory). The drive current can be configured as 8mA or 16mA. They also support weak pull-up and pull-down to save external components.

PCx uses V_{CC33} as its I/O supply voltage. The drive current is fixed to 8mA. PC0 to PC5 are also associated with analog inputs AD0 to AD5 to the ADC.

15.4 GPIO Current Injection

Under normal operation, there should not be current injected into the GPIOs on the device due to the GPIO voltage below ground or above the GPIO supply.[2] Current injected occurs when the GPIO pin voltage is less than -0.3V or when greater than GPIO supply + 0.3V.

In order provide a robust solution when this situation occurs, this device allows a small amount of injected current into the GPIO pins, to avoid excessive leakage or device damage.

For information on the GPIO current injection thresholds, see the absolute maximum parameters for this device.

Sustained operation with the GPIO pin voltage greater than the GPIO supply or when the GPIO pin voltage is less than -0.3V may result in reduced lifetime of the device. GPIO current injection should only be a temporary condition.

[2] VCC33 is the supply for any PC GPIO pin and VCCIO is the supply for any other GPIO pins.

15.5 Electrical Characteristics

Table 15-1 I/O Controller Electrical Characteristics

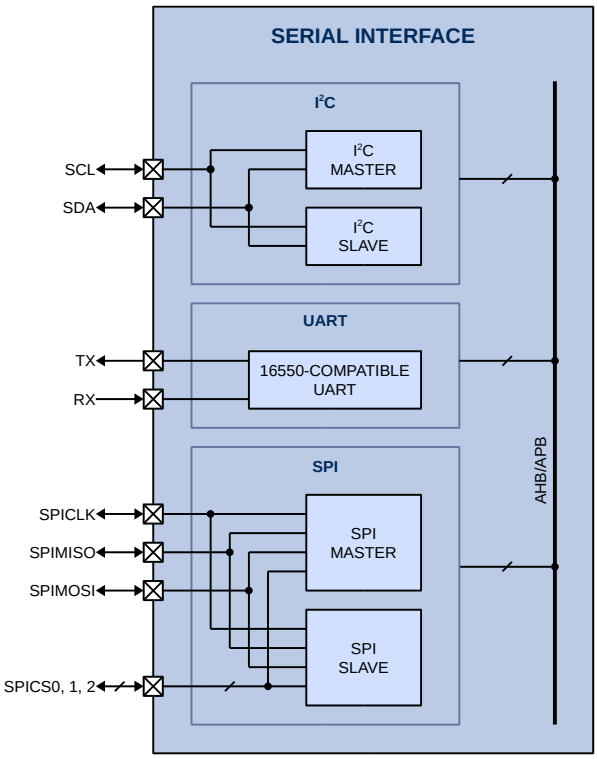
(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
PAx, PDx, PEx (5V Operation)							
V_{IH}	High-level input voltage	V_{CCIO} = 5V		3			V
V_{IL}	Low-level input voltage	V_{CCIO} = 5V				0.8	V
I_{OL}	Low-level output sink current	V_{CCIO} = 5V, V_{OL} = 0.4V	Drive strength setting = 0b	7			mA
			Drive strength setting = 1b	15			
I_{OH}	High-level output source current	V_{CCIO} = 5V, V_{OH} = 2.4V	Drive strength setting = 0b			-7	mA
			Drive strength setting = 1b			-15	
R_{PU}	Weak pull-up resistance	V_{CCIO} = 5V		53	66	87	kΩ
R_{PD}	Weak pull-down resistance	V_{CCIO} = 5V		63	108	244	kΩ
I_{IL}	Input leakage current	T_A = 125°C		-10	0	10	µA
PAx, PDx, PEx (3.3V Operation)							
V_{IH}	High-level input voltage	V_{CCIO} = 3.3V		2			V
V_{IL}	Low-level input voltage	V_{CCIO} = 3.3V				0.8	V
I_{OL}	Low-level output sink current	V_{CCIO} = 3.3V, V_{OL} = 0.4V	Drive strength setting = 0b	4			mA
			Drive strength setting = 1b	8			
I_{OH}	High-level output source current	V_{CCIO} = 3.3V, V_{OH} = 2.4V	Drive strength setting = 0b			-4	mA
			Drive strength setting = 1b			-8	
R_{PU}	Weak pull-up resistance	V_{CCIO} = 3.3V		47	74	104	kΩ
R_{PD}	Weak pull-down resistance	V_{CCIO} = 3.3V		50	84	121	kΩ
I_{IL}	Input leakage current	T_A = 125°C		-10	0	10	µA
PCx (3.3V Operation)							
V_{IH}	High-level input voltage	V_{CC33} = 3.3V		2			V
V_{IL}	Low-level input voltage	V_{CC33} = 3.3V				0.8	V
I_{OL}	Low-level output sink current	V_{CC33} = 3.3V, V_{OL} = 0.4V		7			mA
I_{OH}	High-level output source current	V_{CC33} = 3.3V, V_{OH} = 2.4V				-7	mA
I_{IL}	Input leakage current	T_A = 125°C		-10	0	10	µA

16 SERIAL INTERFACE

16.1 Block Diagram

Figure 16-1 Serial Interface



16.2 Functional Description

The device has up to three serial interfaces: I²C, UART, and SPI.

16.2.1 I²C Controller

The I²C controller is a configurable peripheral that can support various modes of operation:

- I²C master operation
  - Normal mode (100kHz), fast mode (400kHz), or fast mode plus (1MHz)
  - Single and multi-master
  - Synchronization (multi-master)
  - Arbitration (multi-master)
  - 7-bit or 10-bit slave addressing
- I²C slave operation
  - Normal mode (100kHz), fast mode (400kHz), or fast mode plus (1MHz)
  - Clock stretching
  - 7-bit or 10-bit slave addressing

The I²C peripheral may operate either by polling, or can be configured to be interrupt driven for both receive and transmit data.

16.3 UART Controller

The UART peripheral is a configurable peripheral that can support various features and modes of operation:

- Programmable clock selection
- National Instruments PC16550D compatible
- 16-deep transmit and receive FIFO and fractional clock divisor
- Up to 3.125Mbps communication speed (with HCLK = 50MHz)

The UART peripheral may operate either by polling, or can be configured to be interrupt driven for both receive and transmit data.

16.4 SPI Controller

The device contains an SPI controller that can each be used in either master or slave operation, with the following features:

- SPI master operation
  - Control of up to three different SPI slaves
  - Operation up to 25MHz
  - Flexible multiple transmit mode for variable-size SPI data with user-defined chip-select behavior
  - Chip select “shaping” through programmable additional delay for chip-select setup, hold and wait time for back-to-back transfers
- SPI master or slave operation

- Supports clock phase and polarity control
- Data transmission/reception can be on 8-, 16-, 24- or 32-bit boundary
- Selectable data bit ordering (LSB or MSB first)
- Programmable chip select polarity
- Selectable “auto-retransmit” mode

The SPI peripheral may operate either by polling, or can be configured to be interrupt driven for both receive and transmit data.

16.5 Dynamic Characteristics

Table 16-1 Serial Interface Dynamic Characteristics

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I²C						
f_{I2CCLK}	I²C input clock frequency	Standard mode (100kHz)	2.8			MHz
		Fast mode (400kHz)	2.8			MHz
		Fast mode plus (1MHz)	6.14			MHz
UART						
$f_{UARTCLK}$	UART input clock frequency				f_{HCLK}/16	MHz
	UART baud rate	f_{HCLK} = 50MHz			3.125	Mbps
SPI						
f_{SPICLK}	SPI input clock frequency	Master mode			f_{HCLK}/2	MHz
		Slave mode			f_{HCLK}/2	MHz

Table 16-2 I²C Dynamic Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Fast mode	0		400	
		Fast mode plus	0		1000	
t_{LOW}	SCL clock low	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
t_{HIGH}	SCL clock high	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{HD;STA}$	Hold time for a repeated START condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{SU;STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{HD;DAT}$	Data hold time	Standard mode	0		3.45	µs
		Fast mode	0		0.9	
		Fast mode plus	0			
$t_{SU;DAT}$	Data set-up time	Standard mode	250			ns
		Fast mode	100			
		Fast mode plus	50			
$t_{SU;STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
t_r	Rise time for SDA and SCL	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus			120	
t_f	Fall time for SDA and SCL	Standard mode			300	ns
		Fast mode			300	
		Fast mode plus			120	
C_b	Capacitive load for each bus line	Standard mode, Fast mode			400	pF
		Fast mode plus			550	pF

Figure 16-2 I²C Timing Diagram

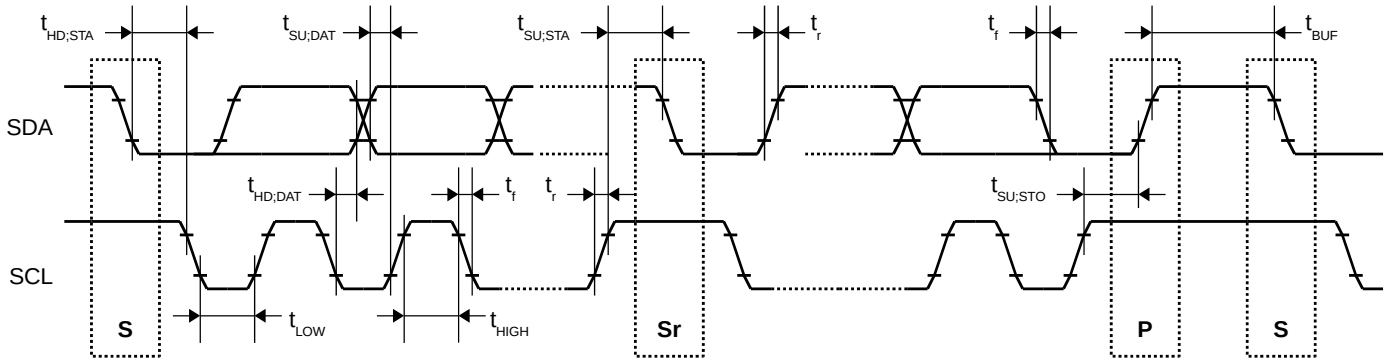
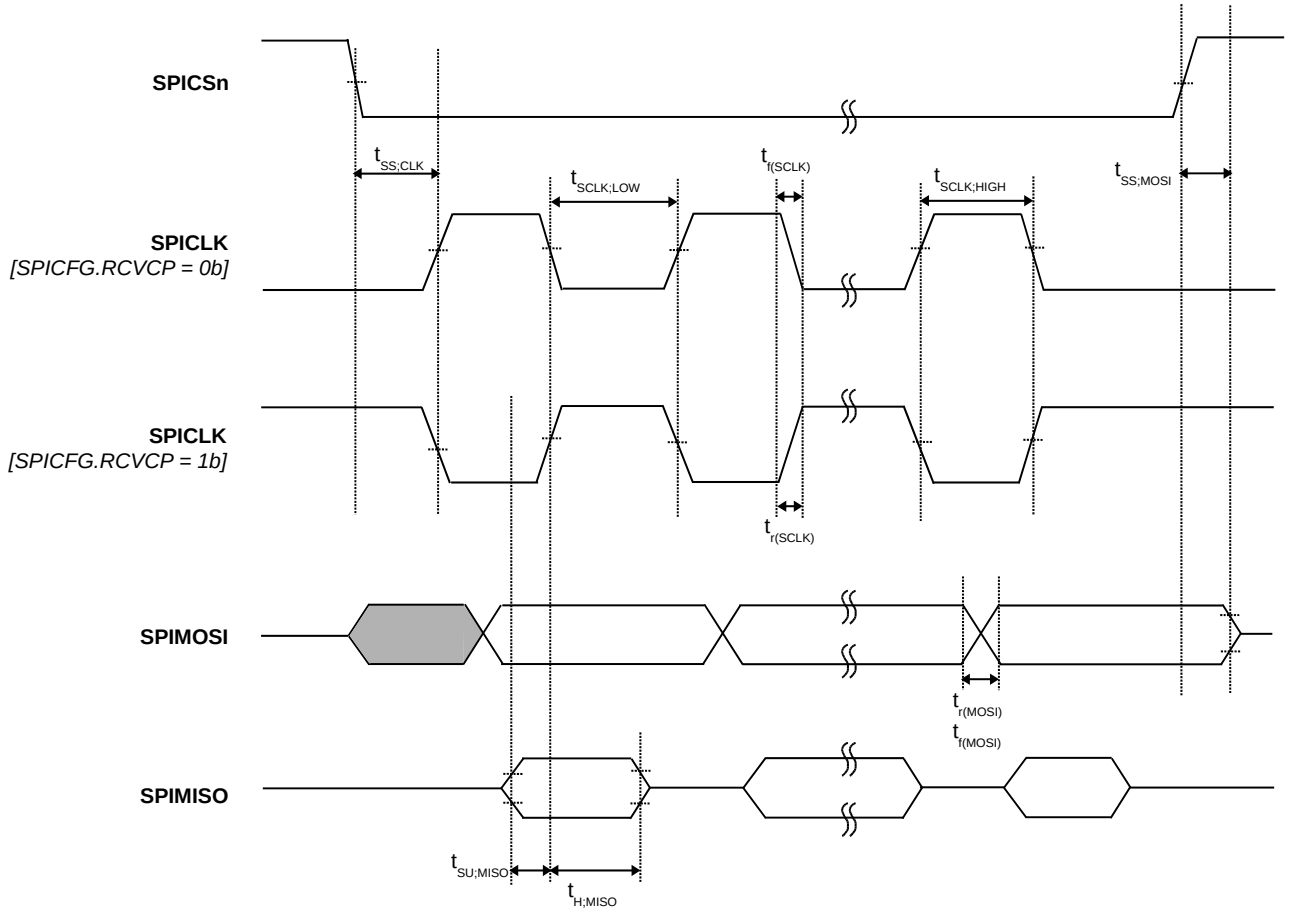


Table 16-3 SPI Dynamic Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SCLK;HIGH}$	SPICLK Input High Time	SPICLK = 25MHz	30			ns
$t_{SCLK;LOW}$	SPICLK Input Low Time		30			ns
$t_{SS;SCLK}$	SPICSn to SPICLK Time		120			ns
$t_{SS;MOSI}$	SPICSn to SPIMISO High-impedance time		10		50	ns
$t_{r(SCLK)}$	SPICLK Rise Time			10	25	ns
$t_{f(SCLK)}$	SPICLK Fall Time			10	25	ns
$t_{r(MOSI)}$	SPIMISO Rise Time			10	25	ns
$t_{f(SMOSI)}$	SPIMISO Fall Time			10	25	ns
$t_{SU;MISO}$	SPIMISO Setup Time		20			ns
$t_{H;MISO}$	SPIMISO Hold Time		20			ns

Figure 16-3 SPI Timing Diagram



17 TIMERS

17.1 Block Diagram

Figure 17-1 Timers A, B, C, and D

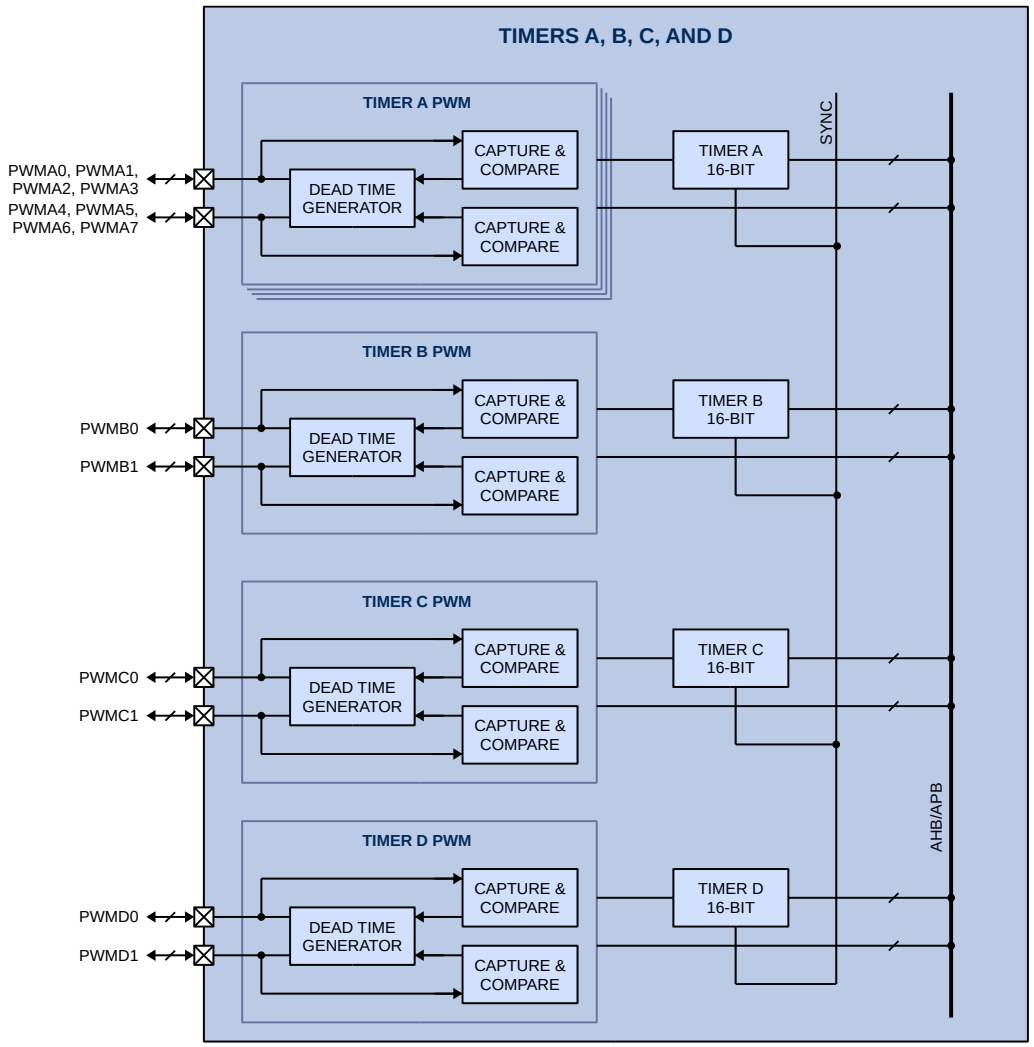


Figure 17-2 AFE Watchdog and Wake-Up Timer

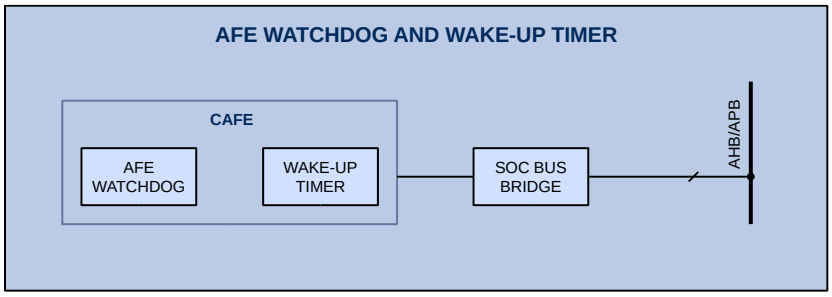
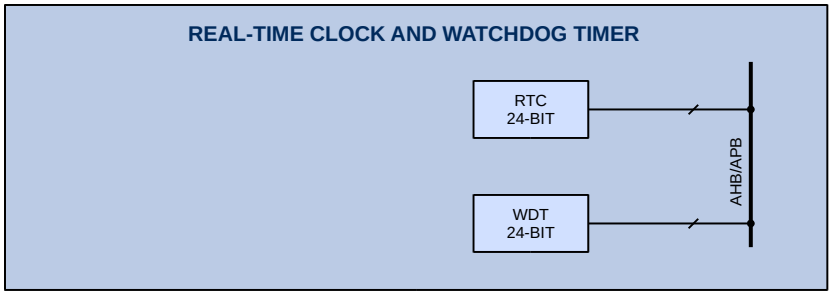


Figure 17-3 Real-Time Clock and Watchdog Timer



17.2 Functional Description

The device includes 9 timers: timer A, timer B, timer C, timer D, watchdog timer 1 (WDT), watchdog timer 2, wake-up timer, real-time clock (RTC), and SysTick timer. The device supports up to 14 different PWM signals and has up to 7 dead-time controllers. Timers A, B, C and D can be concatenated to synchronize to a single clock and start/stop signal for applications that require a synchronized timer period between timers.

17.2.1 Timer A

Timer A is a general purpose 16-bit timer with 8 PWM/capture and compare units. It has 4 pairs of PWM signals going into 4 dead-time controllers. Timer A can be concatenated with timers B, C, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

17.2.2 Timer B

Timer B is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller, as well as 2 additional compare units that can be used for additional system time bases for interrupts. Timer B can be concatenated with timers A, C, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

17.2.3 Timer C

Timer C is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller. Timer C can be concatenated with timers A, B, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

17.2.4 Timer D

Timer D is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller. Timer D can be concatenated with timers A, B, and C to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

17.2.5 Watchdog Timer

The 24-bit watchdog timer (WDT) can be used for long time period measurements or periodic wake up from sleep mode. The watchdog timer can be used as a system watchdog, or as an interval timer, or both. The watchdog timer can use either FRCLK or FCLK as clock input with an additional clock divider from /2 to /65536.

17.2.6 CAFE Watchdog Timer

There is a second watchdog timer in the AFE that can be used to monitor communication between the MCU and AFE on the PAC SOC bus. If this timer expires, it will trigger a device reset when there is no communication for a period of either 4s or 8s.

17.2.7 Wake-Up Timer

The wake-up timer can be used for very low power hibernate and sleep modes to wake up the micro controller periodically. It can be configured to be 125ms, 250ms, 500ms, 1s, 2s, 4, or 8s.

17.2.8 Real-Time Clock

The 24-bit real-time clock (RTC) can be used for time measurements when an accurate clock source is used. This timer can also be used for periodic wake up from sleep mode. The RTC uses FRCLK as clock input with an additional clock divider from /2 to /65536.

18 THERMAL CHARACTERISTICS

Table 18-1 Thermal Characteristics

PARAMETER	VALUE	UNIT
Operating ambient temperature range	-40 to 105	°C
Operating junction temperature range	-40 to 125	°C
Storage temperature range	-55 to 150	°C
Lead temperature (Soldering, 10 seconds)	300	°C
Junction-to-case thermal resistance (θ_{JC})	2.897	°C/W
Junction-to-ambient thermal resistance (θ_{JA})	23.36	°C/W

19 APPLICATION EXAMPLES

The following simplified diagram shows a typical three phase inverter implementation . Refer to application notes for detailed design description.

Figure 19-1 3-Phase Motor Drive Using PAC52710/11 (Simplified Diagram)

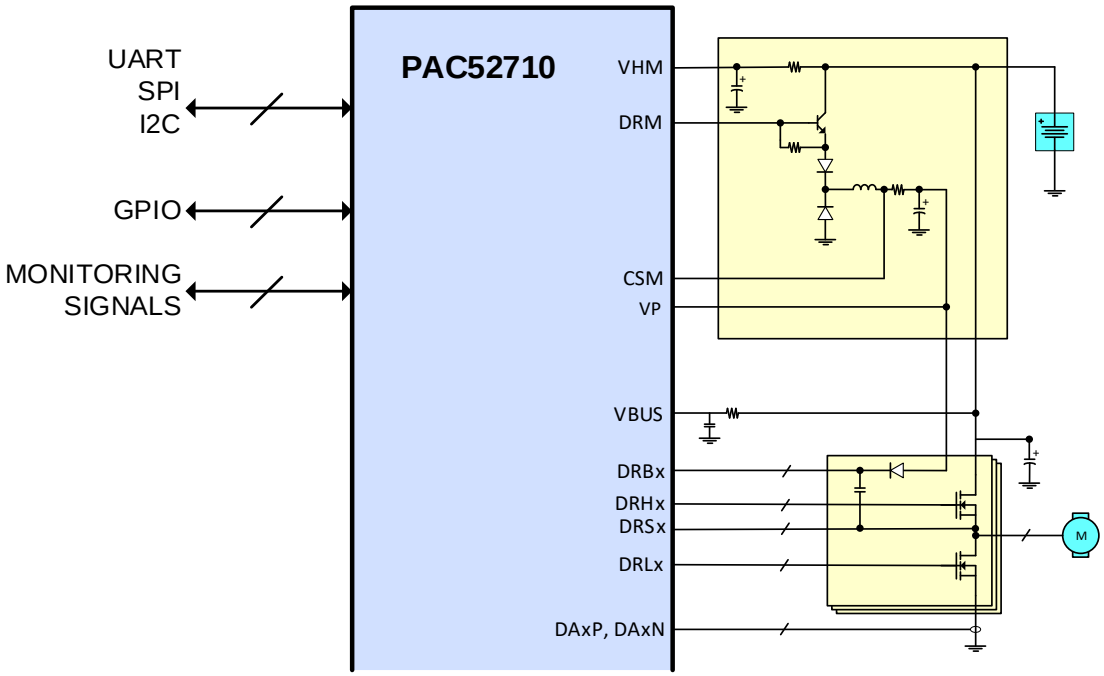
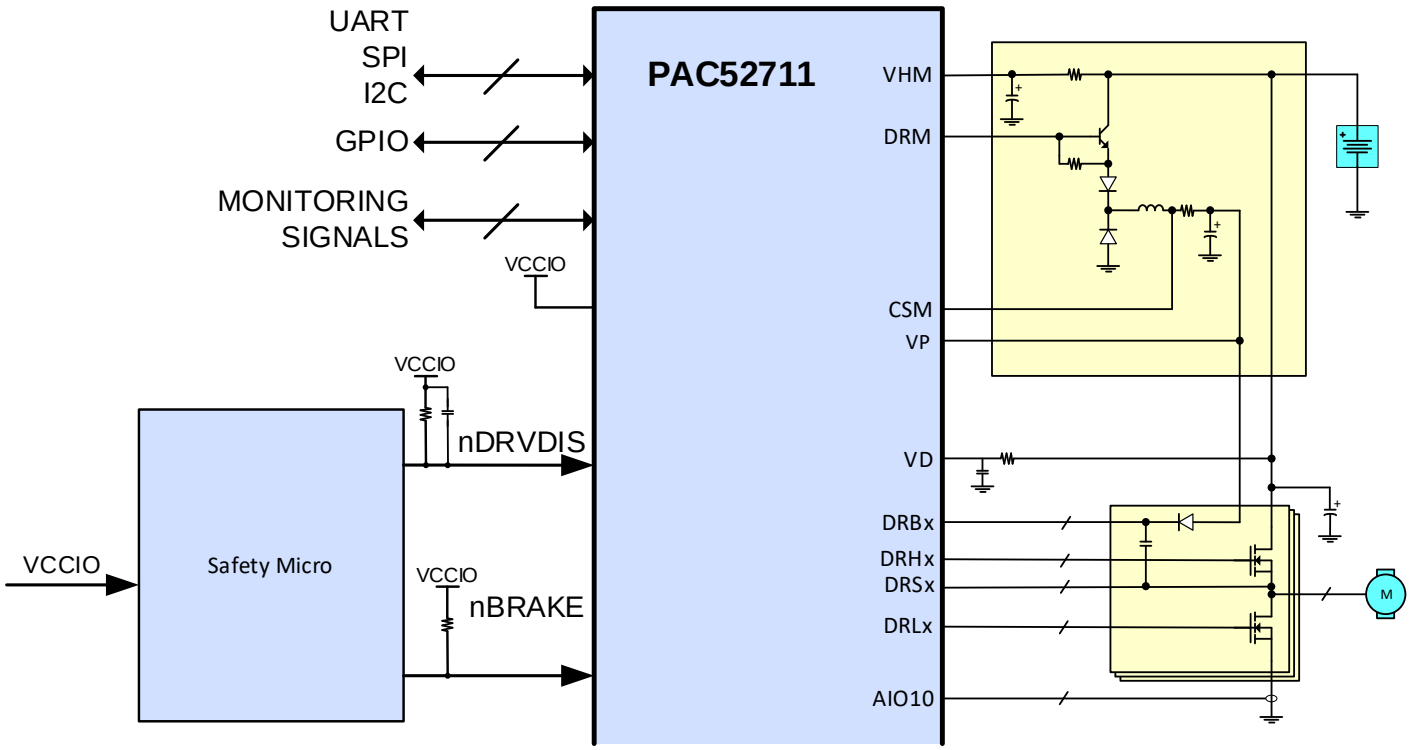


Figure 19-2 3-Phase Motor Drive Using PAC52711 and Safety MCU (Simplified Diagram)



20 PACKAGE OUTLINE AND DIMENSIONS

20.1 TQFN66-48 Package Outline and Dimensions

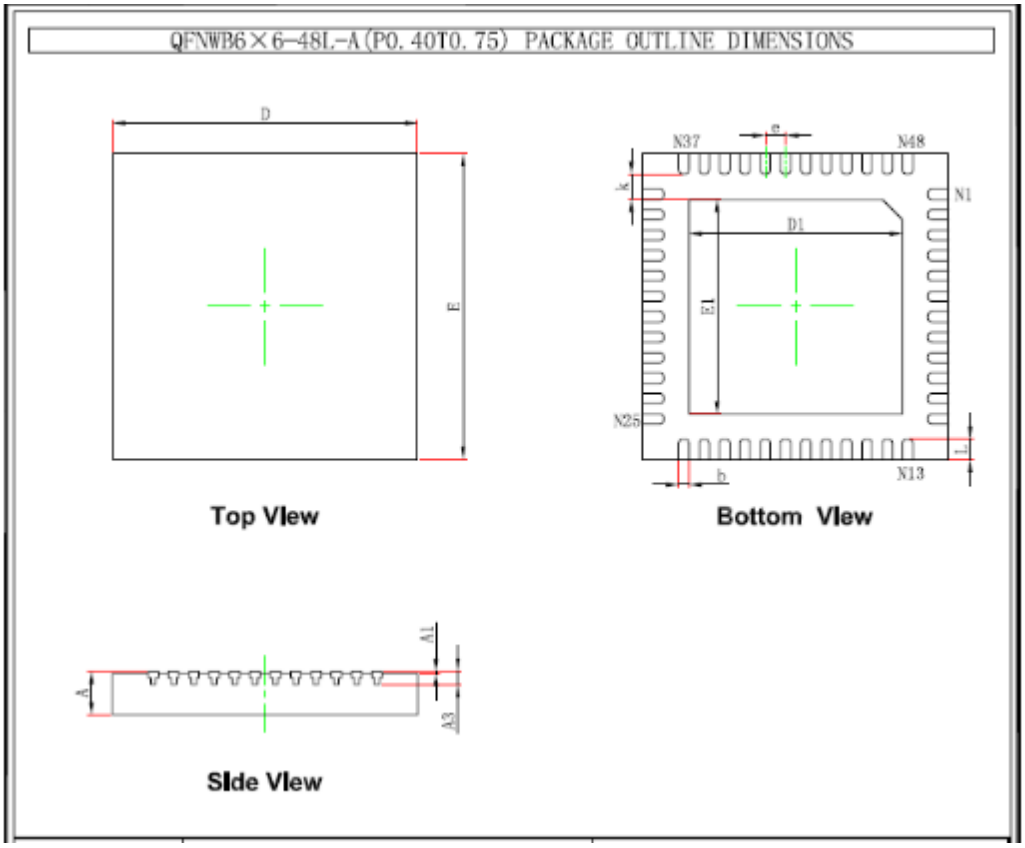


Table 20-1 Dimensions

	Millimeters		Inches	
Dimensions	**Minimum**	**Maximum**	**Minimum**	**Maximum**
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203		0.008	
b	0.150	0.250	0.006	0.010
D	5.924	6.076	0.233	0.239
D1	4.100	4.400	0.161	0.173
E	5.924	6.076	0.233	0.239
E1	4.100	4.400	0.161	0.173
e	0.400		0.016	
L	0.324	0.476	0.013	0.019
K	0.200		0.008	

HANDLING PRECAUTIONS

PARAMETER	RATING	STANDARD
ESD – Human Body Model (HBM)	Class 1A	ESDA/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

SOLDERABILITY

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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