



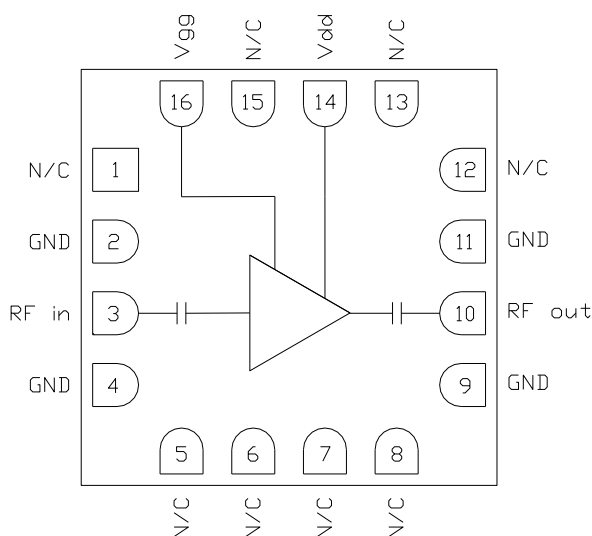
CMD319C3

8-12 GHz Ultra Low Noise Amplifier

Product Overview

The CMD319C3 is a broadband MMIC low noise amplifier housed in a leadless 3x3 mm surface mount package. The CMD319C3 is ideally suited for EW and communications systems where small size and low power consumption are needed. The device is optimized for broadband performance and delivers 20 dB of gain with a corresponding noise figure of 0.92 dB at 10 GHz. The CMD319C3 is a 50 ohm matched design which eliminates the need for external DC blocks and RF port matching.

Functional Block Diagram



Key Features

- Ultra Low Noise Figure
- High Gain Broadband Performance
- Low Power Dissipation
- Pb-Free RoHs Compliant 3x3 QFN Package

Ordering Information

Part No.	Description
CMD319C3	8-12 GHz Ultra Low Noise Amplifier, 100 Piece 7" Reel
CMD319C3-EVB	Evaluation Board

Electrical Performance ($V_{dd} = 3\text{ V}$, $V_{gg} = 1.5\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $F = 10\text{ GHz}$)

Parameter	Min	Typ	Max	Units
Frequency Range	8		12	GHz
Gain		20		dB
Noise Figure		0.92		dB
Input Return Loss		19		dB
Output Return Loss		16		dB
Output P1dB		16		dBm
Supply Current		30		mA



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Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage, V_{dd}	2	3	5	V
Gate Control Power Supply, V_{gg}	0	1.5	3	V
Drain Current, I_{dd}		30		mA
Gate Control Power Supply Current, I_{gg}		2		mA
Operating Temperature Range	-40		85	°C

Electrical performance is measured at specific test conditions. Electrical specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications ($V_{dd} = 3\text{ V}$, $V_{gg} = 1.5\text{ V}$, $T_A = 25\text{ °C}$)

Parameter	Min	Typ	Max	Units
Frequency Range	8		12	GHz
Gain @ 8 GHz	19	24		dB
Gain @ 10 GHz	19	21		dB
Gain @ 12 GHz	16	18		dB
Noise Figure @ 8.5 GHz		0.8	1.2	dB
Noise Figure @ 10.1 GHz		0.8	1.2	dB
Noise Figure @ 11.9 GHz		1.1	1.4	dB
Input Return Loss (8 to 10 GHz)		19		dB
Input Return Loss (10 to 12 GHz)		12		dB
Output Return Loss (8 to 10 GHz)		17		dB
Output Return Loss (10 to 12 GHz)		12		dB
Output P1dB		16		dBm
Output IP3		22		dBm
Supply Current	20	30	40	mA
Gain Temperature Coefficient		0.013		dB/°C
Noise Figure Temperature Coefficient		0.0066		dB/°C

Absolute Maximum Ratings

Parameter	Min Values	Max Values	Units
Drain Voltage, V_{dd}	0	5.5	V
Gate Control Power Supply Voltage, V_{gg}	0	3.3	V
RF Input Power	-	20	dBm
Power Dissipation, P_{diss}	-	921	mW
Channel Temperature (for MTTF of 1E6 hours of operation)	-	175	°C
Storage Temperature	-55	150	°C

Exceeding any one or combination of the maximum ratings may cause permanent damage to the device.

Thermal and Reliability Information

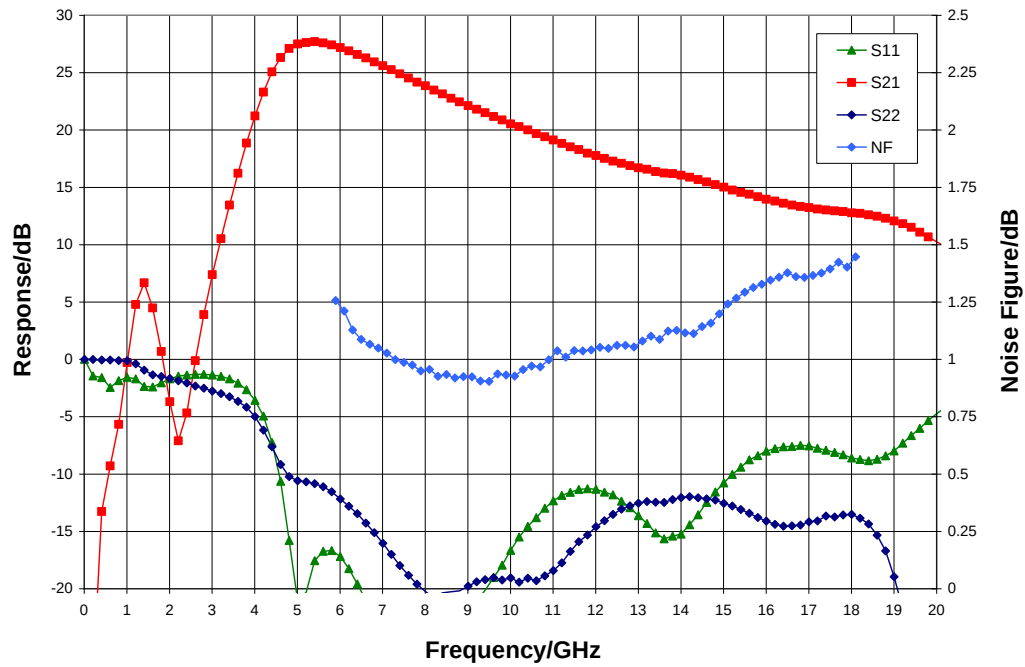
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{base} = 85^{\circ}\text{C}$, $V_D = 3.0\text{ V}$, $I_{DQ} = 30\text{ mA}$ Quiescent / Small Signal operation $P_{DISS} = 0.09\text{ W}$	70	°C/W
Channel Temperature (T_{CH})		91.3	°C
Median Lifetime (T_M)		1.28E10	Hrs

Notes:

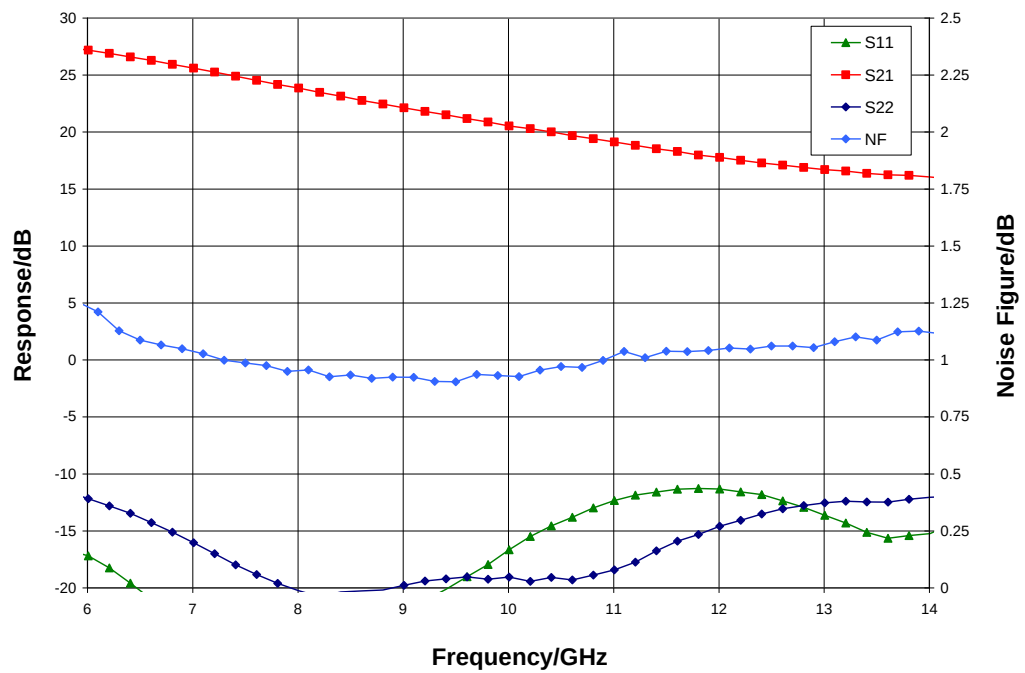
1. Thermal resistance is referenced to the bottom of the package.

Typical Performance

Broadband Performance, $V_{dd} = 3\text{ V}$, $V_{gg} = 1.5\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$

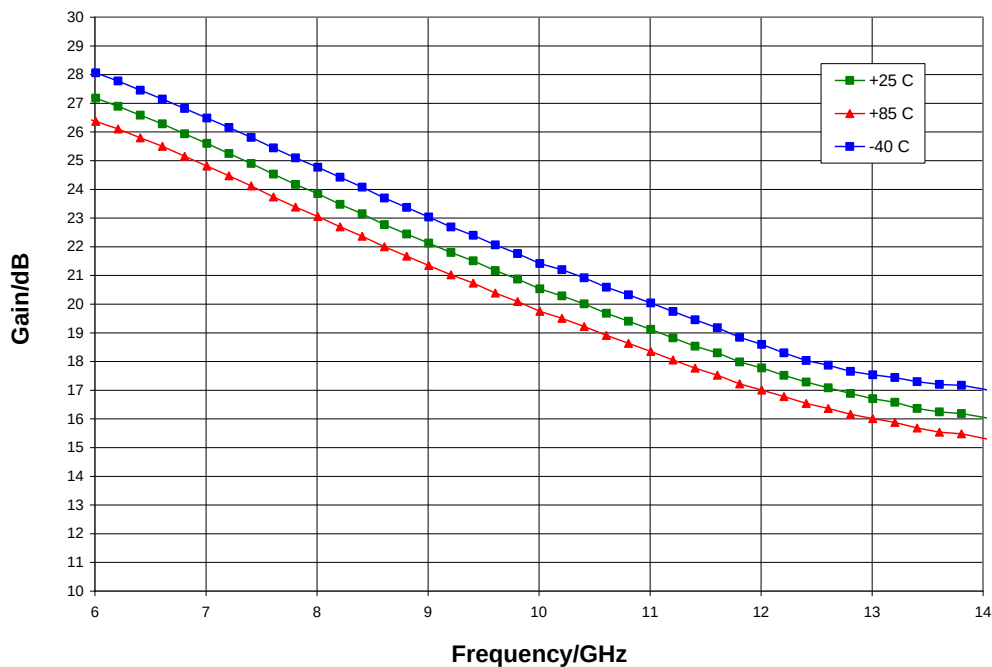


Narrow-band Performance, $V_{dd} = 3\text{ V}$, $V_{gg} = 1.5\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$

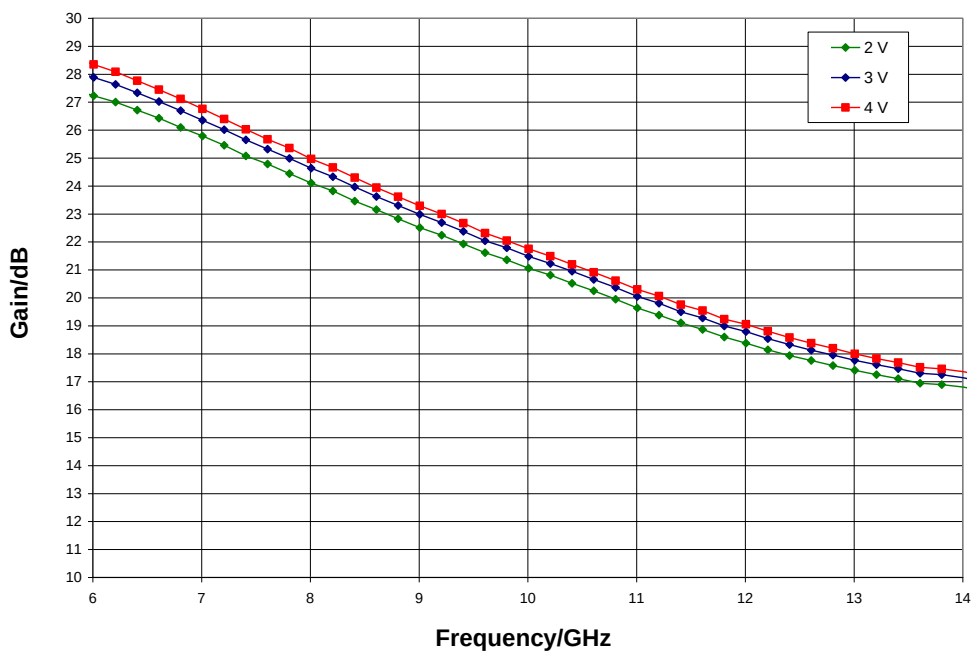


Typical Performance

Gain vs. Temperature, $V_{dd} = 3\text{ V}$, $V_{gg} = 1.5\text{ V}$

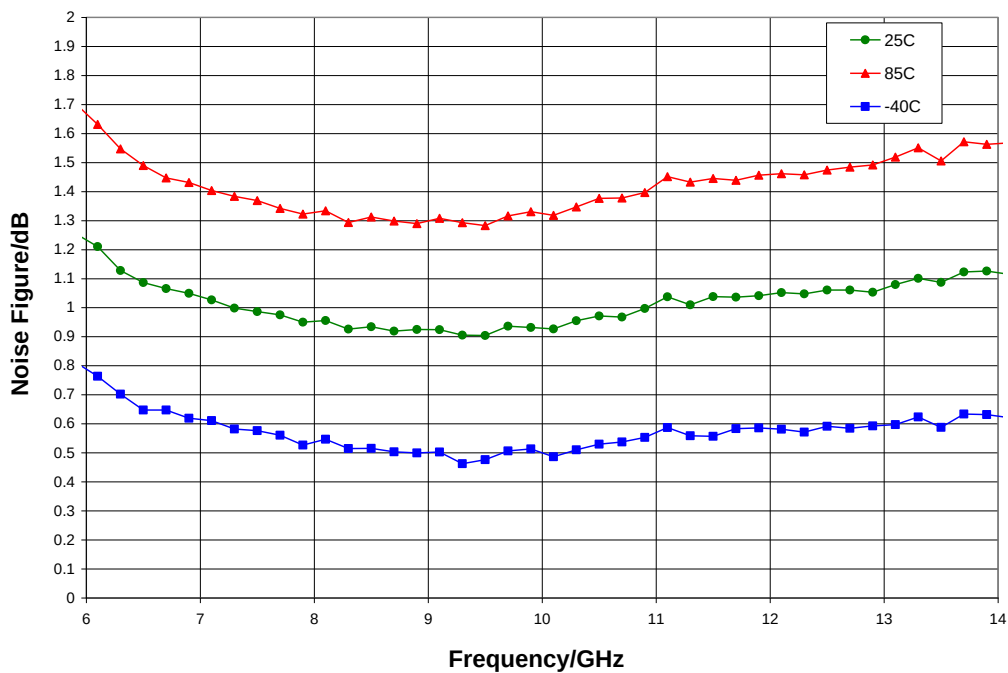


Gain vs. V_{dd} , $V_{gg} = 1.5\text{ V}$, $T_A = 25\text{ °C}$

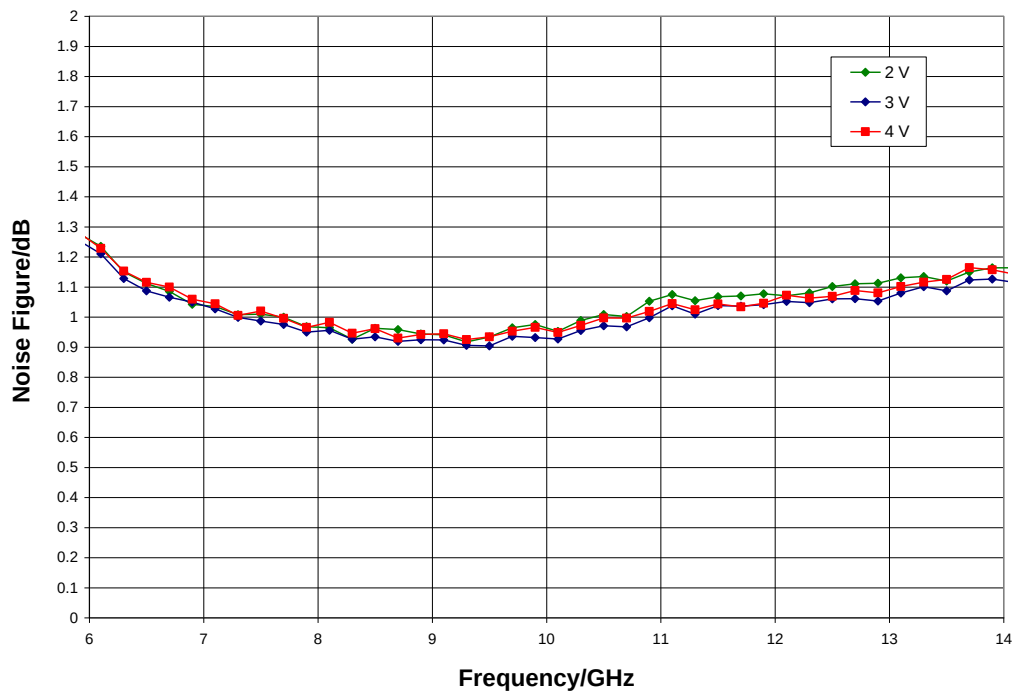


Typical Performance

Noise Figure vs. Temperature, $V_{dd} = 3\text{ V}$, $V_{gg} = 1.5\text{ V}$

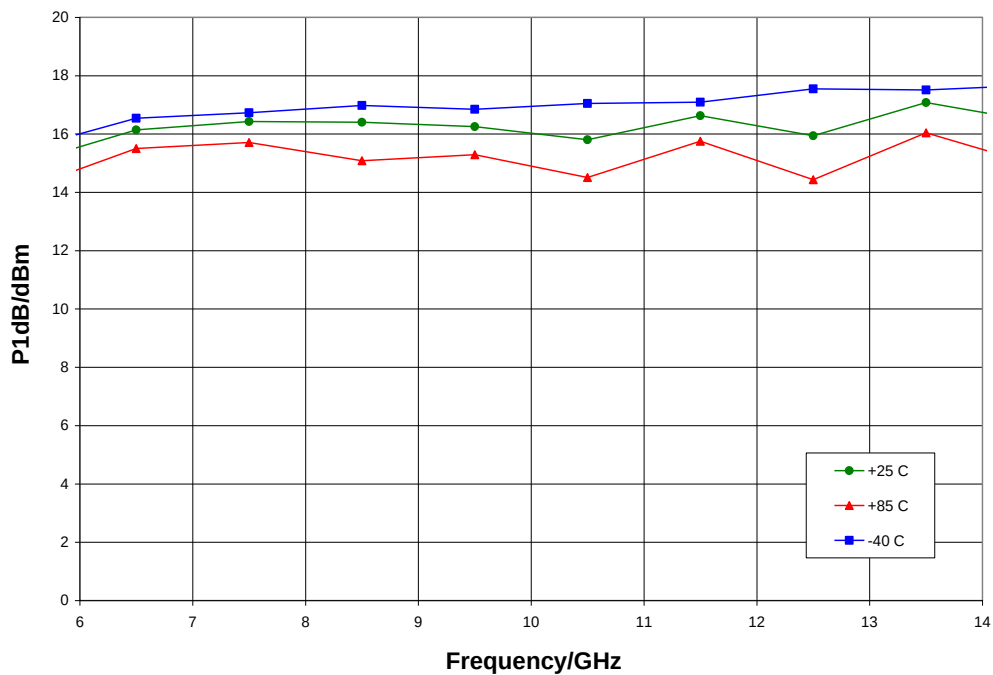


Noise Figure vs. V_{dd} , $V_{gg} = 1.5\text{ V}$, $T_A = 25\text{ °C}$

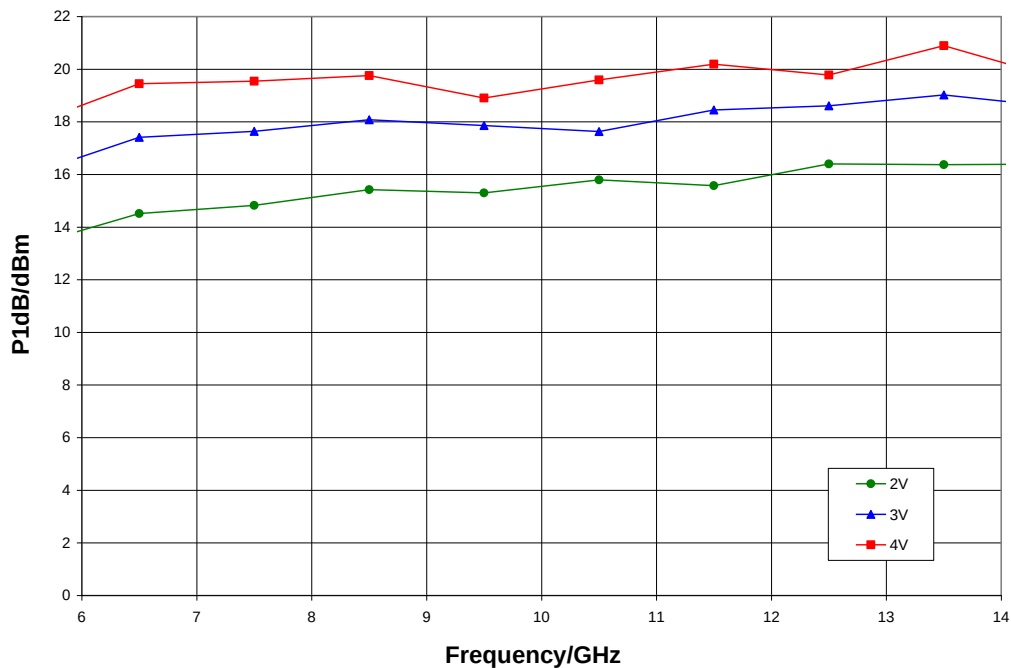


Typical Performance

P1dB vs. Temperature, $V_{dd} = 3\text{ V}$, $V_{gg} = 1.5\text{ V}$

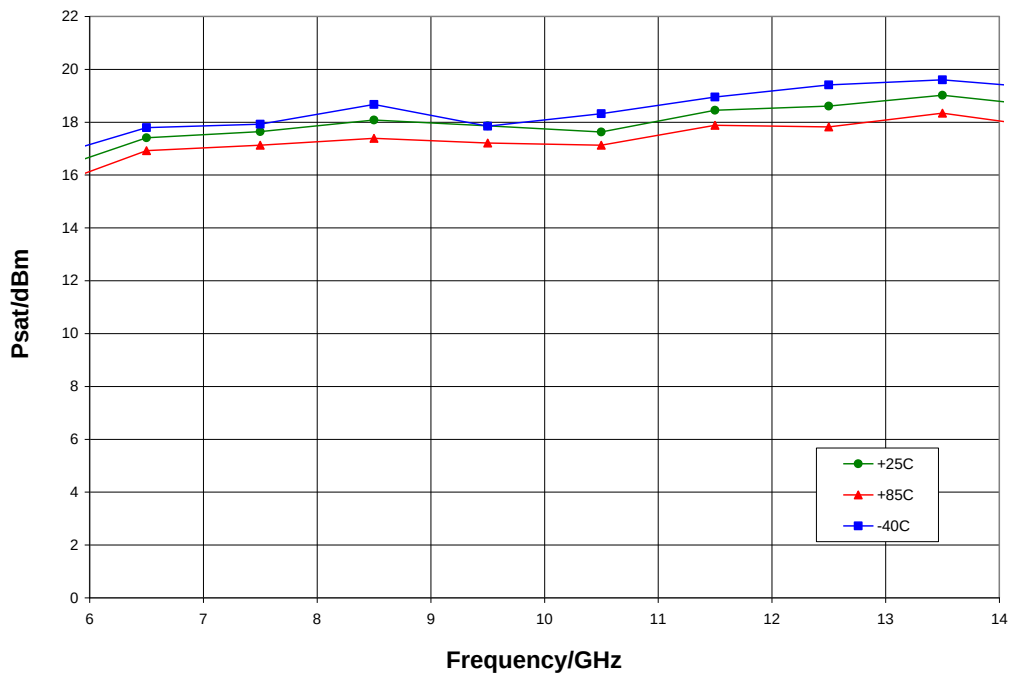


P1dB vs. V_{dd} , $V_{gg} = 1.5\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$

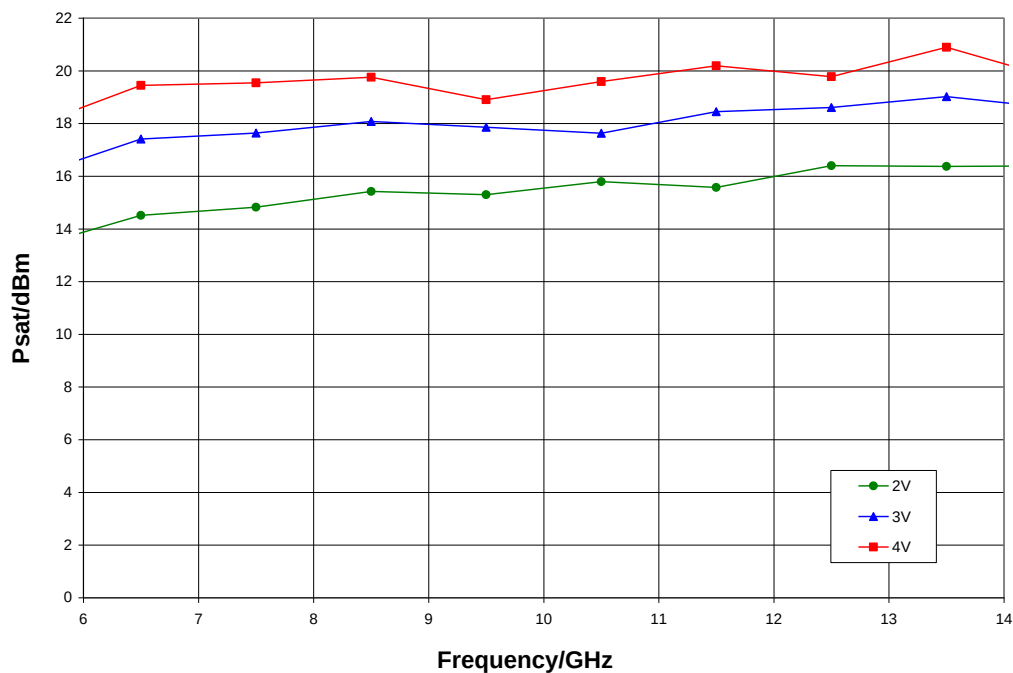


Typical Performance

Psat vs. Temperature, $V_{dd} = 3\text{ V}$, $V_{gg} = 1.5\text{ V}$

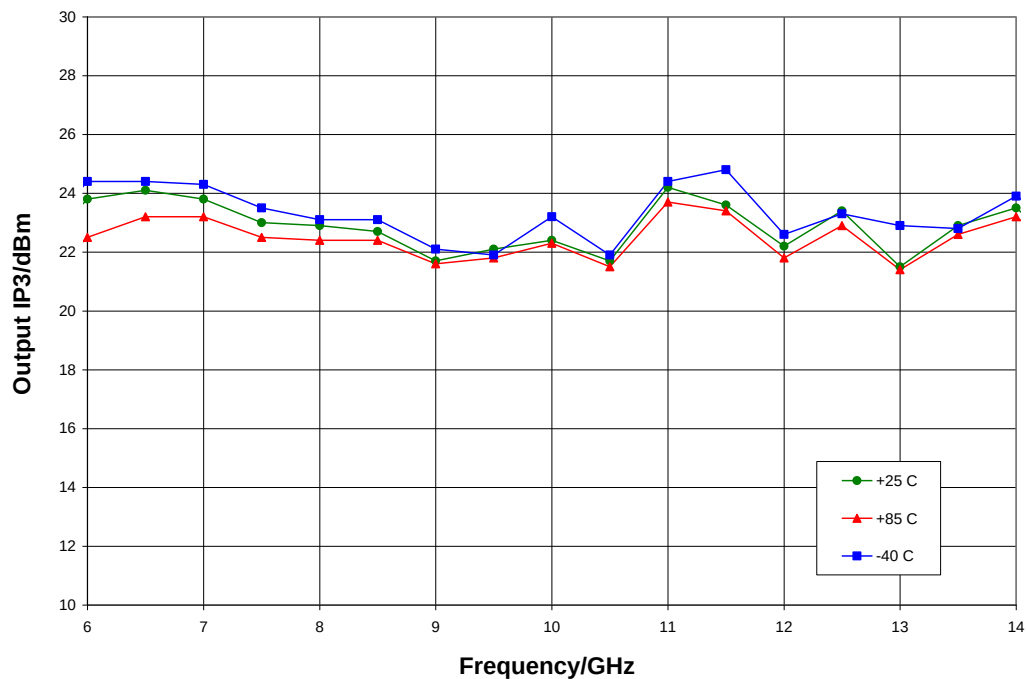


Psat vs. V_{dd} , $V_{gg} = 1.5\text{ V}$, $T_A = 25\text{ °C}$

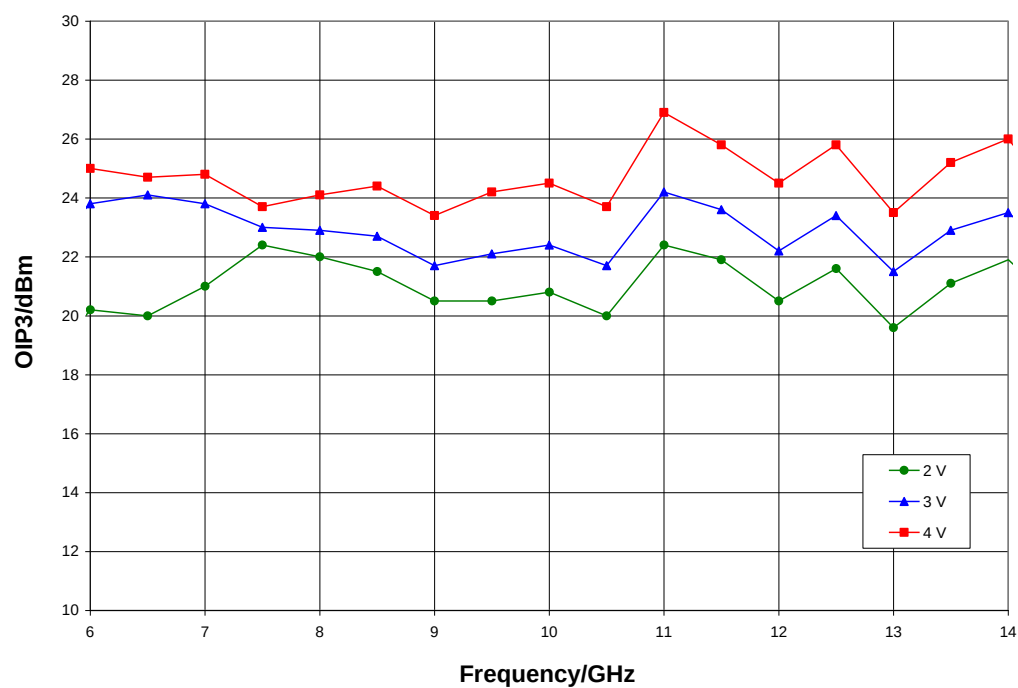


Typical Performance

Output IP3 vs. Temperature, $V_{dd} = 3\text{ V}$, $V_{gg} = 1.5\text{ V}$

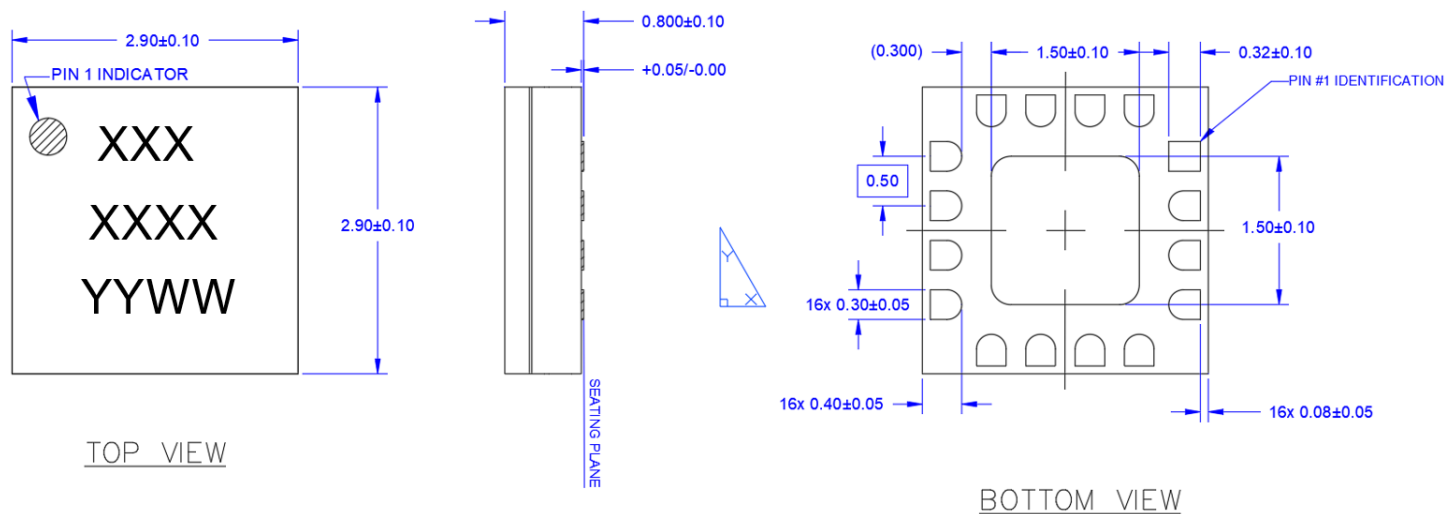


Output IP3 vs. V_{dd} , $V_{gg} = 1.5\text{ V}$, $T_A = 25\text{ °C}$



Mechanical Information

Package Information and Dimensions



Notes:

- All dimensions shown in mm.
- Material: Black alumina
- Lead finish
 - Ni: 8.89 μ m max, 1.27 μ m min
 - Pd: 0.17 μ m max, 0.07 μ m min
 - Au: 0.254 μ m max, 0.03 μ m min
- Marking
 - Line 1: Part number
 - Example: CMD319C3 shall be marked as 319
 - Line 2: Lot number
 - Line 3: Date code - Last 2 digits of the year of manufacture followed by a 2 digit week code
- Alternate pin #1 identifier is a single square pad
- Alternate die paddle may have chamfered corners

Recommended PCB Land Pattern

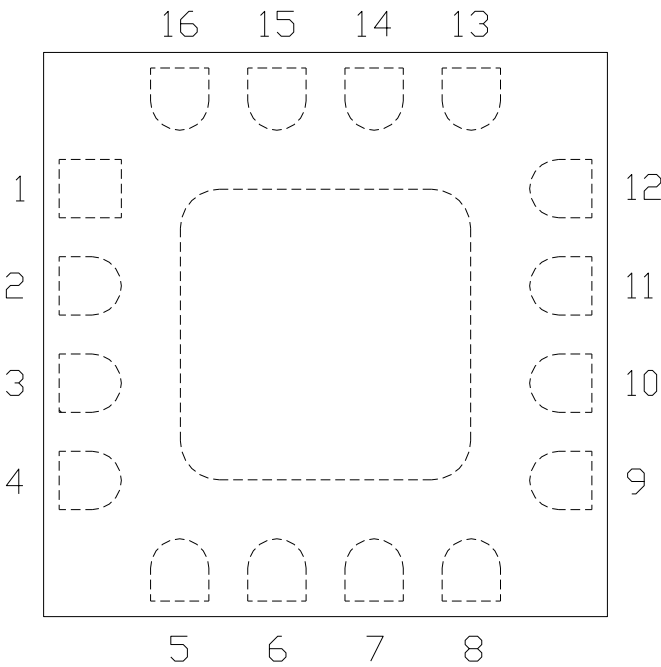
Qorvo recommends that the user develop the land pattern that will provide the best design for proper solder reflow and device attach for their specific application. Please review Qorvo Application Note AN 105 for a recommended land pattern approach.

Recommended Solder Reflow Profile

Qorvo recommends screen printing with belt furnace reflow to ensure proper solder reflow and device attach. Please review Qorvo Application Note AN 102 for a recommended solder reflow profile.

Pin Description

Pin Diagram

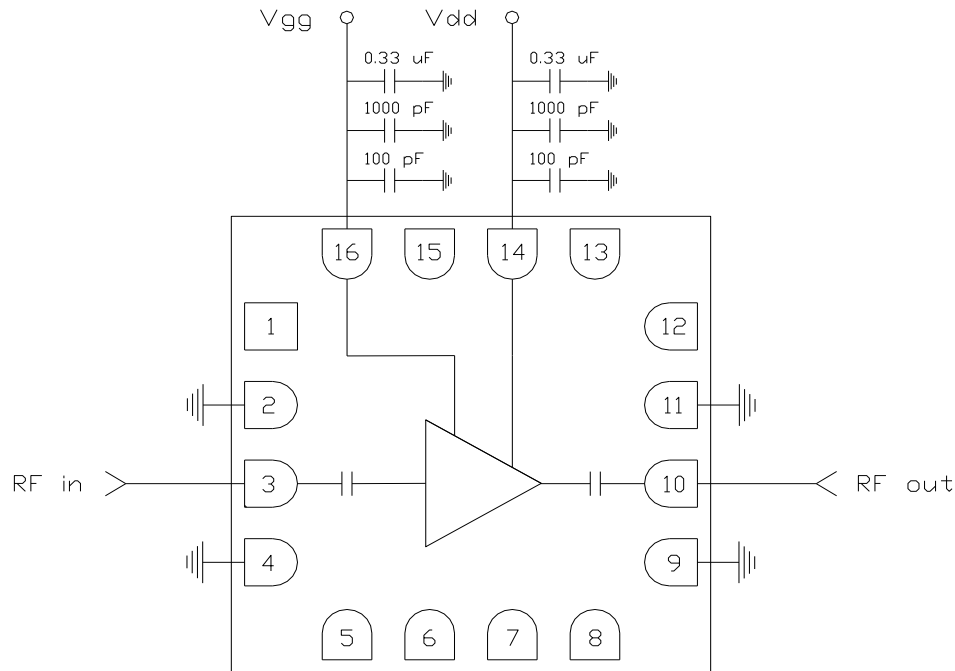


Functional Description

Pin	Function	Description	Schematic
1, 5 - 8, 12, 13, 15	N/C	No connection required These pins may be connected to RF / DC ground	
2, 4, 9, 11 and die paddle	Ground	Connect to RF / DC ground	
3	RF in	DC blocked and 50 ohm matched	
10	RF out	DC blocked and 50 ohm matched	
14	V _{dd}	Power supply voltage Decoupling and bypass caps required	
16	V _{gg}	Power supply voltage Decoupling and bypass caps required	

Applications Information

Application Circuit



Biasing and Operation

The CMD319C3 is biased with a 3 V positive drain supply and a 1.5 V positive gate supply.

Turn ON procedure:

1. Apply drain voltage V_{dd} and set to +3 V
2. Apply gate voltage V_{gg} and set to +1.5 V

Turn OFF procedure:

1. Turn off gate voltage V_{gg}
2. Turn off drain voltage V_{dd}

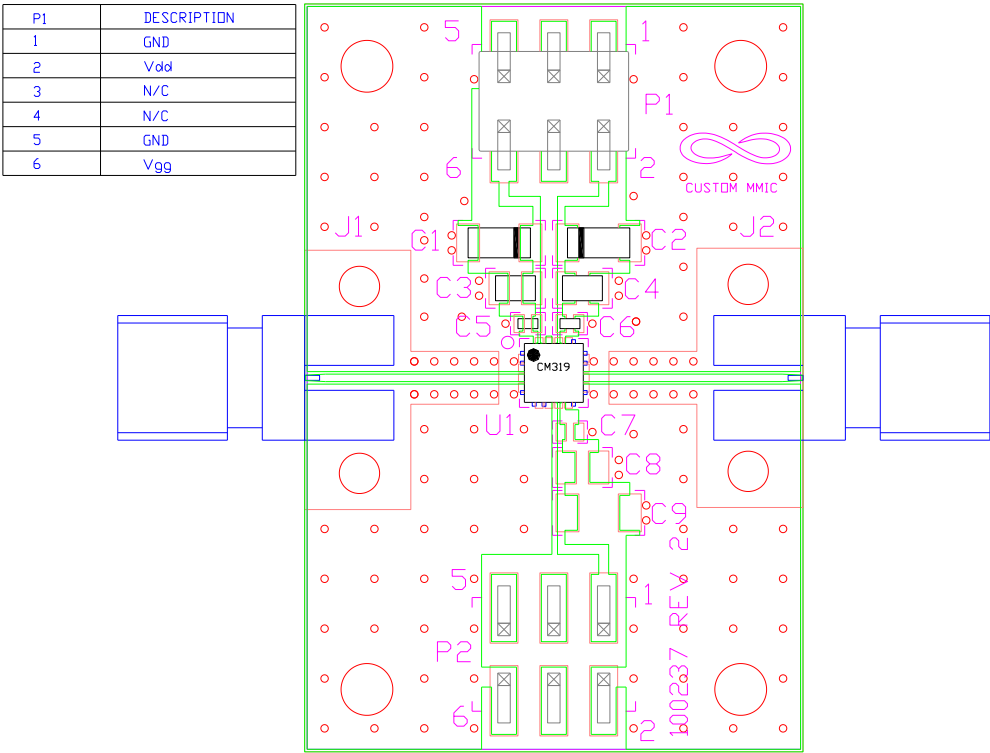
Refer to Application Note 103: Amplifier Biasing Techniques for instructions on how to implement a single supply biasing scheme.

RF power can be applied at any time

Applications Information

Evaluation Board

The circuit board shown has been developed for optimized assembly at Qorvo. A sufficient number of via holes should be used to connect the top and bottom ground planes. As surface mount processes vary, careful process development is recommended.



Designator	Value	Description
J1, J2		SMA End Launch Connector
P1		6 Pin Header
C1, C2	0.33 μ F	Capacitor, Tantalum
C3, C4	1000 pF	Capacitor, 0603
C5, C6	100 pF	Capacitor, 0402
U1		CMD319C3 Low Noise Amplifier
PCB		100237 Evaluation PCB

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C2B	ESDA / JEDEC JS-001-2012
MSL – Moisture Sensitivity Level	MSL 1	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- SVHC Free
- Halogen Free
- PFOS Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

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