



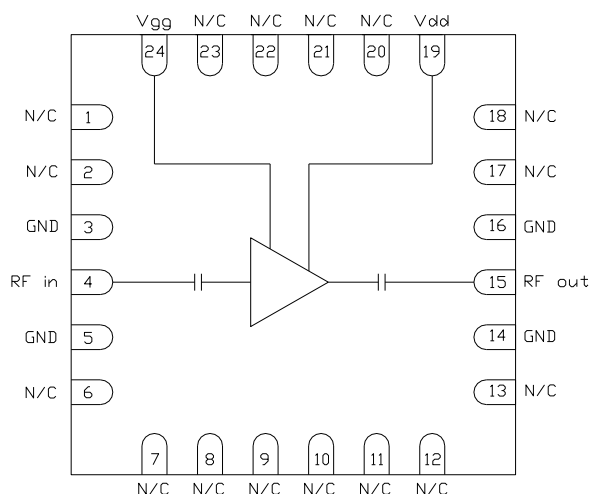
CMD299K4

18-40 GHz Low Noise Amplifier

Product Overview

The CMD299K4 is a highly efficient GaAs MMIC low noise amplifier housed in a leadless surface mount package. The amplifier is ideally suited for EW and communications systems where small size and low power consumption are needed. The device delivers greater than 16 dB of gain with a corresponding noise figure of 4 dB and output 1 dB compression point of +7 dBm at 30 GHz. The CMD299K4 is a 50 ohm matched design which eliminates the need for external DC blocks and RF port.

Functional Block Diagram



Key Features

- Low Noise Performance
- Wide Bandwidth
- All Positive Supply Voltages
- Low Current Consumption
- Pb-Free RoHS Compliant 4x4 mm SMT Package

Ordering Information

Part No.	Description
CMD299K4	100 pcs on 7" reel
CMD299K4-EVB	Evaluation Board

Electrical Performance ($V_{dd} = 3.0\text{ V}$, $V_{gg} = 3.0\text{ V}$, $T_A = 25^\circ\text{ C}$, $F = 30\text{ GHz}$)

Parameter	Min	Typ	Max	Units
Frequency Range		18 - 40		GHz
Gain		16		dB
Noise Figure		4		dB
Input Return Loss		20		dB
Output Return Loss		10		dB
Output P1dB		7		dBm
Output IP3		18		dBm
Supply Current		33		mA

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage, V_{dd}	3.5 V
Gate Voltage, V_{gg}	4.5 V
RF Input Power	+20 dBm
Channel Temperature, T_{ch}	150° C
Power Dissipation, P_{diss}	408 mW
Thermal Resistance, Q_{JC}	159.3° C/W
Operating Temperature	-40 to 85° C
Storage Temperature	-55 to 150° C

Exceeding any one or combination of the maximum ratings may cause permanent damage to the device.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{dd}	1.5	3.0	3.3	V
I_{dd}		33		mA
V_{gg}		3.0		V
I_{gg}		2.3		mA

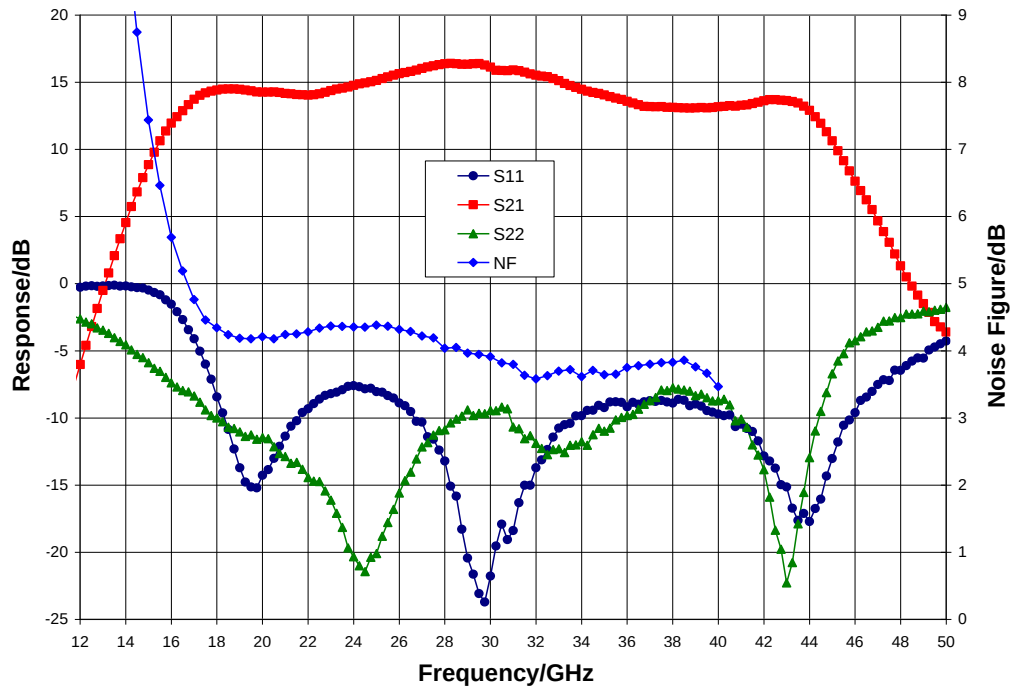
Electrical performance is measured at specific test conditions.
 Electrical specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications ($V_{dd} = 3.0$ V, $V_{gg} = 3.0$ V, $T_A = 25$ °C)

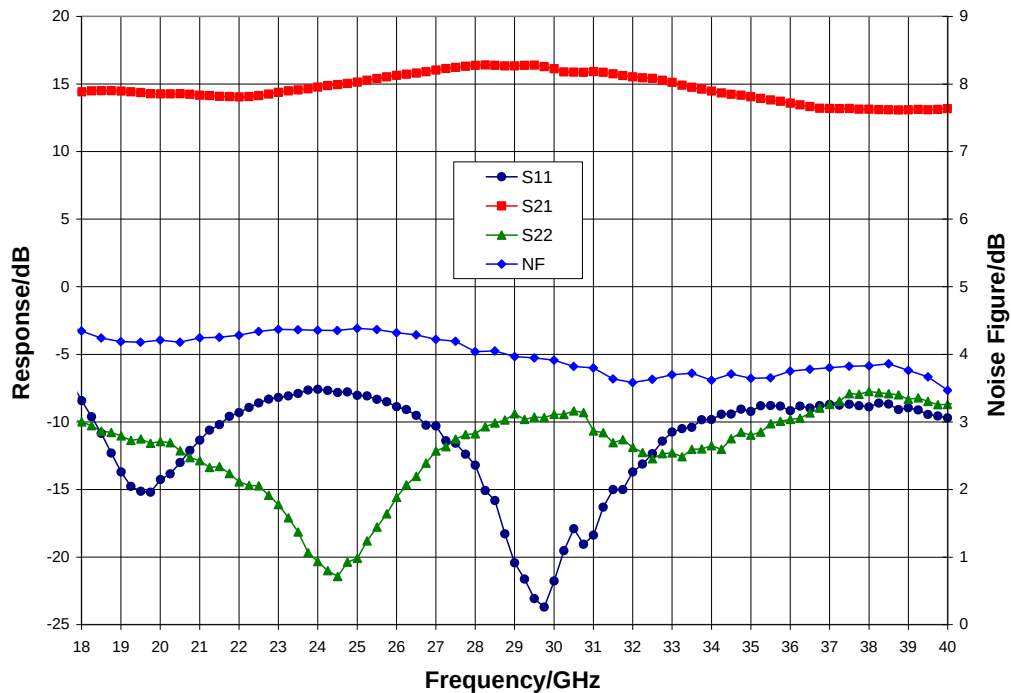
Parameter	Min	Typ	Max	Min	Typ	Max	Units
Frequency Range	18 - 30			30 - 40			GHz
Gain	11	15		10	14		dB
Noise Figure		4.2	4.9		3.7	4.4	dB
Input Return Loss		10			10		dB
Output Return Loss		13			10		dB
Output P1dB		6			6.5		dBm
Output IP3		15			17		dBm
Supply Current	23	33	43	23	33	43	mA
Gain Temperature Coefficient		0.017			0.02		dB/°C
Noise Figure Temperature Coefficient		0.015			0.014		dB/°C

Typical Performance

Broadband Performance, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 3.0\text{ V}$, $I_{dd} = 33\text{ mA}$, $T_A = 25^\circ\text{C}$

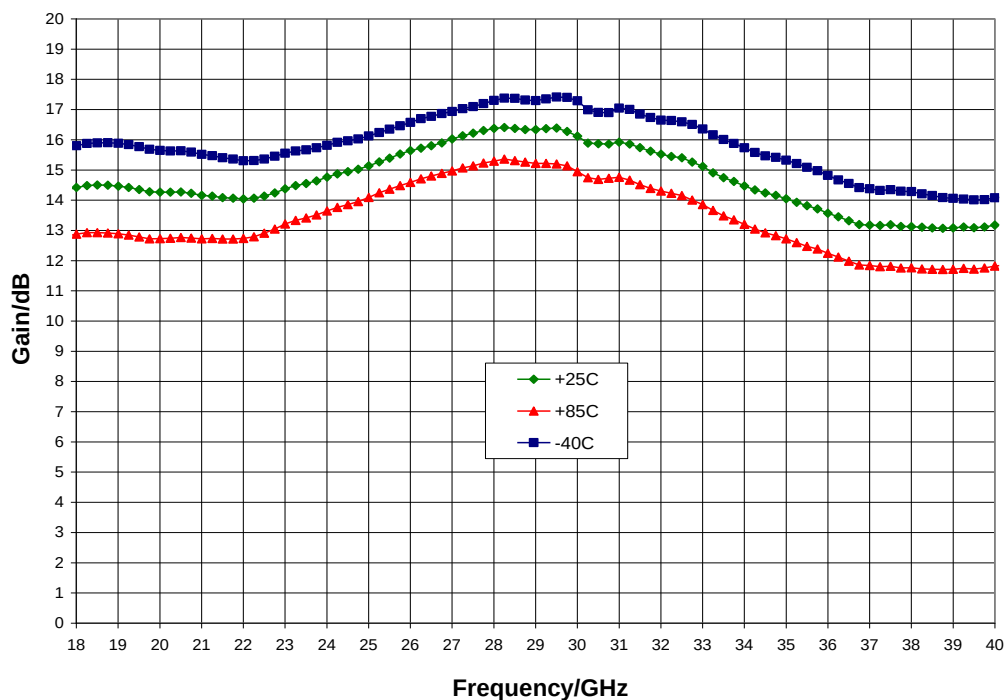


Narrow-band Performance, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 3.0\text{ V}$, $I_{dd} = 33\text{ mA}$, $T_A = 25^\circ\text{C}$

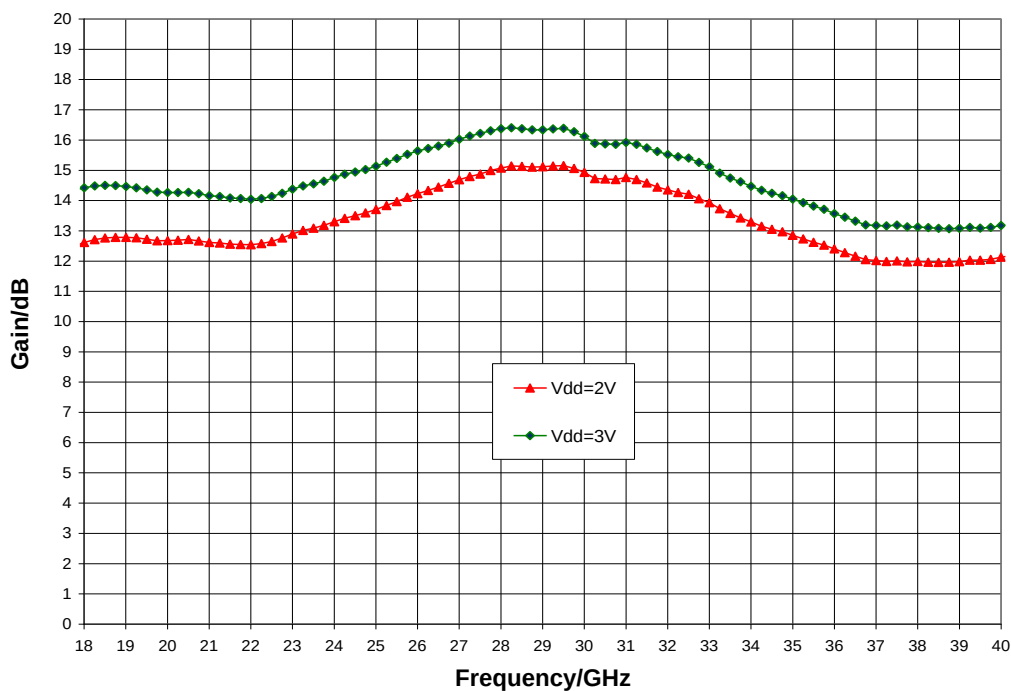


Typical Performance

Gain vs. Temperature, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 3.0\text{ V}$

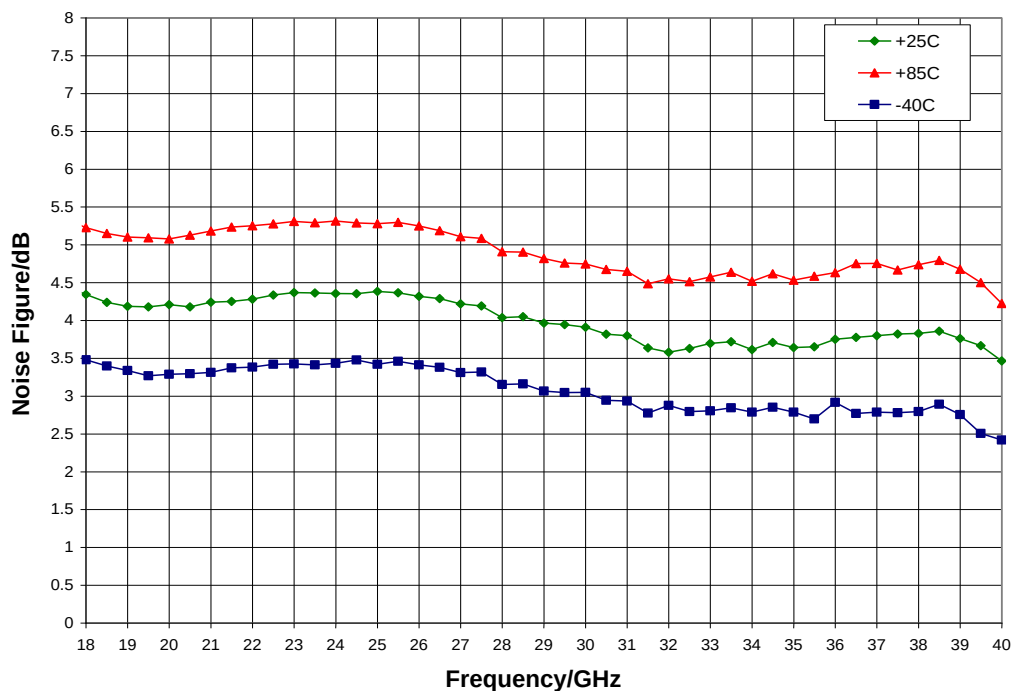


Gain vs. V_{dd} , $T_A = 25^\circ\text{C}$

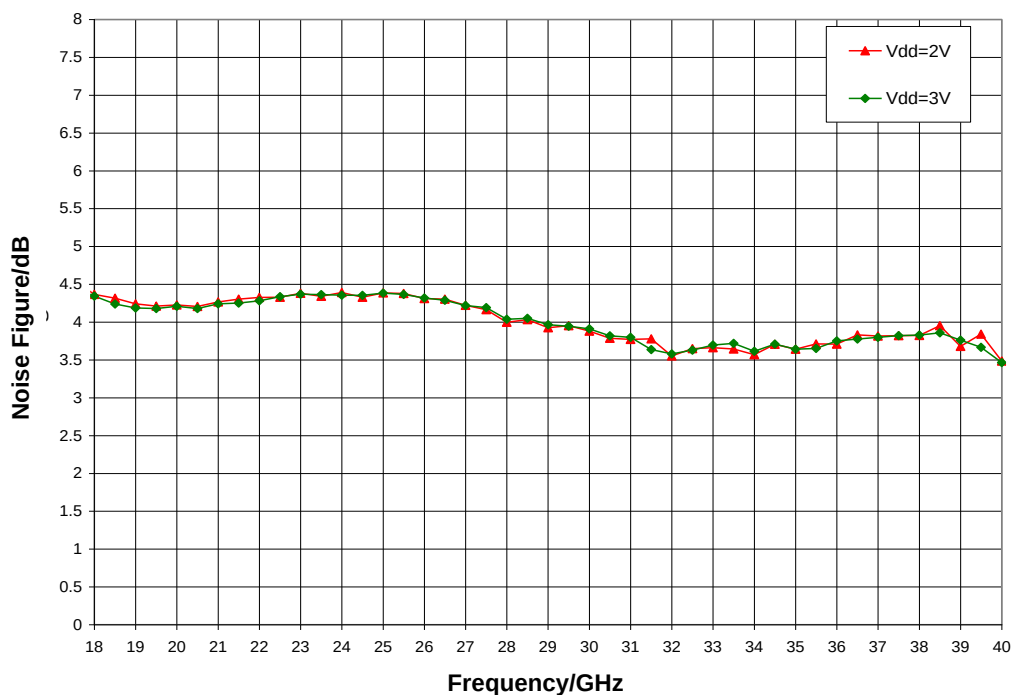


Typical Performance

Noise Figure vs. Temperature, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 3.0\text{ V}$

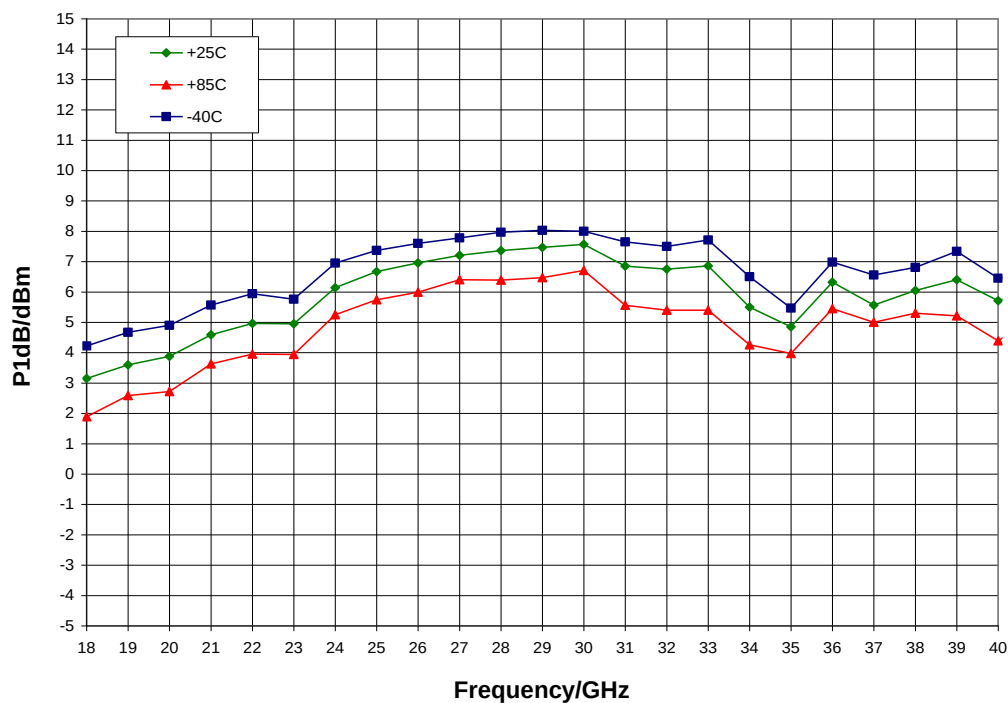


Noise Figure vs. V_{dd} , $T_A = 25^\circ\text{C}$

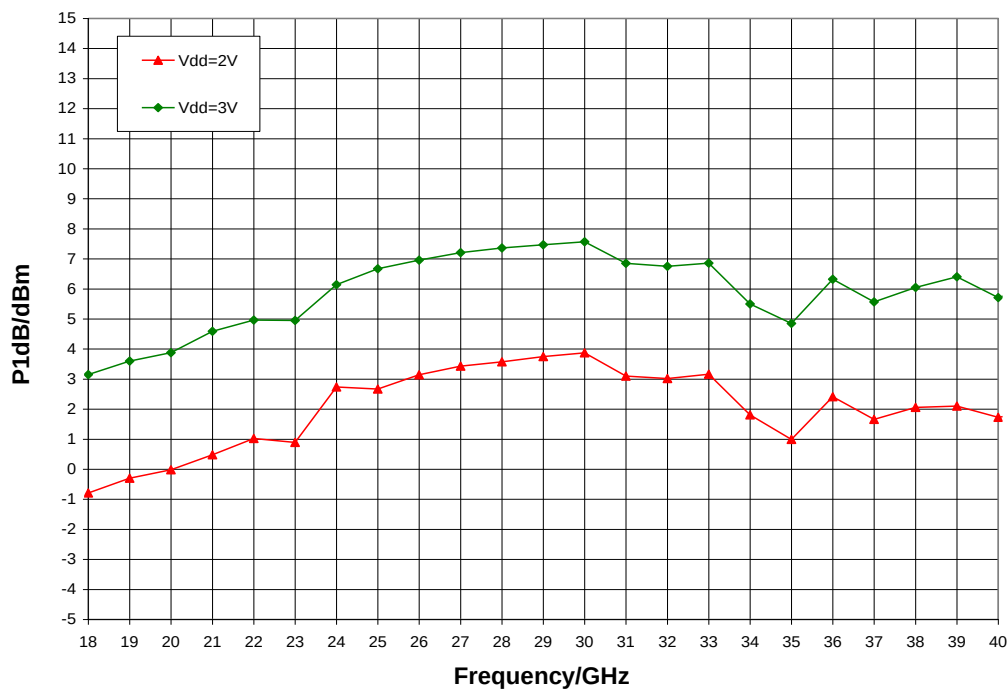


Typical Performance

P1dB vs. Temperature, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 3.0\text{ V}$

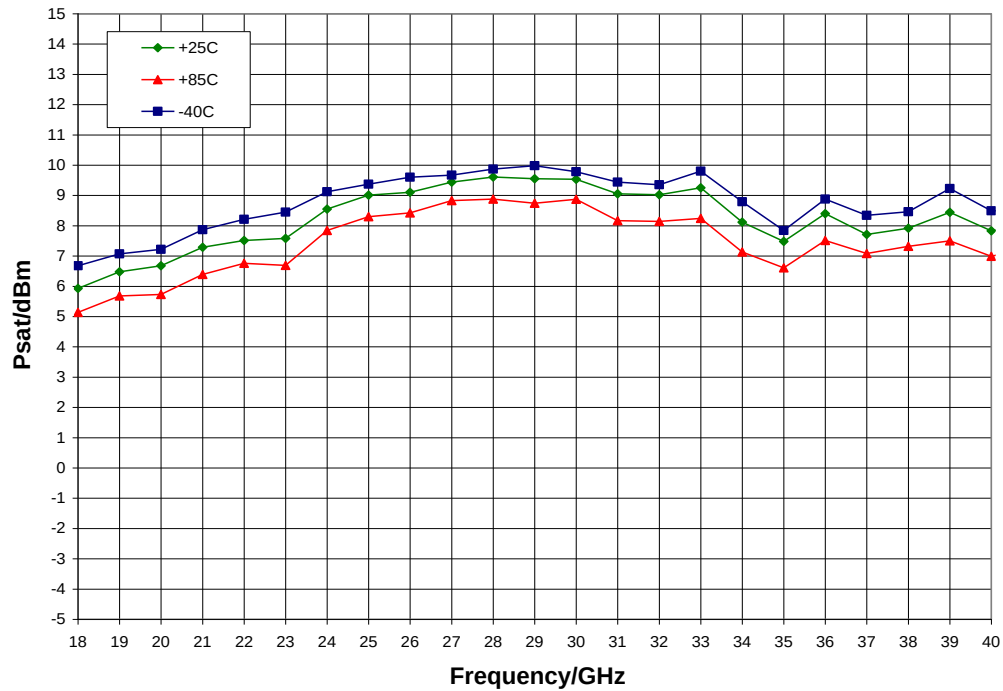


P1dB vs. V_{dd} , $T_A = 25^\circ\text{C}$

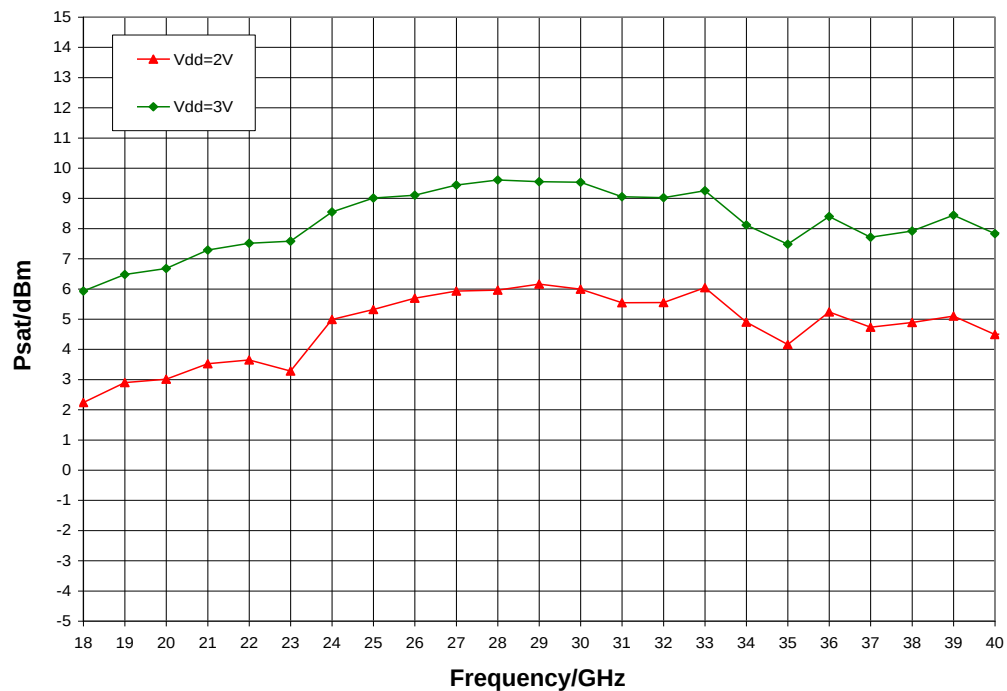


Typical Performance

Psat vs. Temperature, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 3.0\text{ V}$

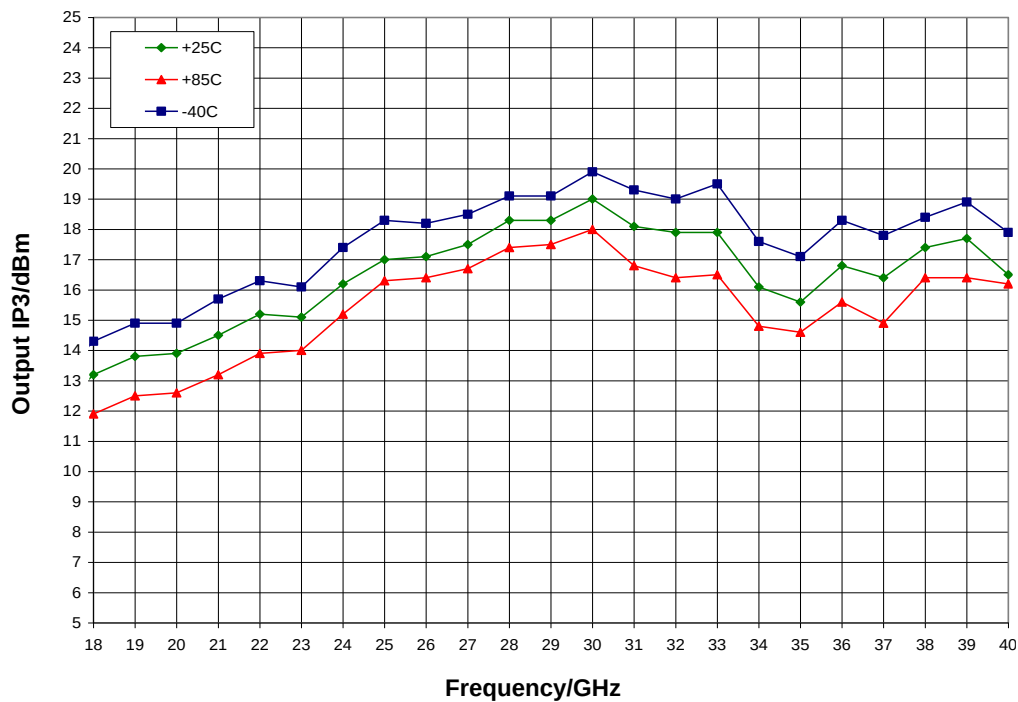


Psat vs. V_{dd} , $T_A = 25^\circ\text{C}$

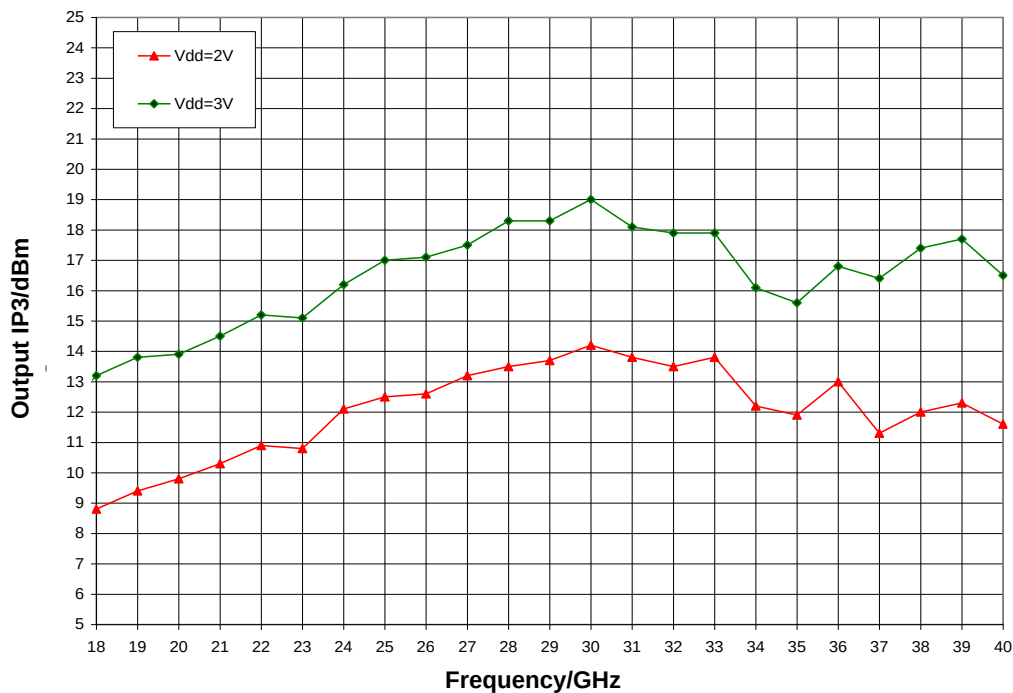


Typical Performance

Output IP3 vs. Temperature, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 3.0\text{ V}$

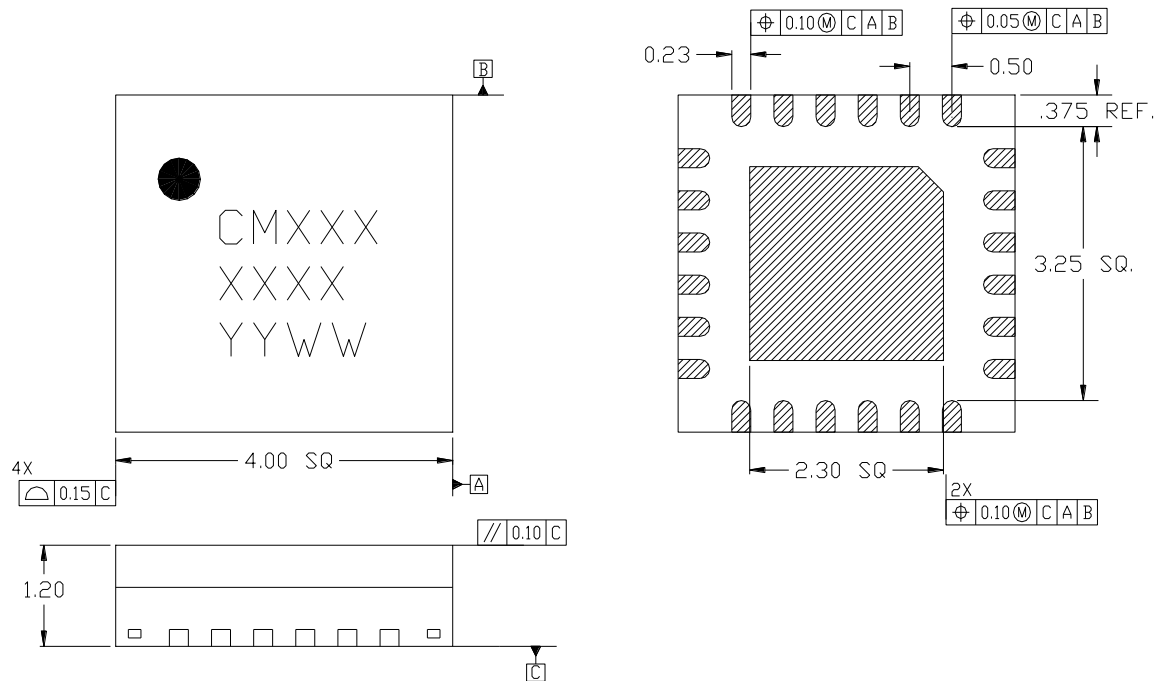


Output IP3 vs. V_{dd} , $T_A = 25^\circ\text{C}$



Mechanical Information

Package Information and Dimensions



Notes:

1. All dimensions shown in mm.
2. Material: RoHS compliant mold compound
3. Lead finish: Electroless Ni, electroless Pd, immersion Au (ENEPIG) per IPC - 4556
4. Marking
 - 4.1. Line 1: Part number
 - 4.1.1. Example: CMD162K4 shall be marked as CM162
 - 4.2. Line 2: Lot number
 - 4.3. Line 3: Date code - Last 2 digits of the year of manufacture followed by a 2 digit week code
5. Alternate pin #1 identifier is a single square pad
6. Alternate die paddle may have chamfered corners

Recommended PCB Land Pattern

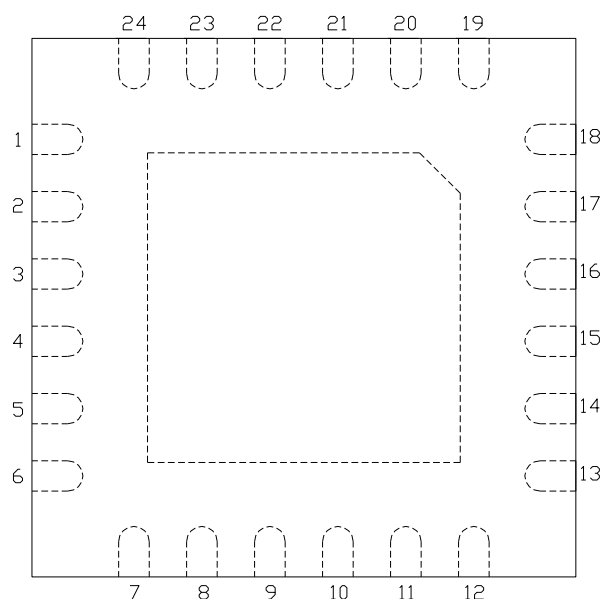
Qorvo recommends that the user develop the land pattern that will provide the best design for proper solder reflow and device attach for their specific application. Please review Qorvo Application Note AN 105 for a recommended land pattern approach.

Recommended Solder Reflow Profile

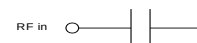
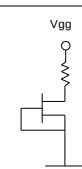
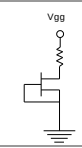
Qorvo recommends screen printing with belt furnace reflow to ensure proper solder reflow and device attach. Please review Qorvo Application Note AN 102 for a recommended solder reflow profile.

Pin Description

Pin Diagram

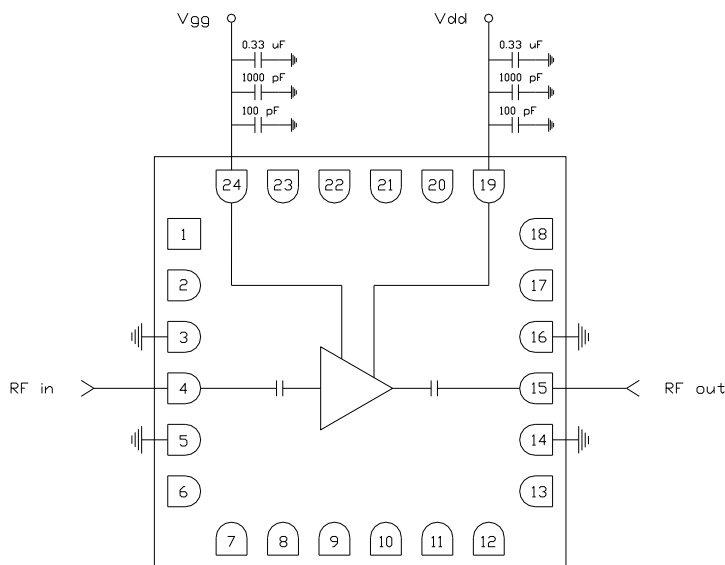


Functional Description

Pin	Function	Description	Schematic
1, 2, 6 - 13, 17, 18, 20 - 23	N/C	No connection required These pins may be connected to RF / DC ground	
3, 5, 14, 16 and die paddle	Ground	Connect to RF / DC ground	
4	RF in	DC blocked and 50 ohm matched	
15	RF out	DC blocked and 50 ohm matched	
19	V _{dd}	Power supply voltage Decoupling and bypass caps required	
24	V _{gg}	Power supply voltage Decoupling and bypass caps required	

Applications Information

Application Circuit



Biasing and Operation

The CMD299K4 is biased with a positive drain supply and positive gate supply. Performance is optimized when the drain voltage is set to +3.0 V, though it may be set to a minimum of +2.0 V and a maximum of +3.3 V. The recommended gate voltage is +3.0 V.

Turn ON procedure:

1. Apply drain voltage V_{dd} and set to +3 V
2. Apply gate voltage V_{gg} and set to +3 V

Turn OFF procedure:

1. Turn off gate voltage V_{gg}
2. Turn off drain voltage V_{dd}

The preferred biasing procedure has been proven to be robust and should be used whenever possible. However, the CMD299K4 does allow for simultaneous biasing (applying V_{dd} and V_{gg} at the same time).

Refer to Application Note 103: Amplifier Biasing Techniques for instructions.

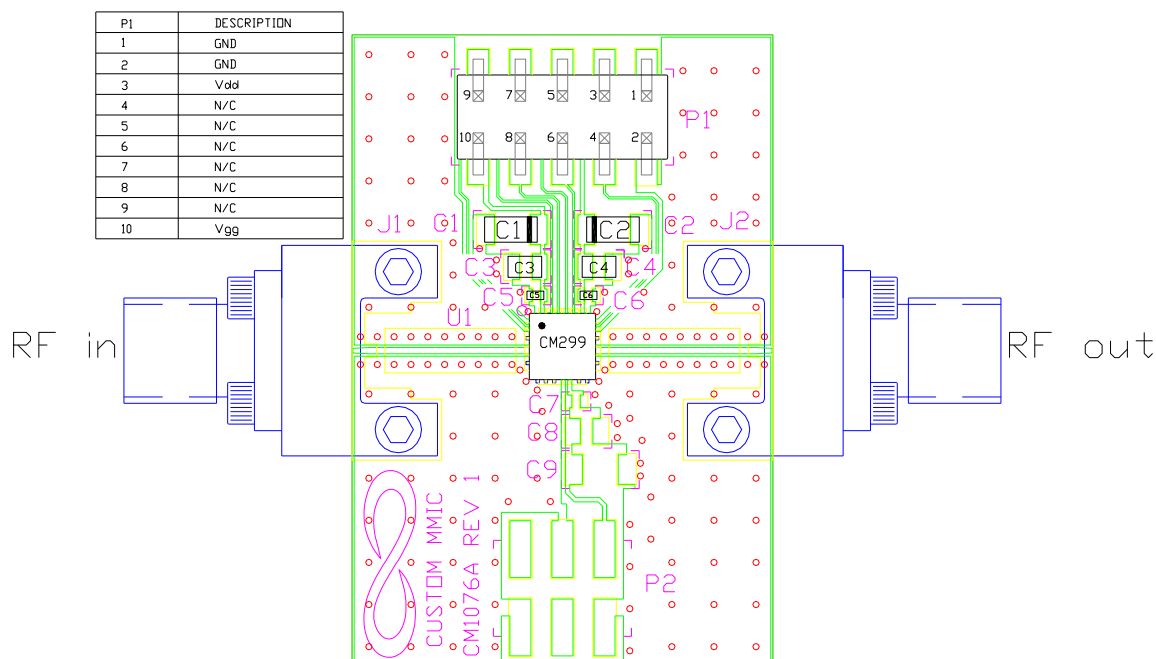
For either approach, RF power can be applied at any time.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Applications Information

Evaluation Board

The circuit board shown has been developed for optimized assembly at Qorvo. A sufficient number of via holes should be used to connect the top and bottom ground planes. As surface mount processes vary, careful process development is recommended.



Bill of Material

Designator	Value	Description
J1, J2		2.4 mm End Launch Connector
P1		10 Pin Header
C1, C2	0.33 μ F	Capacitor, Tantalum
C3, C4	1000 pF	Capacitor, 0603
C5, C6	100 pF	Capacitor, 0402
U1		CMD299K4 Low Noise Amplifier
PCB		102532 Evaluation PCB

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA / JEDEC JS-001-2012
MSL – Moisture Sensitivity Level	Level 3	JEDEC standard IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- SVHC Free
- PFOS Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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