MOSFETs Silicon N-channel MOS (U-MOSⅧ-H)

TPH1110FNH

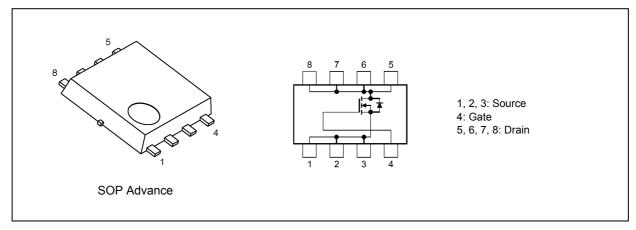
1. Applications

- High-Efficiency DC-DC Converters
- Switching Voltage Regulators

2. Features

- (1) High-speed switching
- (2) Small gate charge: $Q_{SW} = 4.2 \text{ nC}$ (typ.)
- (3) Low drain-source on-resistance: $R_{DS(ON)} = 95 \text{ m}\Omega \text{ (typ.)} (V_{GS} = 10 \text{ V})$
- (4) Low leakage current: $I_{DSS} = 10 \ \mu A \ (max) \ (V_{DS} = 250 \ V)$
- (5) Enhancement mode: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_{D} = 0.3 mA)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (T_a = 25 °C unless otherwise specified)

Characteris	Symbol	Rating	Unit		
Drain-source voltage			V _{DSS}	250	V
Gate-source voltage			V _{GSS}	±20	7
Drain current (DC)	(Silicon limit)	(Note 1), (Note 2)	I _D	15	Α
Drain current (DC)	(Continuous)	(Note 1)	I _D	10	7
Drain current (pulsed)	(t = 1 ms)	(Note 1)	I _{DP}	32	7
Power dissipation	(T _c = 25 °C)		PD	57	W
Power dissipation	(t = 10 s)	(Note 3)	PD	2.8	1
Power dissipation	(t = 10 s)	(Note 4)	PD	1.6	7
Single-pulse avalanche energy	·	(Note 5)	E _{AS}	58	mJ
Avalanche current			I _{AR}	10	Α
Channel temperature			T _{ch}	150	°C
Storage temperature			T _{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit		
Channel-to-case thermal resistance	(T _c = 25 °C)		R _{th(ch-c)}	2.19	°C/W
Channel-to-ambient thermal resistance	(t = 10 s)	(Note 3)	R _{th(ch-a)}	44.6	
Channel-to-ambient thermal resistance	(t = 10 s)	(Note 4)	R _{th(ch-a)}	78.1	

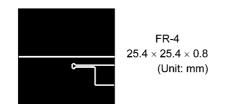
Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Limited by silicon chip capability.

Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 5: V_DD = 60 V, T_ch = 25 °C (initial), L = 0.95 mH, I_{AR} = 10 A



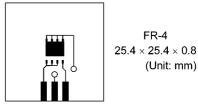


Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a) Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

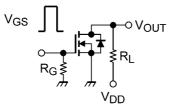
6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I _{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	_	—	±0.1	μA
Drain cut-off current	I _{DSS}	V _{DS} = 250 V, V _{GS} = 0 V	_	—	10	
Drain-source breakdown voltage	V _{(BR)DSS}	I _D = 10 mA, V _{GS} = 0 V	250	—	_	V
	V _{(BR)DSX}	I _D = 10 mA, V _{GS} = -20 V	175	—	_	
Gate threshold voltage	V _{th}	V _{DS} = 10 V, I _D = 0.3 mA	2.0	—	4.0	
Drain-source on-resistance	R _{DS(ON)}	V _{GS} = 10 V, I _D = 5 A		95	112	mΩ

6.2. Dynamic Characteristics ($T_a = 25$ °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C _{iss}	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	_	810	1100	pF
Reverse transfer capacitance	C _{rss}		_	3	50	
Output capacitance	C _{oss}			75	_	
Gate resistance	rg	—		2.8	4.2	Ω
Switching time (rise time)	t _r	See Fig. 6.2.1		6.5	_	ns
Switching time (turn-on time)	t _{on}			17	_	
Switching time (fall time)	t _f			4.8	_	
Switching time (turn-off time)	t _{off}		_	20	_	



$$\begin{split} V_{DD} &\approx 100 \text{ V} \\ V_{GS} &= 0 \text{ V}/10 \text{ V} \\ I_D &= 5.0 \text{ A} \\ R_L &= 20 \ \Omega \\ R_G &= 4.7 \ \Omega \\ Duty &\leq 1 \ \%, \ t_w = 10 \ \mu s \end{split}$$

Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics ($T_a = 25$ °C unless otherwise specified)

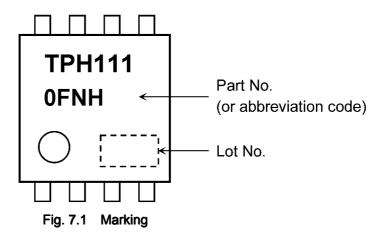
Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Qg	$V_{DD} \approx 100 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	_	11	—	nC
Gate-source charge 1	Q _{gs1}		_	3.8	_	nC
Gate-drain charge	Q _{gd}		_	2.8	_	
Gate switch charge	Q _{SW}			4.2	_	

6.4. Source-Drain Characteristics ($T_a = 25$ °C unless otherwise specified)

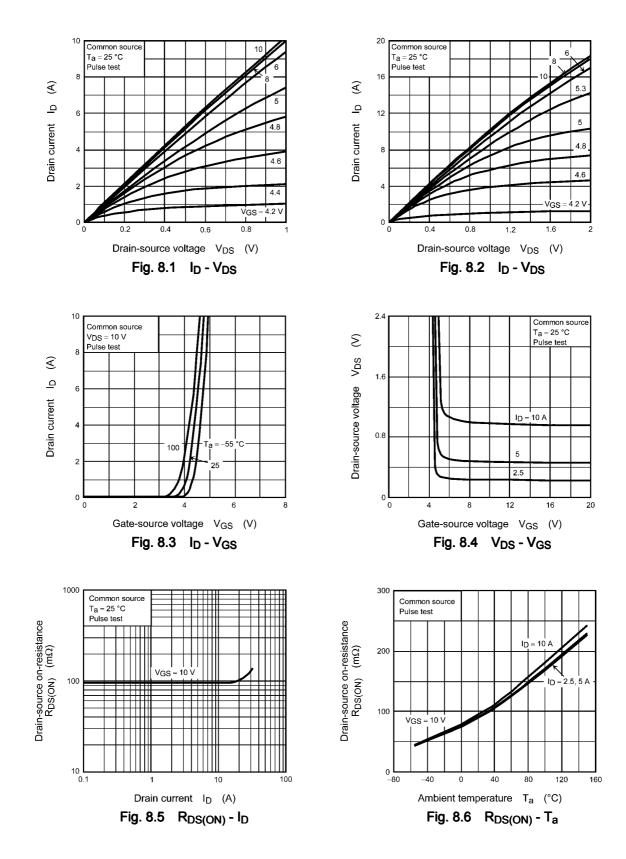
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Reverse drain current (pulsed)	(Note 6)	I _{DRP}	—	_	—	32	А
Diode forward voltage		V _{DSF}	I _{DR} = 10 A, V _{GS} = 0 V	_		-1.2	V

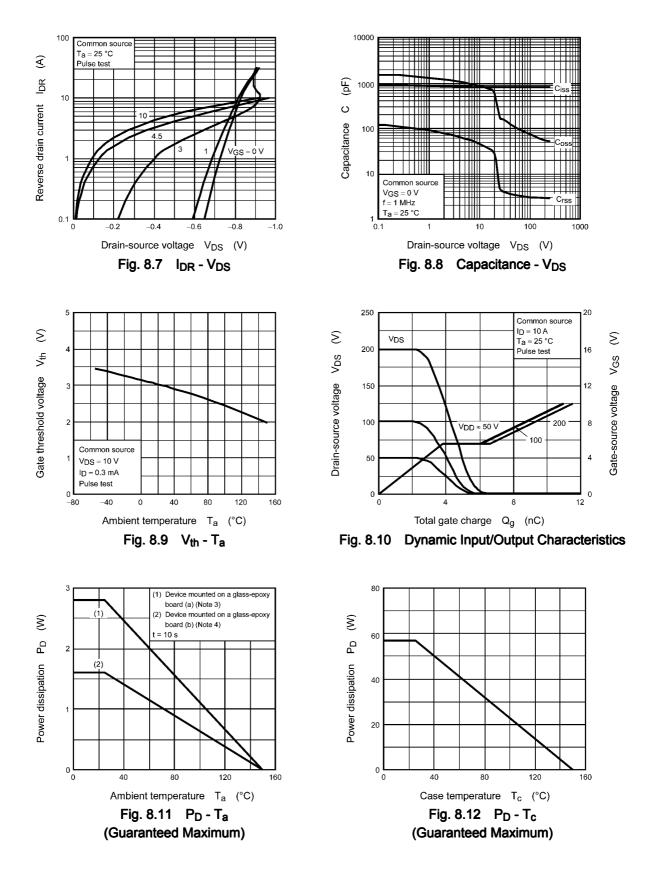
Note 6: Ensure that the channel temperature does not exceed 150 °C.

7. Marking



8. Characteristics Curves (Note)





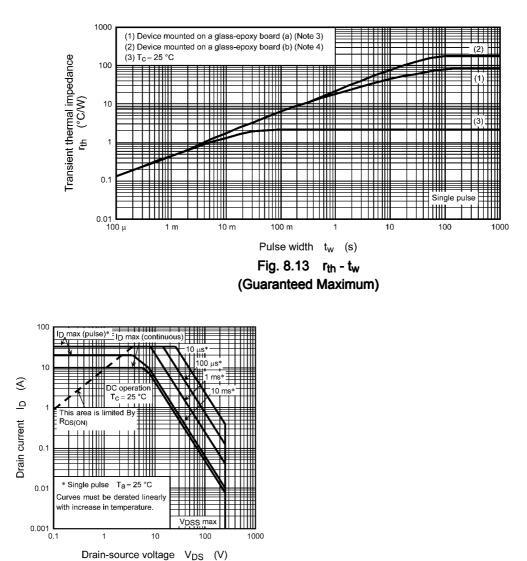


Fig. 8.14 Safe Operating Area (Guaranteed Maximum)

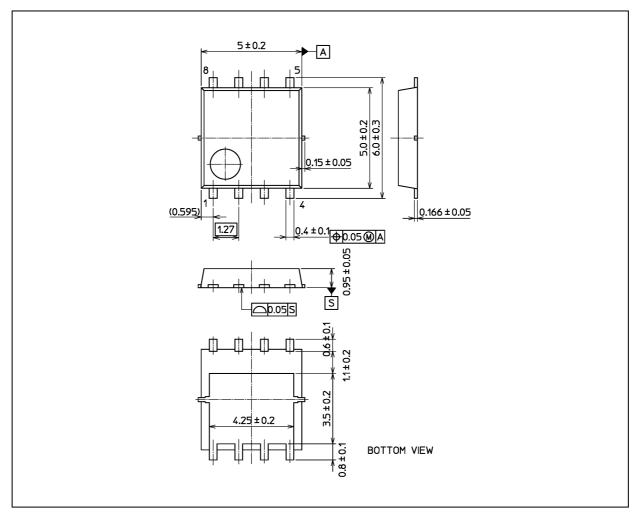
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



TPH1110FNH

Package Dimensions

Unit: mm



Weight: 0.069 g (typ.)

TOSHIBA: 2-5Q1S

Nickname: SOP Advance

Package Name(s)

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