

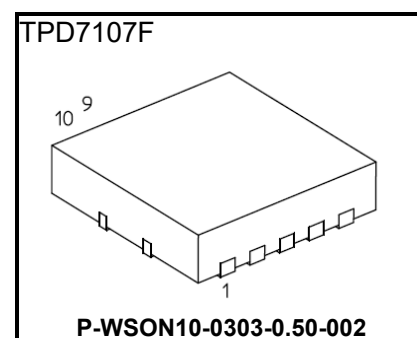
TOSHIBA Intelligent Power Device Silicon Power MOS Integrated Circuit

# TPD7107F

1 channel High-Side N channel Power MOSFET Gate Driver

## 1. Description

TPD7107F is a 1channel high-side N channel power MOSFET gate driver. This IC contains a charge pump circuit, allowing easy configuration of a high-side switch for large-current applications.



## 2. Uses

- Junction Boxes for Automotive.
- Power distribution modules for Automotive.
- Semiconductor relays.

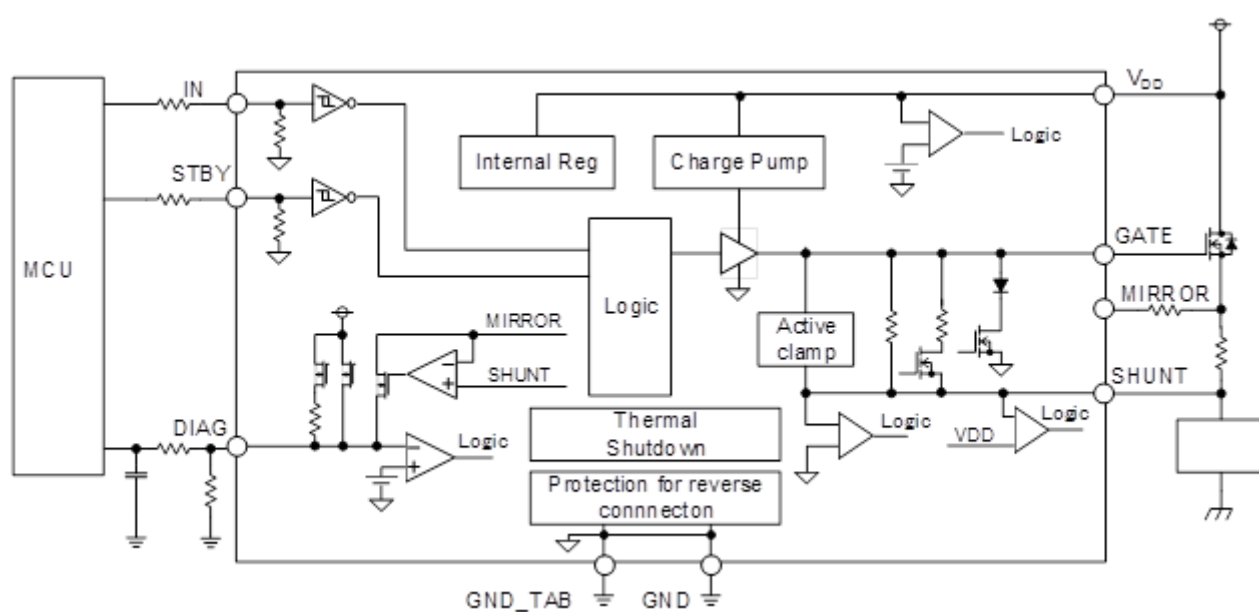
## 3. Features

- AEC-Q100 qualified.
- Built in the charge pump circuit.
- Built in the various protection feature and diagnostic output function.
  - The abnormalities in power supply voltage (a voltage fall, excess voltage, reverse connection of power supply)
  - Current sense of load line.
  - Over current (short circuit of load line)
  - Overheating
  - The abnormalities in Drain-source voltage of external FET
  - Active clamp of external FET
  - Protection for disconnection of GND terminal.
  - $V_{DD}$  short of load line (Short circuit between source of external FET and  $V_{DD}$ )
  - Disconnection of load line (open).
- WSON10A package for surface mounting.

Note: Due to its MOS structure. This product is sensitive to static electricity.

Start of commercial production  
2020-03

#### 4. Block Diagram



Note: Since a function is explained, it may have omitted in part and may have simplified the functional block in a block, the circuit, the constant, etc.

**Figure 4.1 Block Diagram**

## 5. Pin Assignments

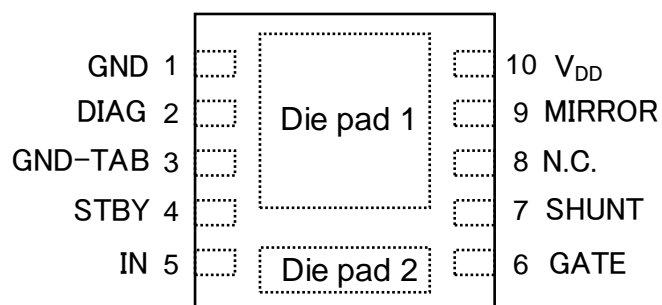


Figure 5.1 Pin Assignments (top view)

## 6. Pin Description

Table 6.1 Pin Description

Pin No	Symbol	Description
1	GND	Ground pin.
2	DIAG	Current sense output and diagnostic output.
3	GND-TAB	Ground pin.
4	STBY	Standby mode control pin.
5	IN	Input pin. Built in pull down resistor.
6	GATE	Output pin for an external FET drive
7	SHUNT	Input pin for shunt resistance connection.
8	N.C.	No-Connect pin.
9	MIRROR	An external FET source pin and a shunt resistance connect pin.
10	V <sub>DD</sub>	Power supply pin.

## 7. Operational Description

### 7.1. Protection for reverse connection of power supply

Reverse connection circuit turns on external FET via M1 in the figure and reduces external FET loss to prevent thermal destruction.

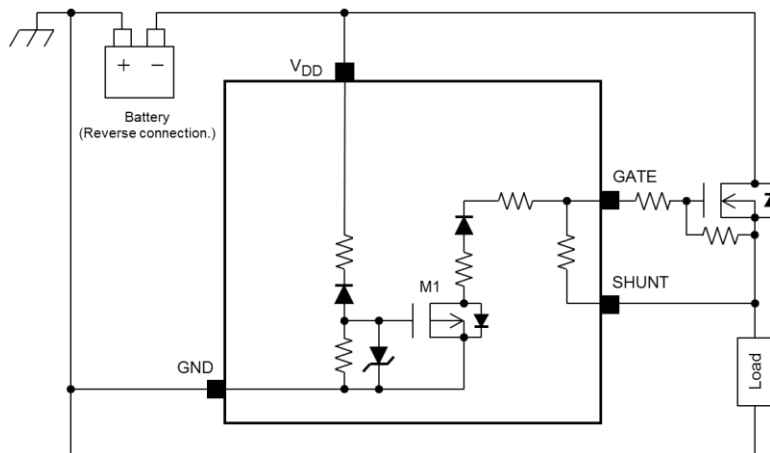


Figure 7.1 Reverse connection circuit.

### 7.2. Active clamp

Active clamp is a function that keeps the voltage between drain and source of external FET below at the break down voltage. When the surge voltage is generated by the inductive load, the voltage between  $V_{DD}$  and SHUNT increases and the active clamp circuit in Figure 7.2 outputs the voltage to the GATE pin. Therefore, the external FET will be in ON state and the voltage between drain and source of external FET will be clamped.

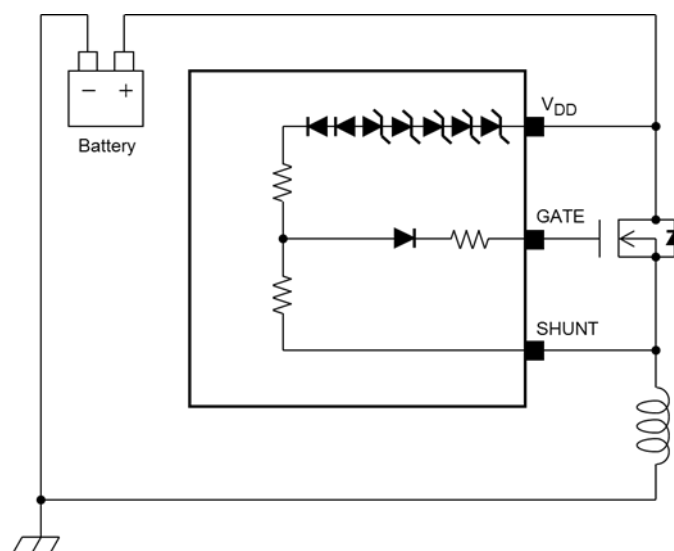
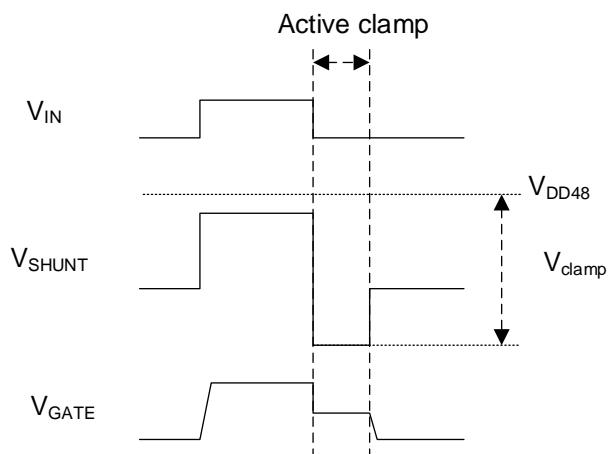


Figure 7.2 Active clamp circuit.



- $V_{IN}$ : IN pin input voltage
- $V_{SHUNT}$ : SHUNT pin input voltage
- $V_{GATE}$ : GATE pin output voltage
- $V_{clamp}$ : Active clamp voltage

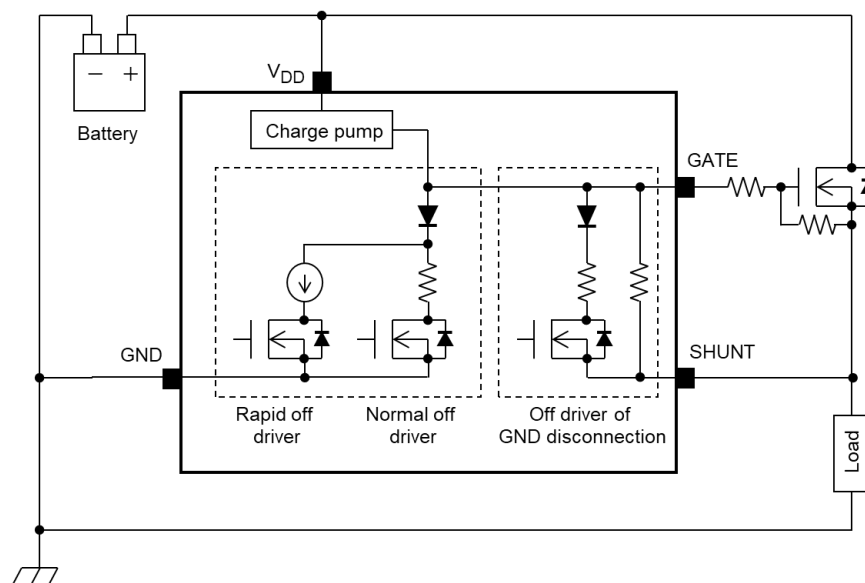
**Figure 7.3 Timing chart of Active clamp operation.**

## 7.3. Gate drive of Power MOSFET (Off driver)

Three kinds of drive circuits which control the turn-off of external FET exist in this products. Operation of each drive is explained below.

### 7.3.1. Normal off, rapid off

The normal off driver makes the external FET an OFF state via the IN pin. The rapid off driver operates and draws out the gate charge of the external FET quickly, when the latch is stopped by the anomaly detection. Whenever the rapid off driver operates, the normal off driver operates in parallel.

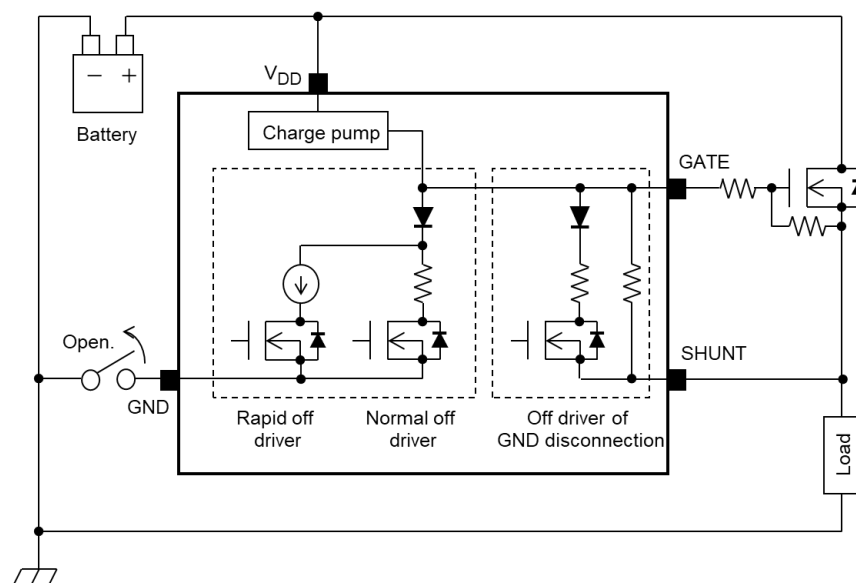


**Figure 7.4 Off driver circuit.**

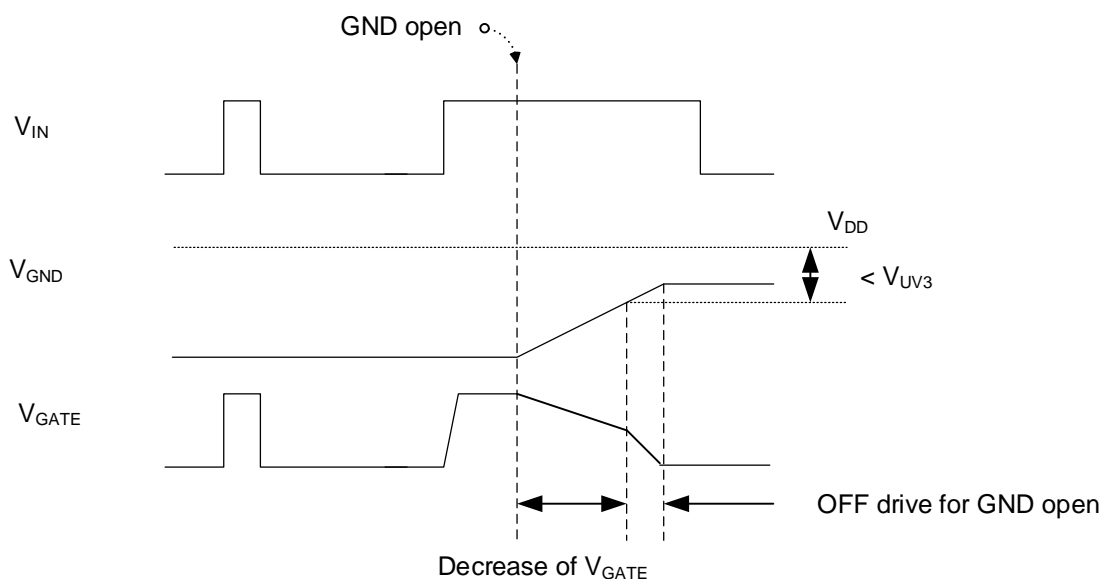
## 7.3.2. Protection for disconnection of GND terminal

GND disconnection protection is a function that keeps an OFF state in order to prevent a malfunction of the external FET, when GND terminal wiring of a unit is disconnected.

In OPEN state as shown in Figure 7.5, the off driver of GND disconnection operates, and turn off the external FET regardless of the condition of an input signal.



**Figure 7.5** Protection circuit for disconnection of GND terminal.

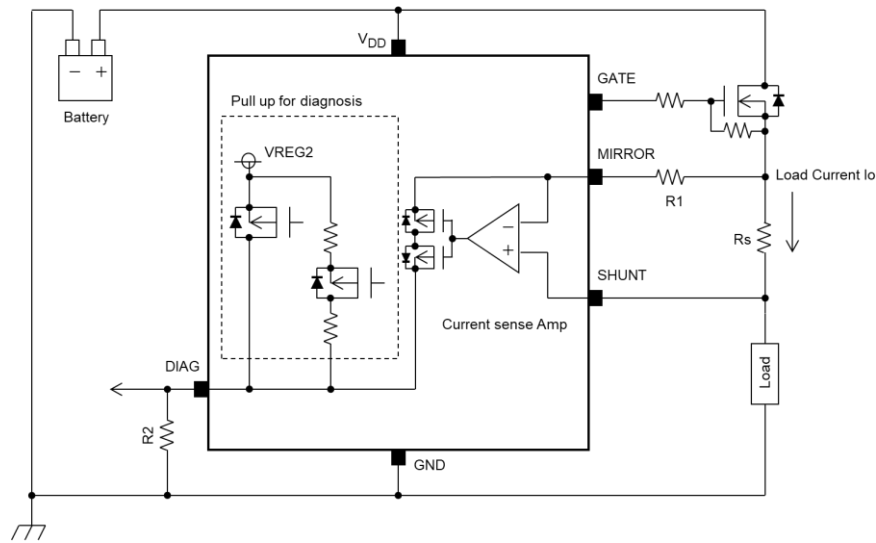


- $V_{IN}$ : IN pin input voltage
- $V_{GND}$ : GND pin voltage
- $V_{GATE}$ : GATE pin output voltage
- $V_{UV3}$ : Low voltage latch threshold

**Figure 7.6** Protect operation of disconnection of GND terminal.

## 7.4. Load current sense at time of Power MOSFET drive

For A/D-converter detection via the DIAG pin, the current sense amplifier and the pull up for diagnosis circuit in Figure 7.7 carry out the conversion from the current which flows into the shunt resistance  $R_s$  to the voltage.



**Figure 7.7 Current sense amp circuit.**

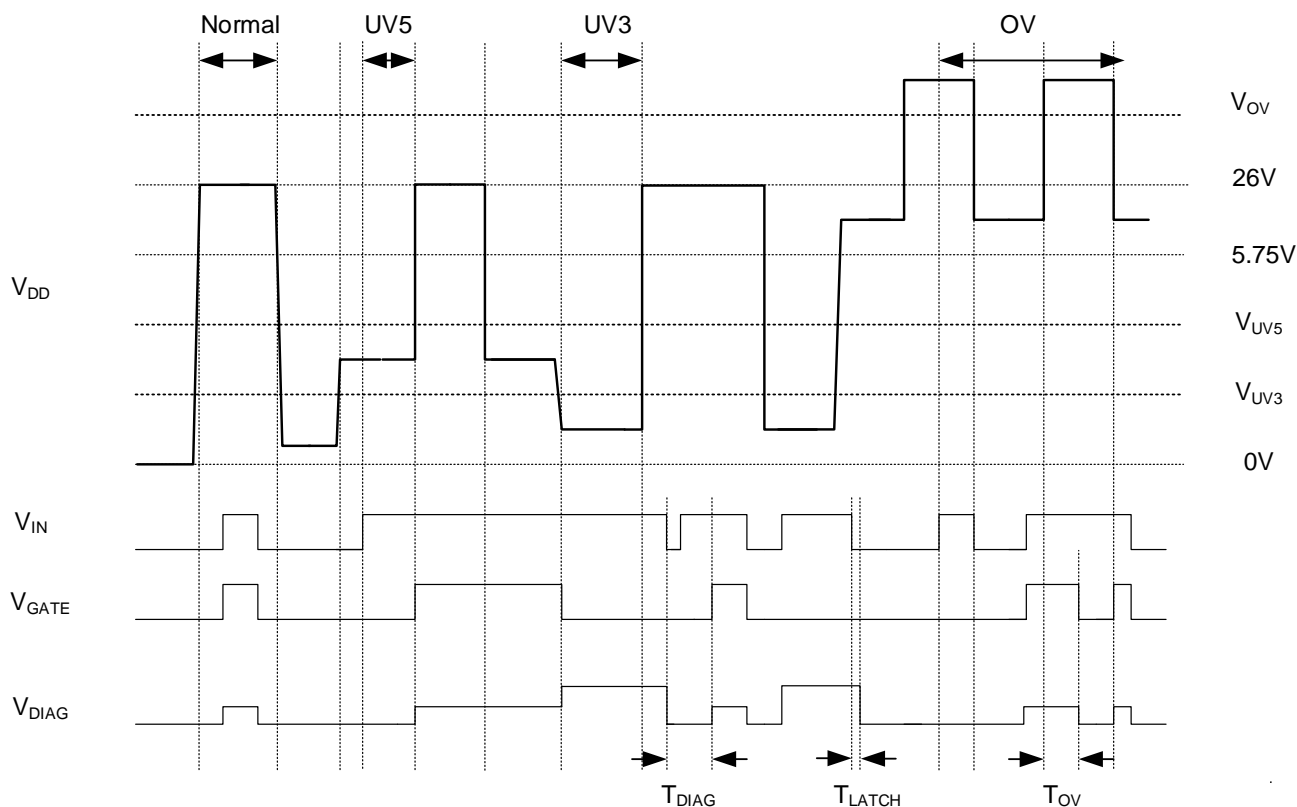
Load current sense output voltage is calculated as below. In addition, when abnormalities are detected, a load current sense output mode is changes to a diagnostic output mode. And the fixed voltage according to the diagnosis results is outputted.

$$V_{DIAG} = \frac{R2}{R1} \times (R_s \times I_O + V_{IO})$$

- $V_{DIAG}$ : DIAG pin output voltage
- $I_O$ : load current
- $V_{IO}$ : Input offset voltage

## 7.5. The abnormalities in power supply voltage ( $V_{DD}$ over voltage, $V_{DD}$ under voltage)

- When the voltage of a  $V_{DD}$  terminal is more than the over voltage detection threshold ( $V_{OV}$ ), the off-driver usually operates and the external FET turns off. After that, if the  $V_{DD}$  terminal voltage is less than the over voltage threshold voltage, the external FET is driven again.
  - In the case of  $V_{IN}=H$  and  $V_{DD}>V_{OV}$ , the off-driver operates after the mask time of  $T_{OV}$  (200us max) ( $V_{GATE}=H$  to  $L$ ).
  - In the case of  $V_{DD}>V_{OV}$  and  $V_{IN}=L$  to  $H$ , it keeps  $V_{GATE}=L$ .
- When  $V_{DD}$  terminal voltage is less than  $V_{UV3}$  (2.7V (typ.)), the rapid off-driver operates, carry out latch-off of the external FET, and outputs H state to DIAG.
- In case  $V_{DD}<V_{UV5}$ , the off-driver operates and  $V_{DD}$  goes up. After that, if  $V_{DD}$  is more than  $V_{UV5}$ , the off-driver will change to normal operation.
- Even if  $V_{DD}$  terminal voltage falls under the conditions of  $V_{GATE}=H$ ,  $V_{GATE}$  keeps H state, and external FET will be ON in  $V_{DD}>V_{UV3}$ . (Low-voltage extension operation)



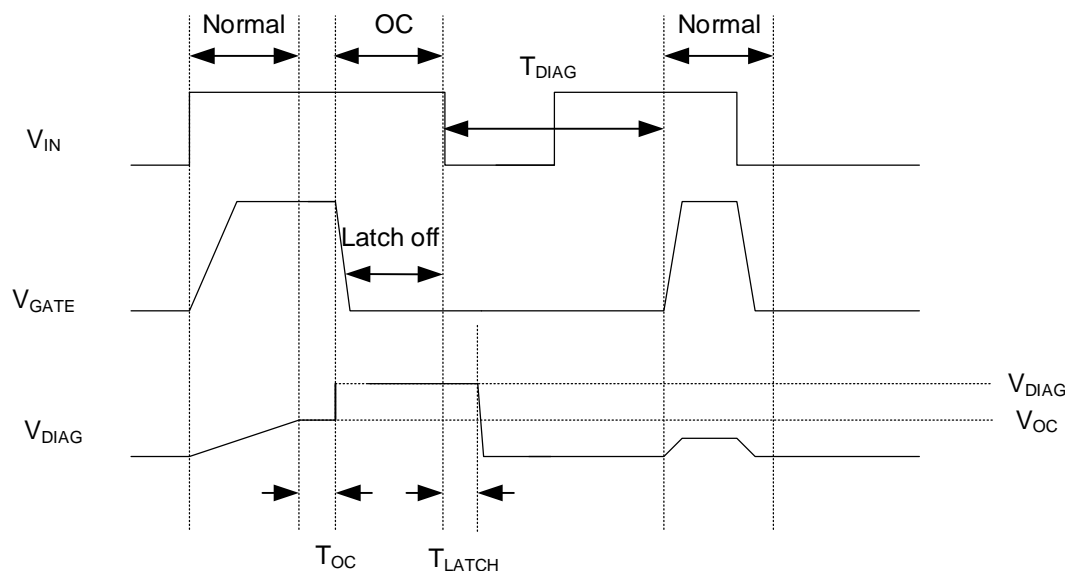
- $V_{IN}$ : IN pin input voltage
- $V_{GATE}$ : GATE pin output voltage
- $V_{DIAG}$ : DIAG pin output voltage
- $V_{UV3}$ : Low voltage latch threshold
- $V_{UV5}$ : Low voltage detection threshold
- $V_{OV}$ : Over voltage detection voltage
- $T_{DIAG}$ : DIAG clear standby time
- $T_{LATCH}$ : Latch clear standby time
- $T_{OV}$ : Over voltage detection mask time

**Figure 7.8 The abnormalities in power supply voltage**



## 7.6. Over current protection

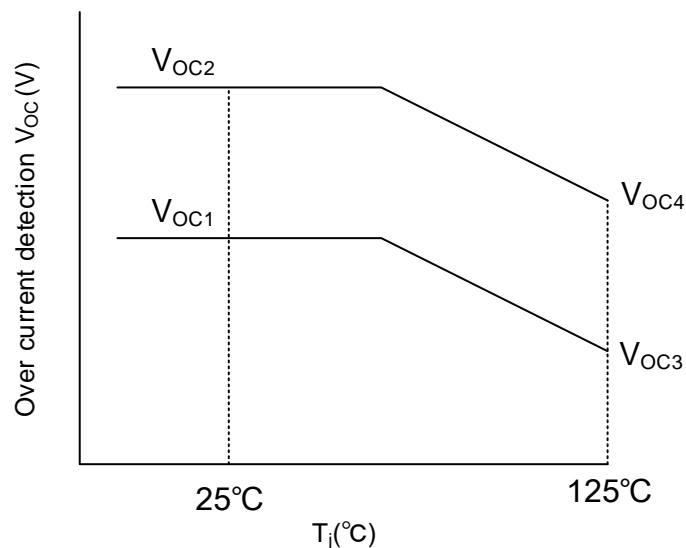
- When the current sense voltage ( $V_{DIAG}$ ) turns into more than over-current detecting voltage ( $V_{OC}$ ), the rapid off-driver operates to protect the external FET. After that, it becomes an OFF & latch state and outputs diagnostic contents.
- The filter (Over current detection delay time  $2.5\mu s$  (typ.)) is built in so that the over-current caused by a power supply variation may not be detected incorrectly.
- In case  $V_{IN}=H$  to  $L$ , the over current protection circuit releases latches. When a latch of DIAG is released, the clear standby time from the falling edge of  $V_{IN}(T_{DIAG})$  is set to 10ms (minimum). In a period of the standby time, the IN terminal cannot control the GATE terminal.



- $V_{IN}$ : IN pin input voltage
- $V_{GATE}$ : GATE pin output voltage
- $V_{DIAG}$ : DIAG pin output voltage
- $V_{OC}$ : Over current detection voltage
- $V_{DIAG1}$ : DIAG output voltage (High Level)
- $T_{OC}$ : Over current detection delay time
- $T_{LATCH}$ : Latch release mask time
- $T_{DIAG}$ : DIAG clear standby time

**Figure 7.9 Over current protection**

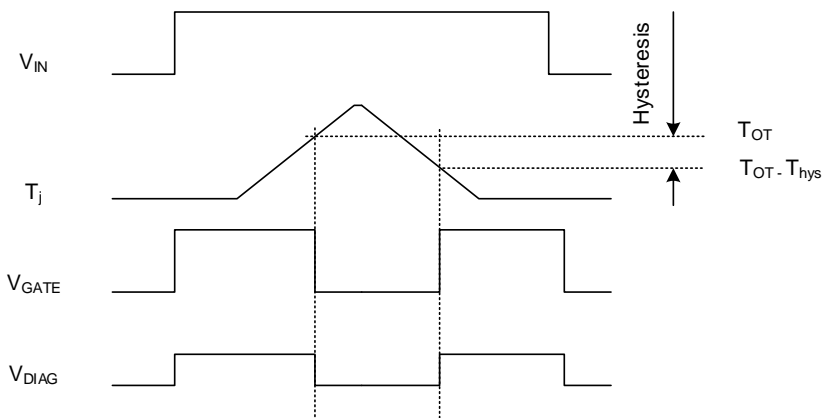
- The over current threshold voltage changes according to the power supply voltage and the junction temperature.
  - $V_{OC1}$ :  $V_{DD}=3V, T_j=25^\circ C$
  - $V_{OC2}$ :  $T_j=25^\circ C$
  - $V_{OC3}$ :  $V_{DD}=3V, T_j=125^\circ C$
  - $V_{OC4}$ :  $T_j=125^\circ C$
- The over current detecting voltage falls to 66% (typ.) of  $V_{OC2}$  and  $V_{OC4}$ , when the abnormalities in voltage between drain and source of the external FET occur.
- The over current detection voltage falls to 50% (typ.) of  $V_{OC2}$  and  $V_{OC4}$ , when the under voltage detection (UV5) occurs.



**Figure 7.10 Junction Temperature dependency of over current detection**

### 7.7. Over temperature protection.

The over temperature protection prevents destruction due to the temperature rise of this product and MOSFET, so if junction temperature exceeds Thermal detection temperature, normal off driver operates and turns the external FET off. When junction temperature drops below hysteresis set temperature, this product returns to normal operation.

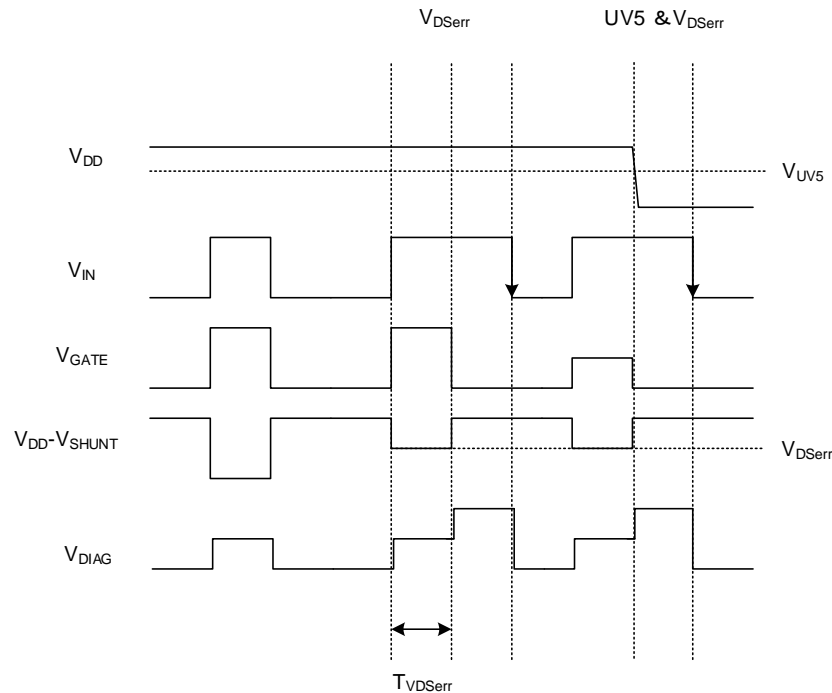


- $V_{IN}$ : IN pin input voltage
- $V_{GATE}$ : GATE pin output voltage
- $V_{DIAG}$ : DIAG pin output voltage
- $T_{OT}$ : Over heat detection temperature
- $T_{hys}$ : Hysteresis of thermal detection

**Figure 7.11 Over temperature protection**

## 7.8. Abnormalities in voltage between Drain and source of the external FET (VDS error)

- The voltage between drain and source of the external FET supervises the differential voltage between the  $V_{DD}$  pin and the SHUNT pin. If the voltage between drain source exceeds the VDS error detection threshold (1.4V (typ.)), the rapid off-driver operates and changes the external FET into the OFF & latch state. Therefore, the diagnostic output will be in H state.
- When a low-voltage (UV5) state occurs simultaneously with the abnormalities of the voltage between Drain and source, the rapid off-driver operates and makes the external FET into an OFF & latch state because of no detection time. The diagnostic output will become the H state.
- GATE pin and DIAG pin latches are released by  $V_{IN}=H$  to L.
- When an error is detected, it is judged as abnormal after the detection time ( $T_{VDSerr}$ ) to prevent malfunction due to noise.



- $V_{IN}$ : IN pin input voltage
- $V_{GATE}$ : GATE pin output voltage
- $V_{DD}-V_{SHUNT}$ : Voltage between  $V_{DD}$  pin and SHUNT pin
- $V_{DIAG}$ : DIAG pin output voltage
- $T_{VDSerr}$ : VDS error detection time

**Figure 7.12 Abnormalities in voltage between Drain and source of external FET**

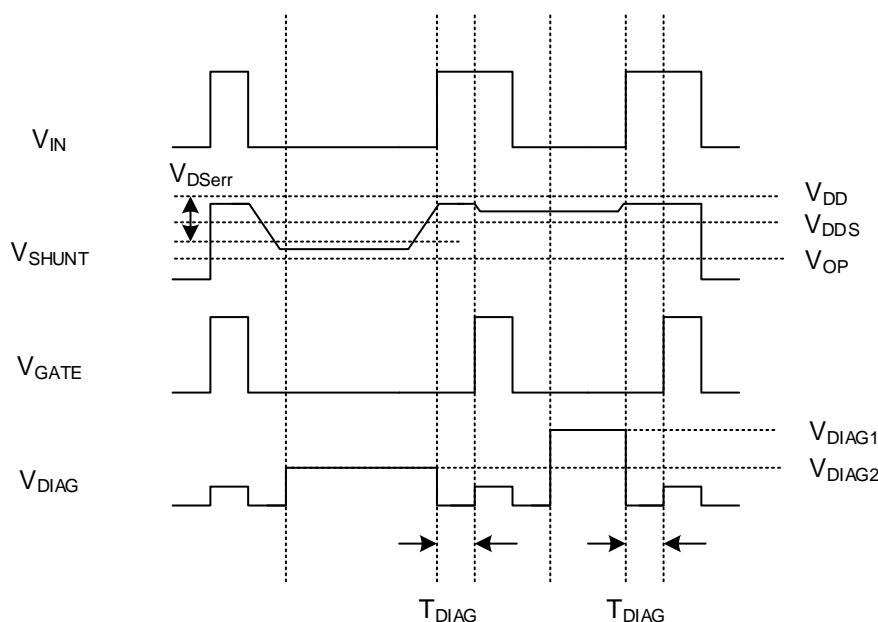
## 7.9. Load open / $V_{DD}$ short of load line and diagnosis output

The load open detects the disconnection of the load connected to SHUNT pin. The  $V_{DD}$  short of load line detects the  $V_{DD}$  short of the load connected to SHUNT pin. A circuit example is shown below (figure 7.14). The detection condition and DIAG pin output voltage for each item are as shown in the table below.

**Table 7.1 Load open detection /  $V_{DD}$  short of load line detection**

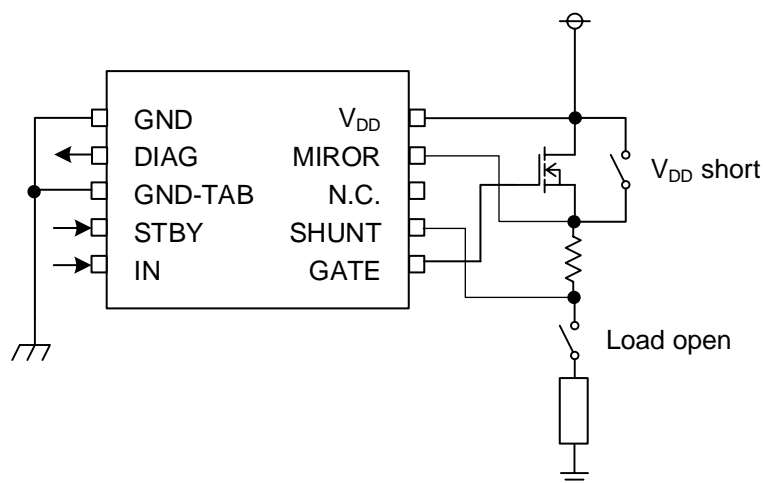
item	Detection condition	DIAG output voltage
Load open detection	$V_{OP} < V_{SHUNT}$ $V_{DSerr} < V_{DD} - V_{SHUNT}$	2.3V(minimum)
$V_{DD}$ short of load line	$V_{DDS} < V_{SHUNT}$ $V_{DD} - V_{SHUNT} < V_{DSerr}$	4.3V(minimum)

- The DIAG output voltage changes from rise edge of  $V_{IN}$  to normal operation after a DIAG clear waiting time ( $T_{DIAG}$ ). See the timing chart below.



- $V_{IN}$ : IN pin input voltage
- $V_{SHUNT}$ : SHUNT pin input voltage
- $V_{GATE}$ : GATE pin output voltage
- $V_{DIAG}$ : DIAG pin output voltage
- $V_{DIAG1}$ : DIAG output voltage (High level)
- $V_{DIAG2}$ : DIAG output voltage (Load open)
- $V_{OP}$ : Load open detection voltage
- $V_{DDS}$ :  $V_{DD}$  short detection voltage
- $T_{DIAG}$ : DIAG clear standby time

**Figure 7.13 Load open /  $V_{DD}$  short detection**



**Figure 7.14** Load open /  $V_{DD}$  short circuit example

### 7.10. Truth Table

Table 7.2 Truth Table

Operation.	STBY	IN	SHUNT,MIRROR	GATE	DIAG
Normal operation (Standby)	L	X	X	L	L
Normal operation	H	H	H ( $\approx V_{DD}$ )	H	analog
Over voltage detection (1) ( $V_{OV} < V_{DD}$ )	H	L	L	L	L
Over voltage detection (2) ( $V_{OV} < V_{DD}$ )	H	H	H ( $\approx V_{DD}$ )	L (Note1)	L (Note1)
Over temperature	H	X	X	L	L
UV5 ( $V_{DD} < V_{UV5}$ )	H	X	X	L	L
UV3 ( $V_{DD} < V_{UV3}$ )	H	X	X	L (Latch off)	H (Latch)
Over current detection	H	X	X	L (Latch off)	H (Latch)
VDS abnormal	H	X	$V_{DSerr} < (V_{DD} - V_{SHUNT})$	L (Note2) (Latch off)	H (Note2) (Latch)
VDS abnormal && UV5 ( $V_{DD} < V_{UV5}$ )	H	X	$V_{DSerr} < (V_{DD} - V_{SHUNT})$	L (Latch off)	H (Latch)
Load open detection.	H	L	$V_{OP} < V_{SHUNT}$	L	$V_{DIAG2}$
VDD short.	H	L	H ( $\approx V_{DD}$ )	L	H

Note1. Mask time 400 $\mu$ s (typ.)

Note2. Mask time 13ms (typ.)

## 7.11. State Transition Diagram

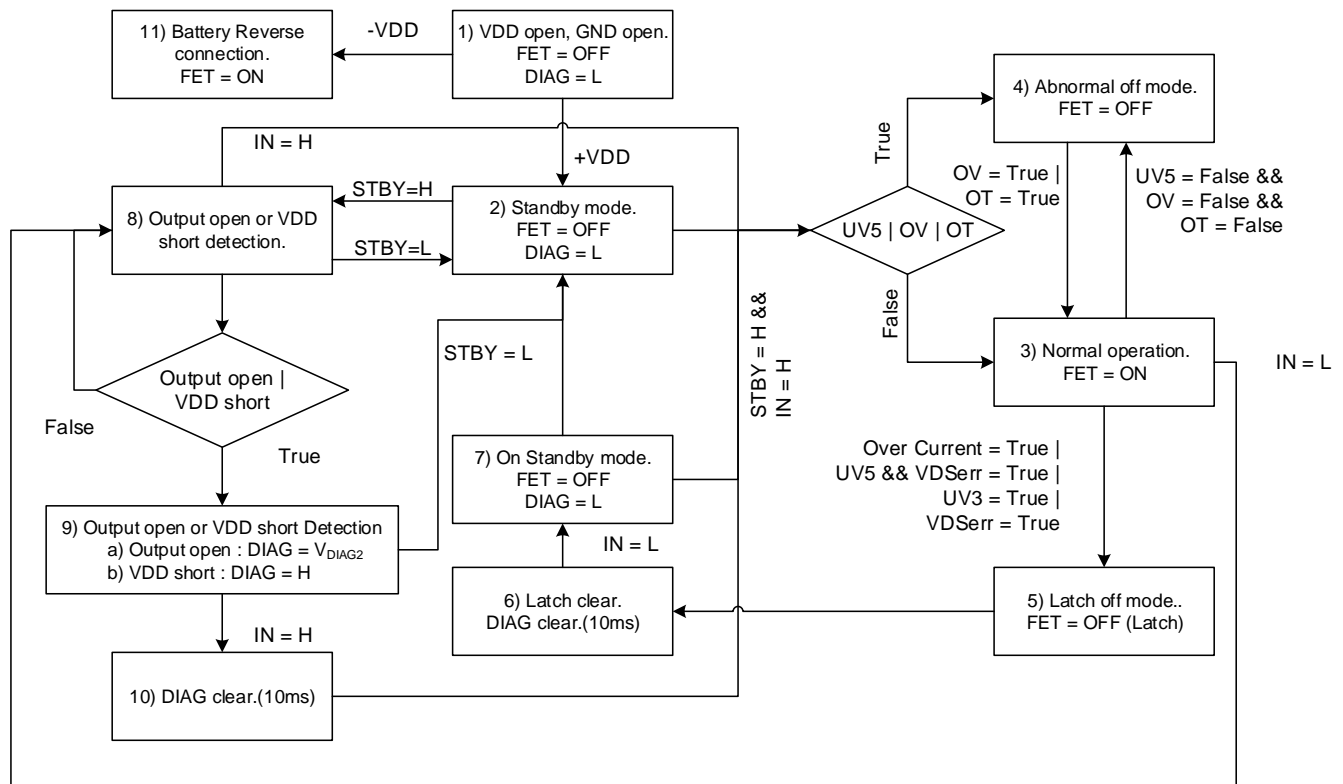


Figure 7.15 State Transition Diagram

## 8. Absolute Maximum Ratings

**Table 8.1 Absolute Maximum Ratings**

( $T_a = 25^\circ\text{C}$  unless otherwise specified)

Characteristics	Symbol	Rating	Unit	Comment(s)
Supply voltage	$V_{DD(1)}$	-16 to 26	V	Supply voltage
	$V_{DD(2)}$	-36 to 36	V	$t \leq 400\text{ms}$
	$V_{DD(3)}$	-40 to 40	V	$t \leq 20\text{ms}$
Input voltage	$V_{IN(1)}$	-16 to 26	V	IN, STBY, SHUNT, MIRROR
	$V_{IN(2)}$	-36 to 36	V	IN, STBY, SHUNT, MIRROR $t \leq 400\text{ms}$
	$V_{IN(3)}$	-40 to 40	V	IN, STBY, SHUNT, MIRROR $t \leq 20\text{ms}$
Output source current	$I_{GATE(+)}$	Internal ability	mA	GATE
Output sink current	$I_{GATE(-)}$	5	mA	GATE
Output voltage	$V_{GATE}$	-0.3 to 40	V	GATE
DIAG Output voltage	$V_{DIAG}$	-0.3 to 6	V	DIAG
DIAG Output current	$I_{DIAG}$	5	mA	DIAG
Power dissipation	$P_{D(1)}$	1.84	W	-
Operating temperature	$T_{opr}$	-40 to 125	$^\circ\text{C}$	-
Junction temperature	$T_j$	150	$^\circ\text{C}$	-
Storage temperature	$T_{stg}$	-55 to 150	$^\circ\text{C}$	-

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report, estimated failure rate, etc.)

### 8.1. Thermal Resistance

**Table 8.2 Thermal resistance**

Charateristics	Symbol	Rating	unit
Thermal resistance, junction to ambient	$R_{th(j-a)}$	67.6	$^\circ\text{C} / \text{W}$

Note: Glass epoxy board

Material: FR-4(4 layer) Board size: 76.2mmx114.3mmx1.6mm

Via:  $\phi 0.3\text{mm}$ (2 points)



## 9. Operating Ranges

Table 9.1 Operating Ranges

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Operating supply voltage	$V_{DD}$	$T_j = -40$ to $125^\circ\text{C}$	5.75	12.00	26.00	V

## 10. Electrical Characteristics

### 10.1. Electrical characteristics 1

Table 10.1 Electrical Characteristics 1

(Unless otherwise specified,  $T_j = -40$  to  $125^\circ\text{C}$ ,  $V_{DD} = 5.75$  to  $26\text{V}$ )

Characteristics	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage	$V_{DD(\text{opr})}$	$V_{DD}$	-	5.75	12.00	26.00	V
Supply current	$I_{DD(\text{off})}$	$V_{DD}$	$V_{DD} = 16\text{V}$ , Standby, $T_j = 25^\circ\text{C}$	-	-	3	$\mu\text{A}$
	$I_{DD(\text{on})}$	$V_{DD}$	$V_{DD} = 12\text{V}$ , $V_{IN} = V_{IH}$ , $T_j = 25^\circ\text{C}$	-	2	3	mA
High level input voltage	$V_{IH}$	IN, STBY	-	2.4	-	-	V
Low level input voltage	$V_{IL}$	IN, STBY	-	-	-	0.6	
Hysteresis	$V_{Ihys}$	IN, STBY	-	-	0.5	-	V
Input current	$I_{IH}$	IN, STBY	$V_{IN} = 5\text{V}$	-	21	50	$\mu\text{A}$
	$I_{IL}$	IN, STBY	$V_{IN} = 0\text{V}$	-1	-	1	
High level output voltage(1)	$V_{GATEH1}$	GATE	$V_{DD} = 3\text{V}$ , $V_{IN} = V_{IH}$ , GATE-SHUNT = $200\text{k}\Omega$	$V_{DD} + 6.5$	$V_{DD} + 8.6$	-	V
High level output voltage(2)	$V_{GATEH2}$	GATE	$V_{DD} = 5.75$ to $26\text{V}$ , $V_{IN} = V_{IH}$ , GATE-SHUNT = $200\text{k}\Omega$	$V_{DD} + 7.5$	$V_{DD} + 10.0$	$V_{DD} + 12.5$	V
High level output voltage(3)	$V_{GATEH3}$	GATE	$V_{DD} = -12\text{V}$ Measurement 1	6	-	-	V
Low level output voltage	$V_{GATEL}$	GATE	$V_{IN} = V_{IL}$	-	-	0.5	V
Active clamp voltage	$V_{\text{clamp}}$	$V_{DD}$ , SHUNT	$V_{IN} = V_{IL}$ , $V_{GATE} = 2\text{V}$ , $V_{SHUNT} = 0\text{V}$	35	39	-	V
Latch release mask time	$T_{\text{LATCH}}$	-	$V_{IN} = V_{IL}$	-	50	-	$\mu\text{s}$
Switching time	$T_{d\text{-ON}}$	GATE	Measurement 2, $T_j = 25^\circ\text{C}$	-	35	55	$\mu\text{s}$
	$T_{d\text{-OFF}}$			-	154	195	
	$T_r$			-	321	460	
	$T_f$			-	138	176	

## 10.2. Electrical characteristics 2

Table 10.2 Electrical Characteristics 2

(Unless otherwise specified,  $T_j = -40$  to  $125^\circ\text{C}$ ,  $V_{DD} = 5.75$  to  $26\text{V}$ )

Characteristics	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Off impedance at GND open	$R_{GO}$	GATE	Measurement 3	25	51	80	k $\Omega$
GATE-SHUNT resistance	$R_{GSH}$	GATE	-	500	1000	2000	k $\Omega$
Rapid off state current	$I_{GL}$	GATE	Latch off state.	100	237	500	mA
Over current detection (1)	$V_{OC1}$	DIAG	$V_{DD}=3\text{V}, T_j=25^\circ\text{C}$	-	1.75	-	V
Over current detection (2)	$V_{OC2}$	DIAG	$T_j=25^\circ\text{C}$	3.25	3.45	3.65	V
Over current detection (3)	$V_{OC3}$	DIAG	$V_{DD}=3\text{V}, T_j=125^\circ\text{C}$	-	1.4	-	V
Over current detection (4)	$V_{OC4}$	DIAG	$T_j=125^\circ\text{C}$	2.6	2.8	3.2	V
Over current threshold down rate at VDS error	-	-	$V_{DSerr}$ detection.	-	66	-	%
Over current threshold down rate at Low voltage	-	-	UV5 detection.	-	50	-	%
Over current detection delay time	$T_{OC}$	-	-	-	2.5	10.0	$\mu\text{s}$
Over heat detection temperature	$T_{OT}$	-	$V_{STBY} = V_{IH}$	150	169	200	$^\circ\text{C}$
Hysteresis of thermal detection	$T_{hys}$	-	-	-	16	-	$^\circ\text{C}$
Low voltage latch threshold (UV3)	$V_{UV3}$	$V_{DD}$	$V_{STBY} = V_{IH}$	2.5	2.7	3.0	V
Low voltage detection threshold (UV5)	$V_{UV5}$	$V_{DD}$	$V_{STBY} = V_{IH}$	4.15	4.40	4.65	V
UV5 release voltage	$V_{UV5R}$	$V_{DD}$	$V_{STBY} = V_{IH}$	4.9	5.1	5.4	V
Over voltage detection voltage (OV)	$V_{OV}$	$V_{DD}$	$V_{STBY} = V_{IH}$	26.0	27.4	30.0	V
Over voltage detection mask time	$T_{OV}$	$V_{DD}$	$V_{STBY} = V_{IH}$	150	400	650	$\mu\text{s}$
VDS error detection threshold	$V_{DSerr}$	$V_{DD}$ SHUNT	$V_{STBY} = V_{IH}, V_{IN} = V_{IH}$	1.0	1.4	2.0	V
VDS error detection time	$T_{VDSerr}$	$V_{DD}$ SHUNT	$V_{STBY} = V_{IH}, V_{IN} = V_{IH}$	10	13	20	ms
SHUNT leakage current	$I_{SHUNTS}$	SHUNT	$V_{IN} = V_{STBY} = L,$ $V_{SHUNT} = 0\text{V}, V_{DD} = 16\text{V}$	-	-	1.5	$\mu\text{A}$
Load open detection resistance	$R_{OP}$	SHUNT	-	5	11	20	k $\Omega$
Load open detection voltage	$V_{OP}$	SHUNT	$V_{STBY} = V_{IH}, V_{IN} = V_{IL}$	2.0	2.6	-	V
$V_{DD}$ short detection voltage	$V_{DDS}$	SHUNT	$V_{STBY} = V_{IH}, V_{IN} = V_{IL}$	$V_{DD}-2$	-	$V_{DD}$	V
DIAG clear standby time	$T_{DIAG}$	DIAG	$V_{STBY} = V_{IH},$ Error detection is canceled	10	-	20	ms
DIAG output voltage (High level)	$V_{DIAG1}$	DIAG	Abnormality is detected DIAG-GND = 10k $\Omega$	4.3	-	5.0	V
DIAG output voltage (Load open)	$V_{DIAG2}$	DIAG	Open is detected. DIAG-GND = 10k $\Omega$	2.3	-	3.8	V

## 10.3. Current sense amp Electrical Characteristics

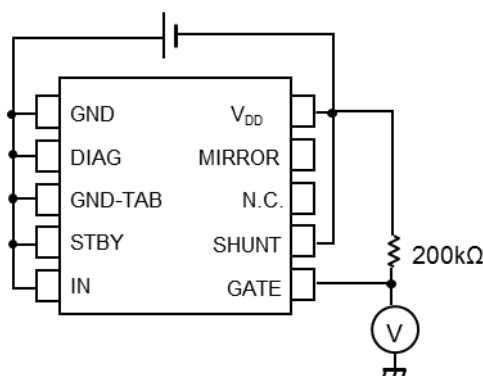
**Table 10.3 Current sense amp Electrical Characteristics**

(Unless otherwise specified,  $T_j = -40$  to  $125^\circ\text{C}$ ,  $V_{DD} = 5.25$  to  $26\text{V}$ )

Characteristics	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Common mode input voltage range	$CMV_{IN}$	SHUNT, MIRROR	-	2.5	-	$V_{DD}$	V
Input offset voltage	$V_{IO}$	SHUNT, MIRROR	$V_{DD}=13.5\text{V}$ , $T_j=25^\circ\text{C}$ Measurement 4	-2	-	2	mV
Input offset voltage temperature drift	$V_{IOT}$	SHUNT, MIRROR	$V_{DD}=13.5\text{V}$ , $T_j=25^\circ\text{C}$ Measurement 4	-10	-	10	$\mu\text{V}/^\circ\text{C}$
SHUNT terminal current	$I_{SHUNT}$	SHUNT	$V_{SHUNT}=V_{DD}$ , $V_{IN}=5\text{V}$	-	-	5	$\mu\text{A}$
MIRROR terminal current	$I_{MIRROR}$	MIRROR	$V_{MIRROR}=V_{DD}$ , $V_{IN}=5\text{V}$	-	-	5	$\mu\text{A}$

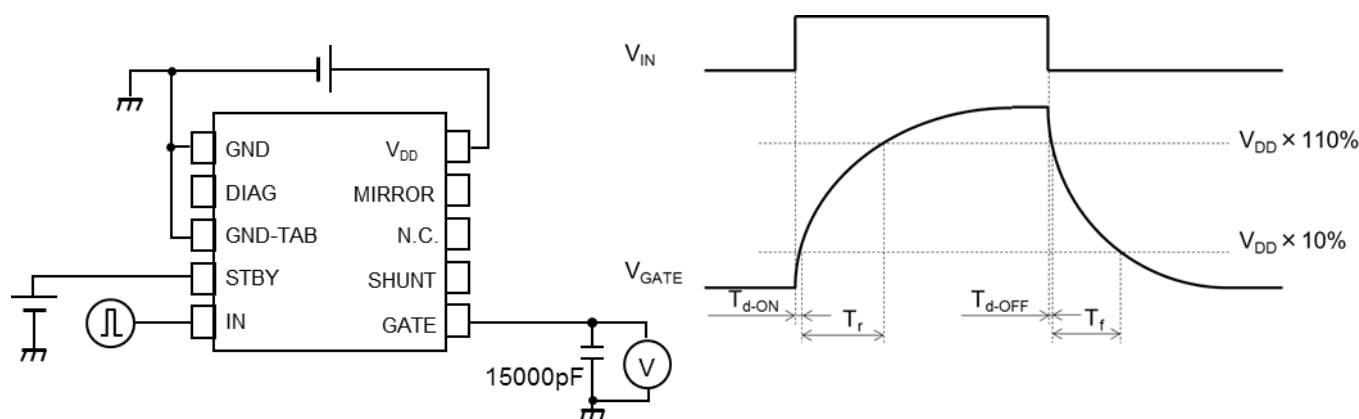
## 11. Test Circuit

### 11.1. Test circuit 1 High level output voltage (3)



**Figure 11.1 Test circuit 1**

### 11.2. Test circuit 2 Switching time ( $T_{d-ON}$ , $T_{d-OFF}$ , $T_r$ , $T_f$ )



**Figure 11.2 Test circuit 2**

## 11.3. Test circuit 3 Off impedance at GND open

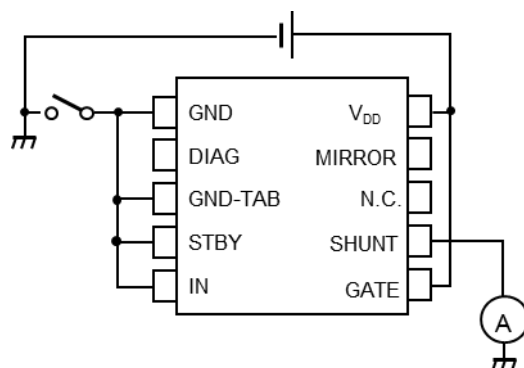


Figure 11.3 Test Circuit 3

## 11.4. Test circuit 4 Input offset voltage

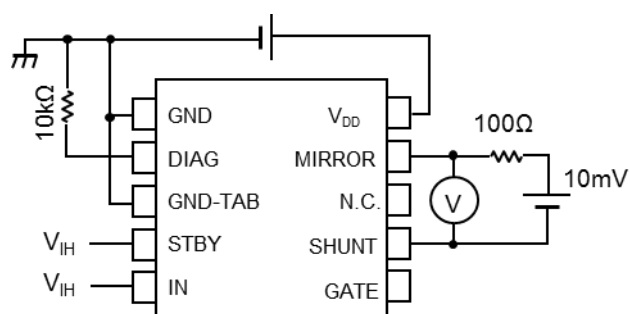
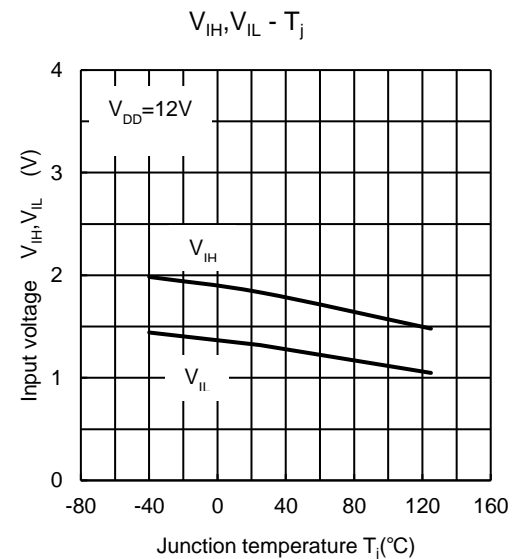
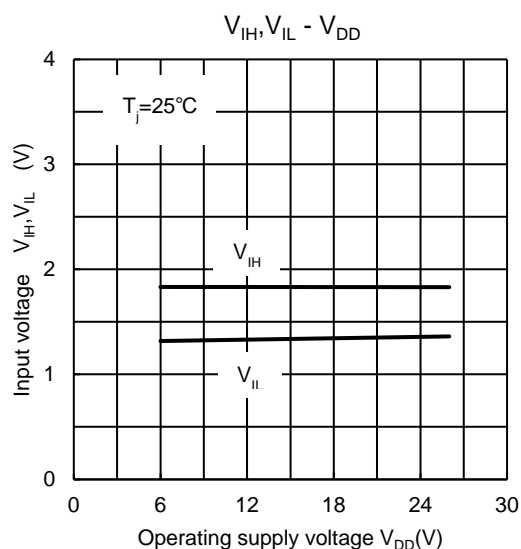
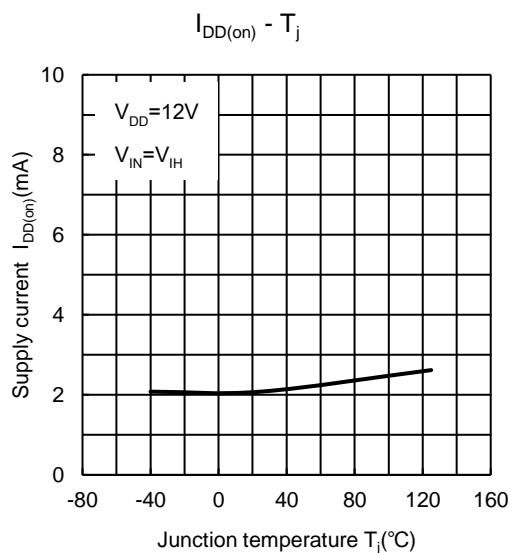
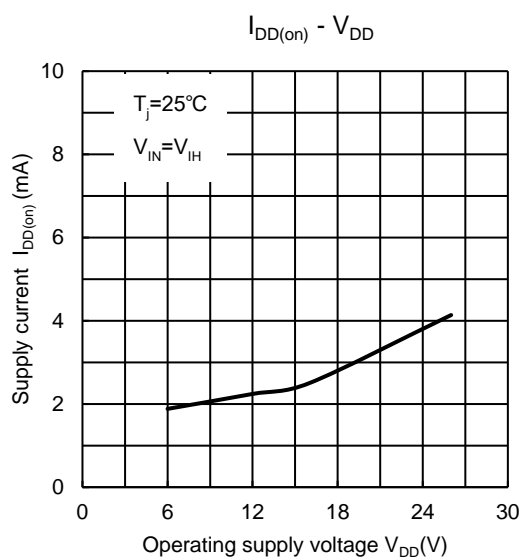
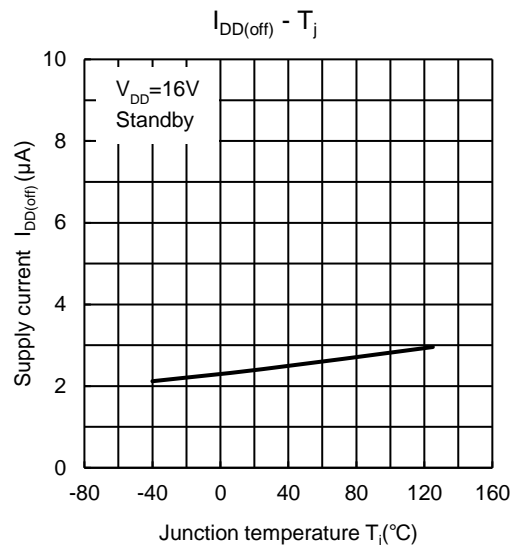
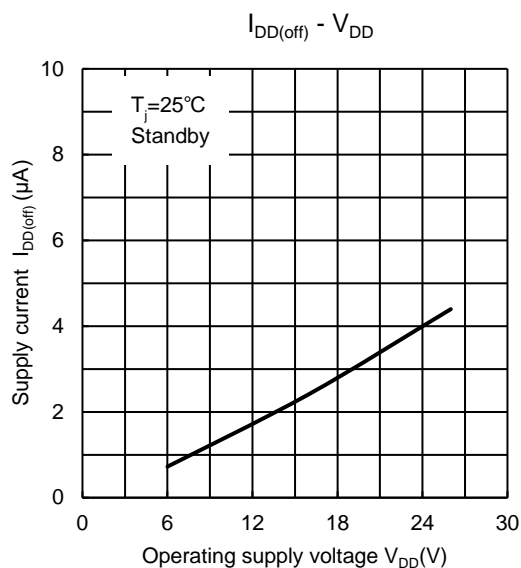
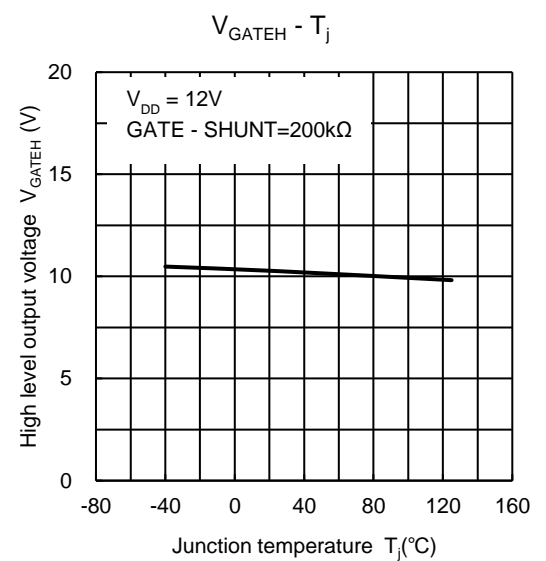
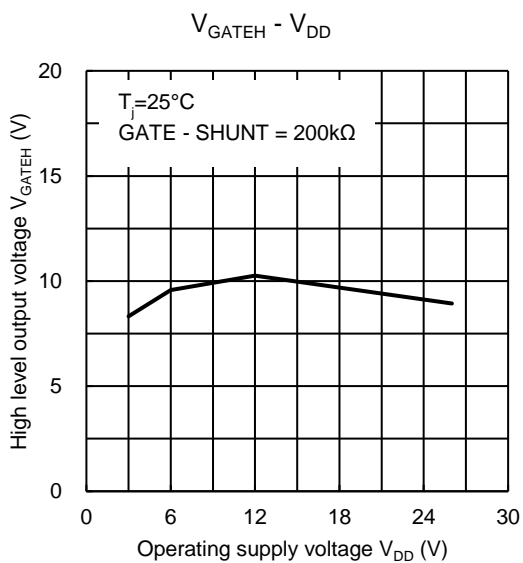
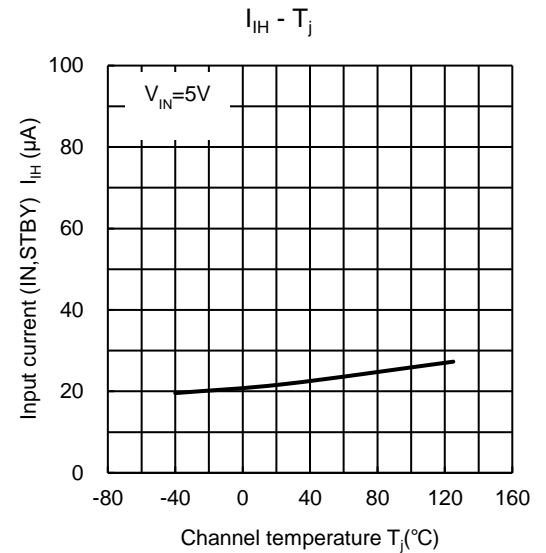
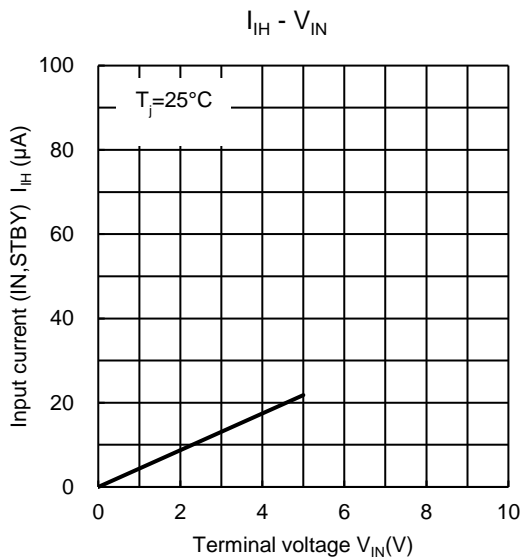
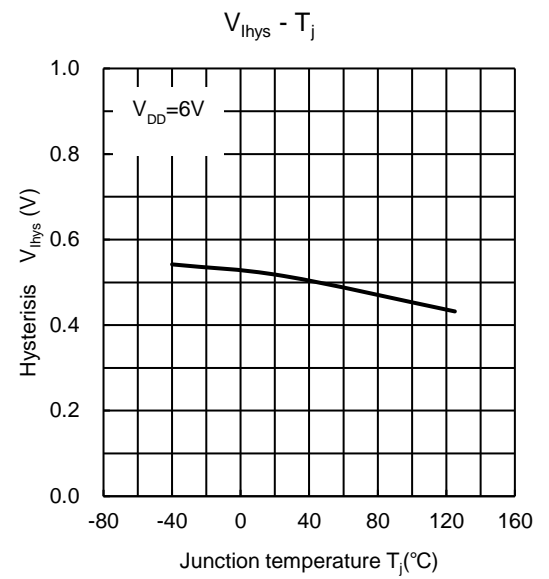
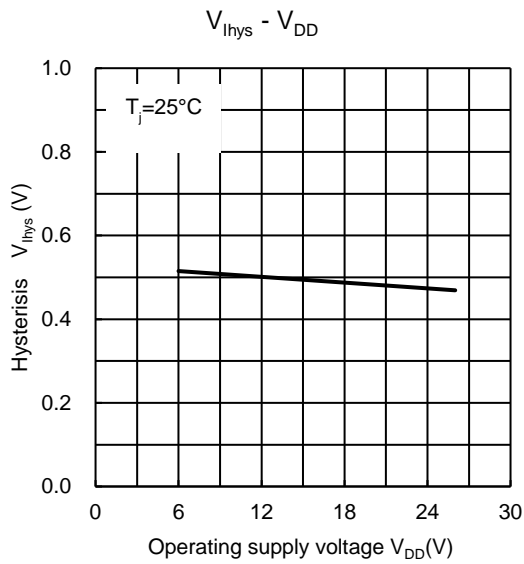


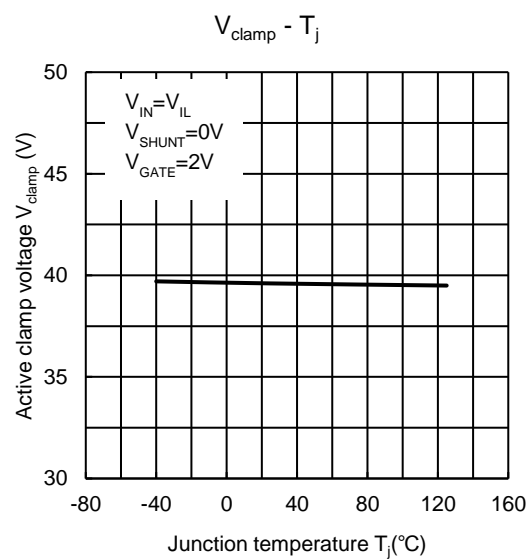
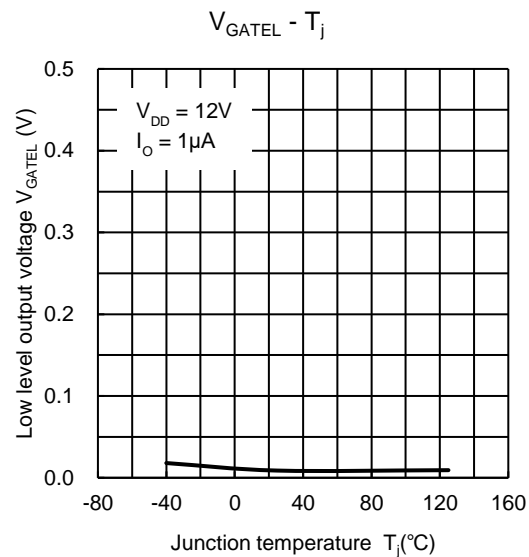
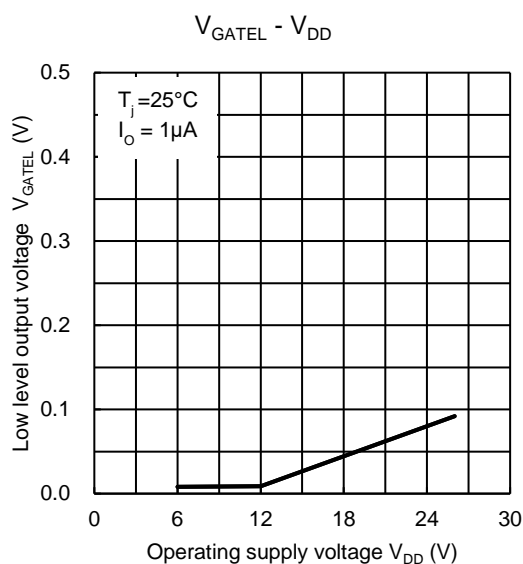
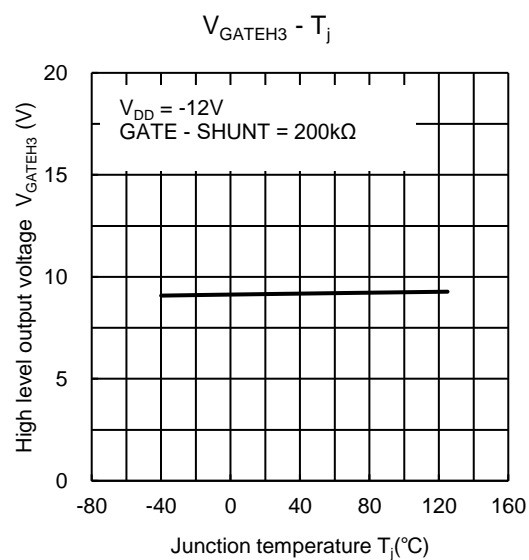
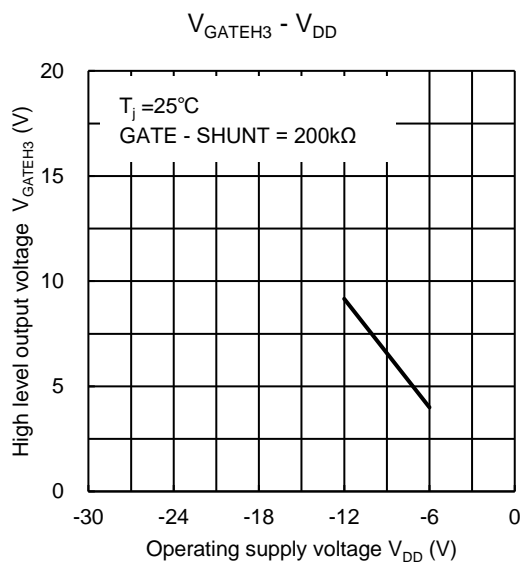
Figure 11.4 Test Circuit 4

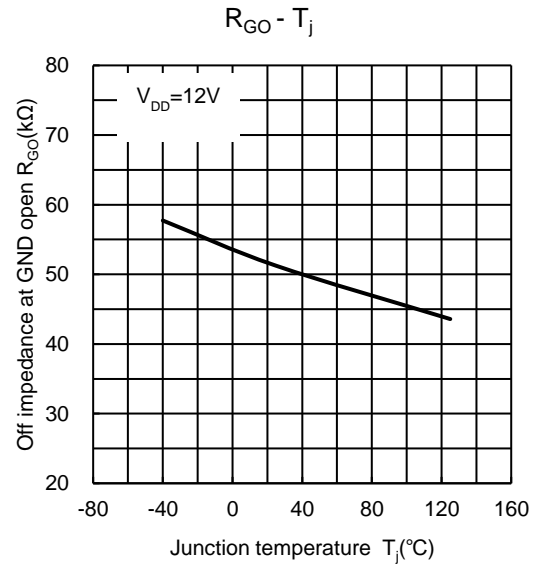
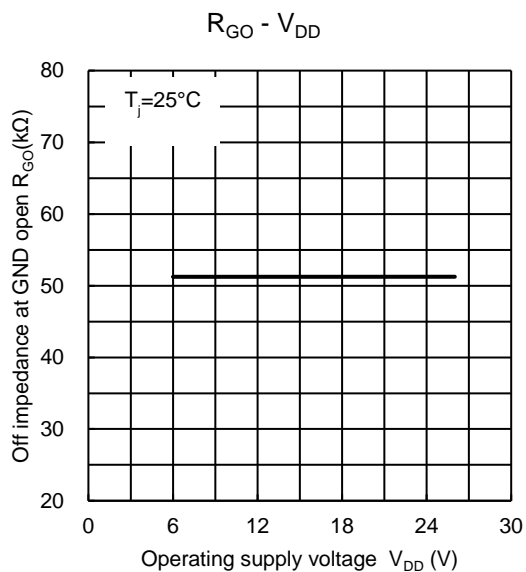
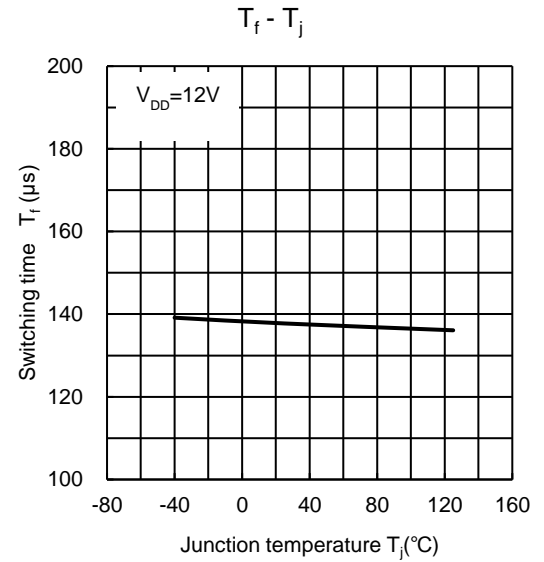
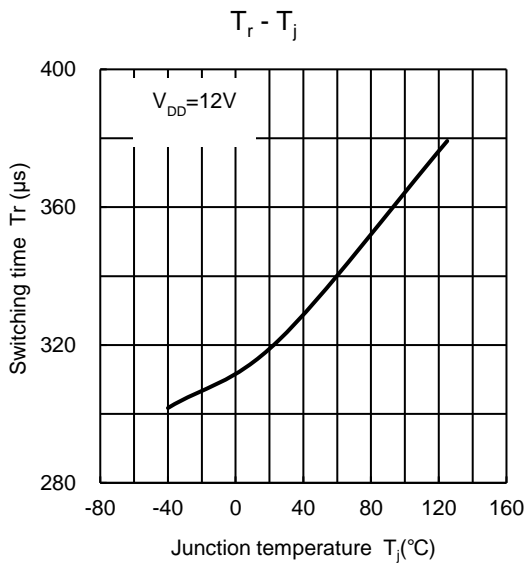
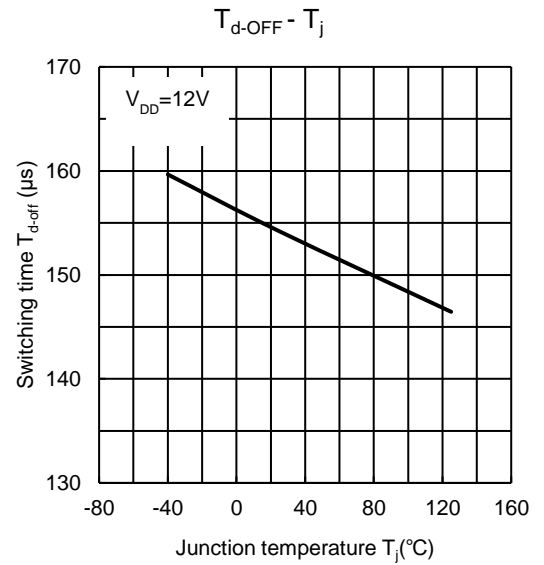
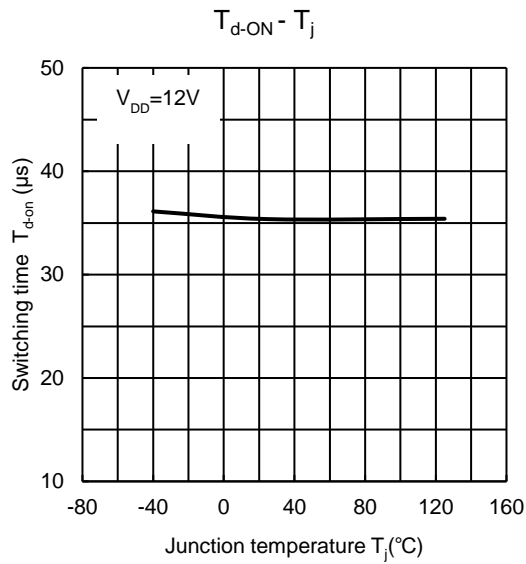
## 12. Characteristic curves

The below characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



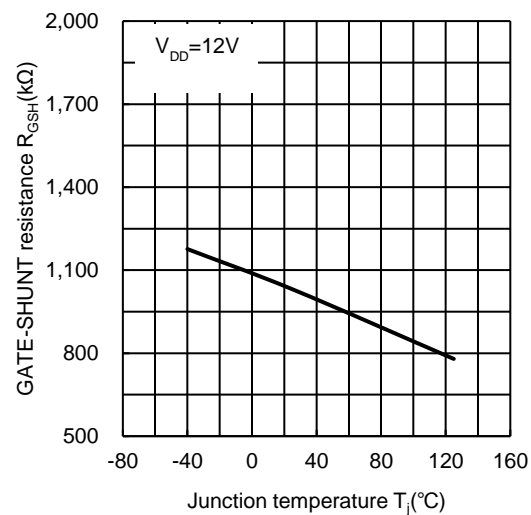




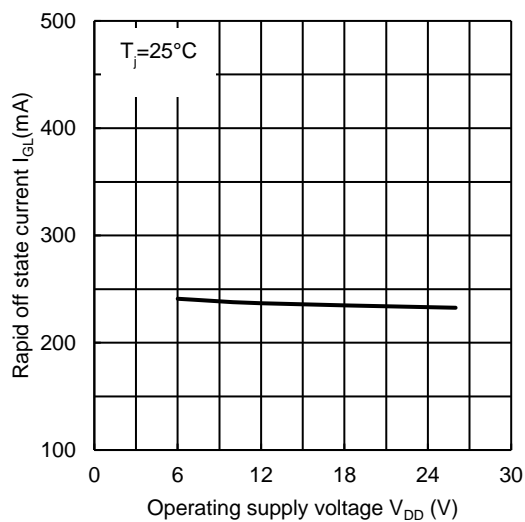




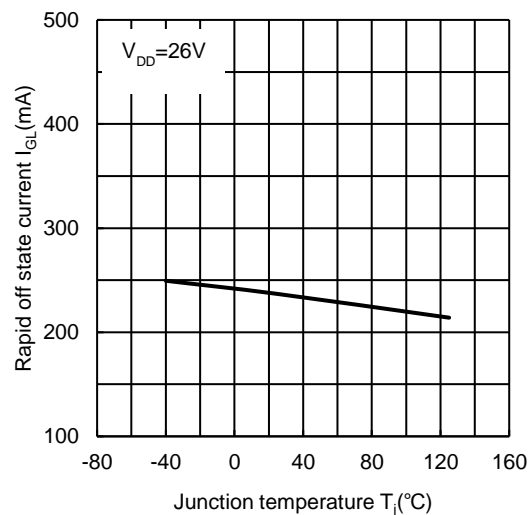
$R_{GSH} - T_j$



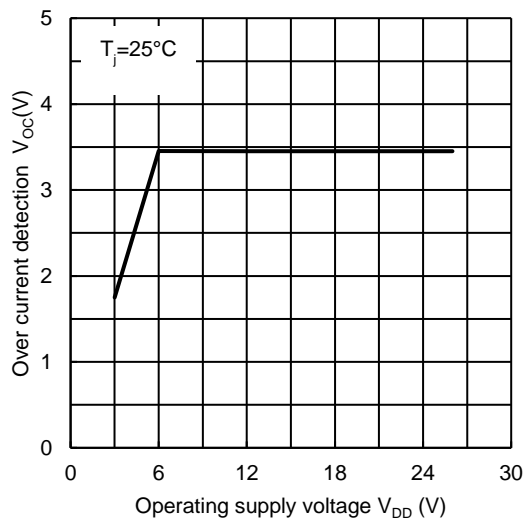
$I_{GL} - V_{DD}$



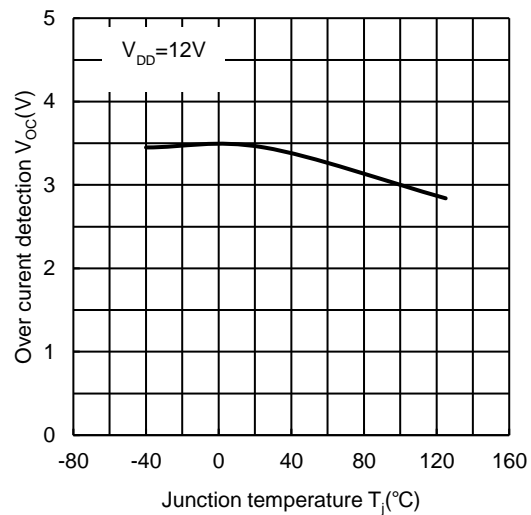
$I_{GL} - T_j$

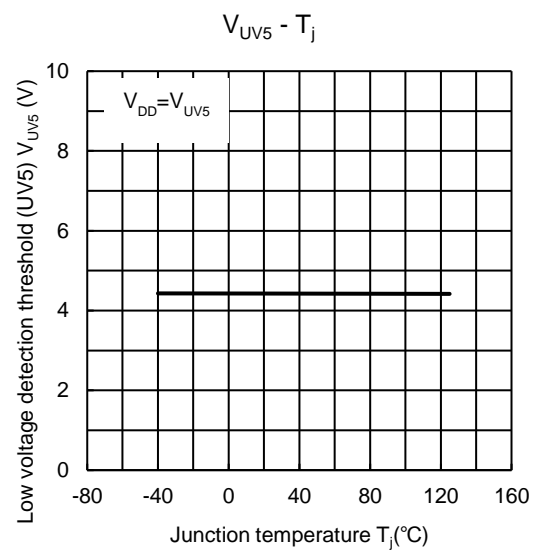
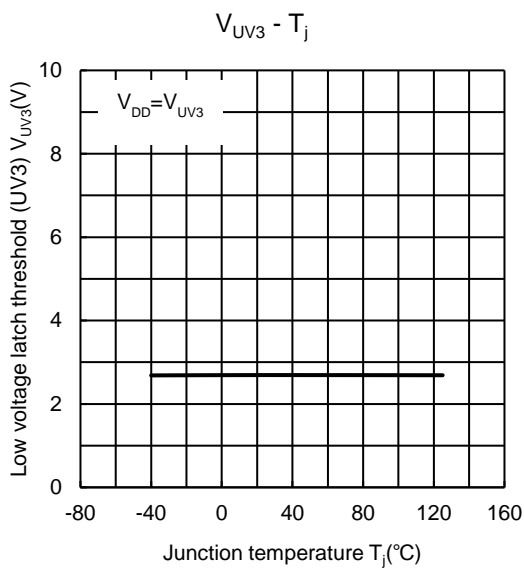
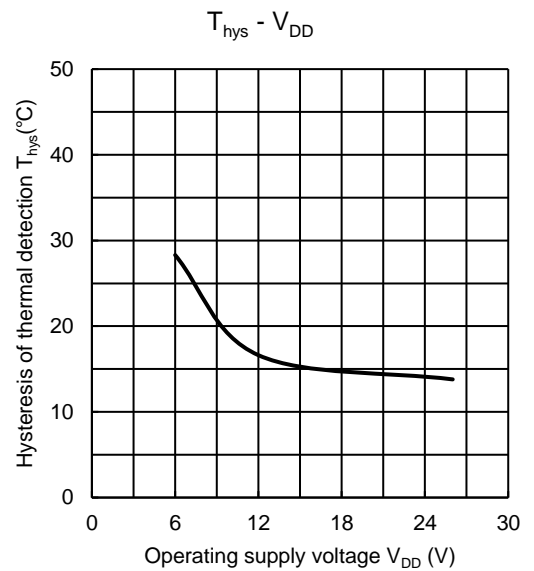
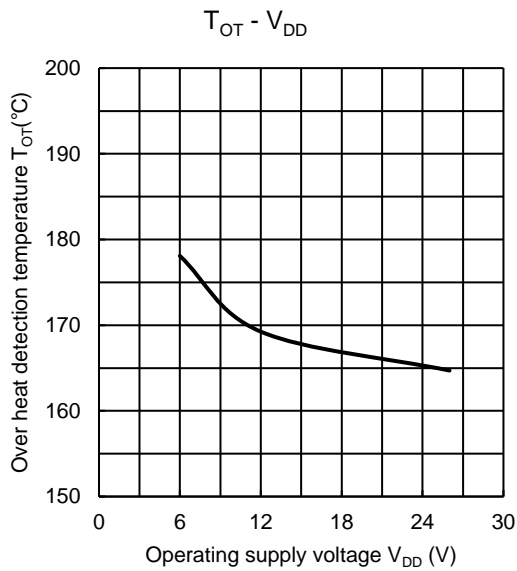
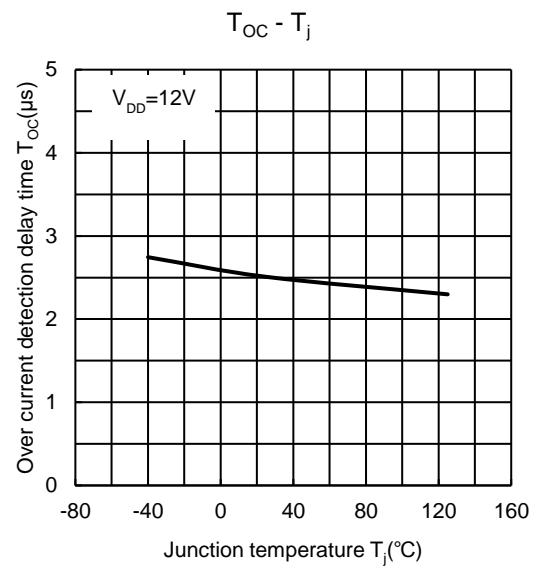
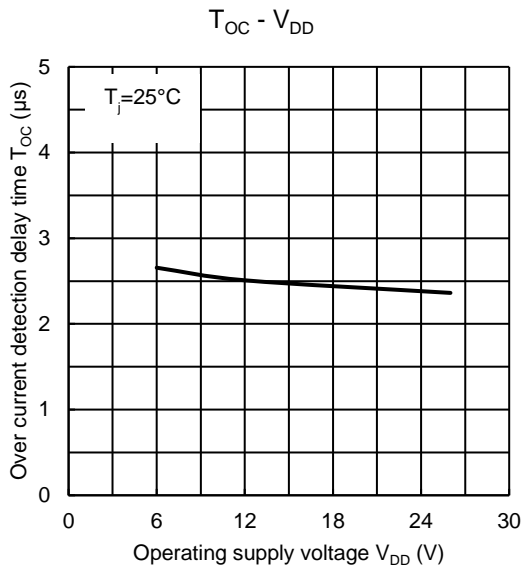


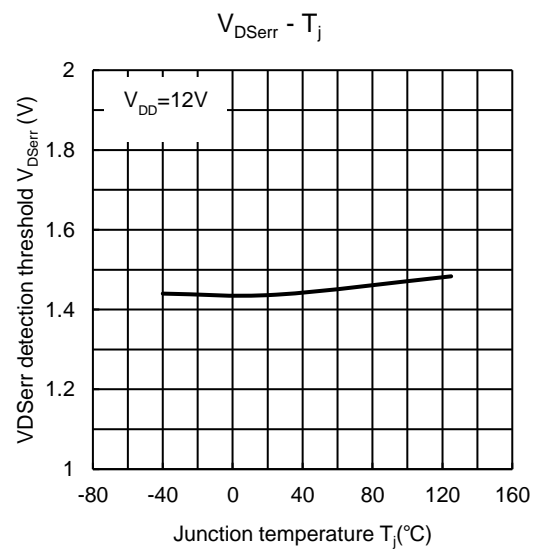
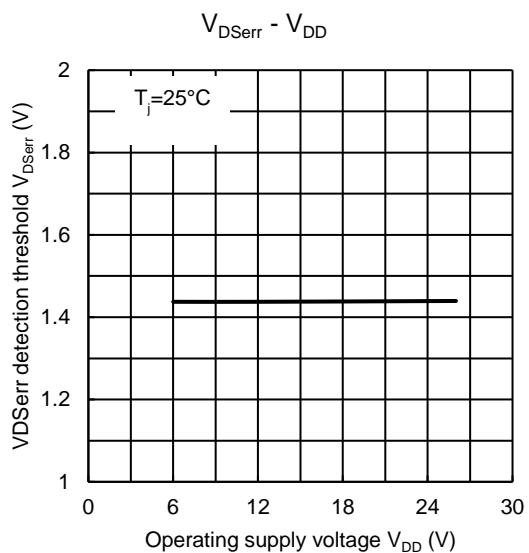
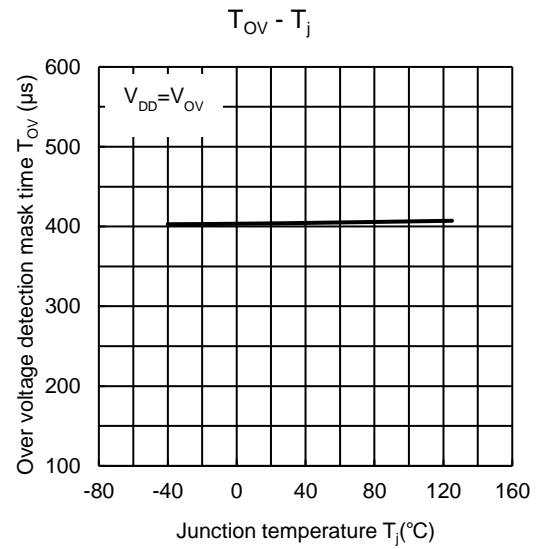
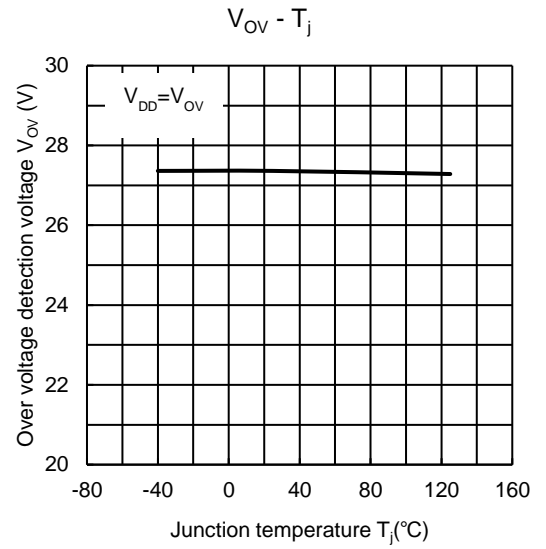
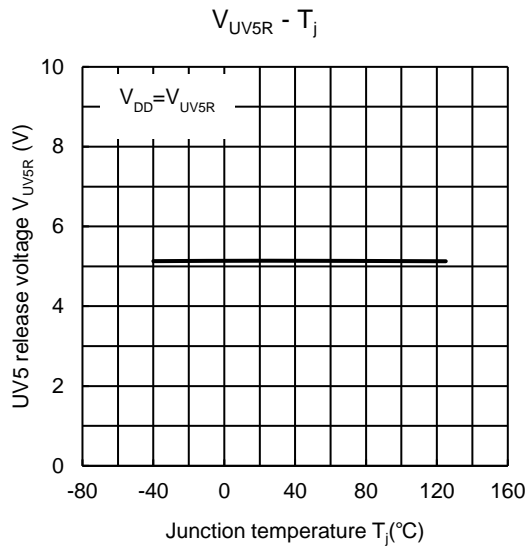
$V_{OC} - V_{DD}$

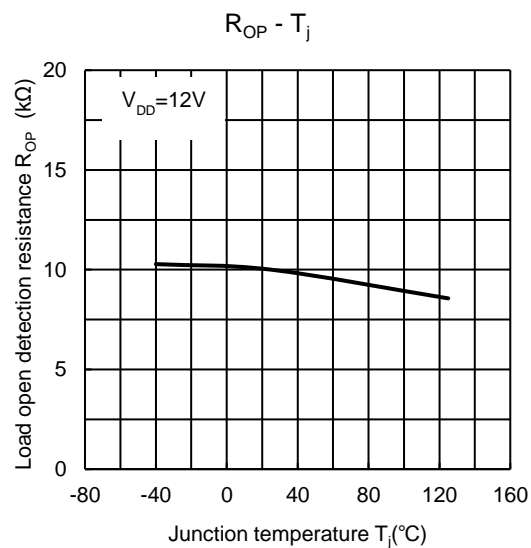
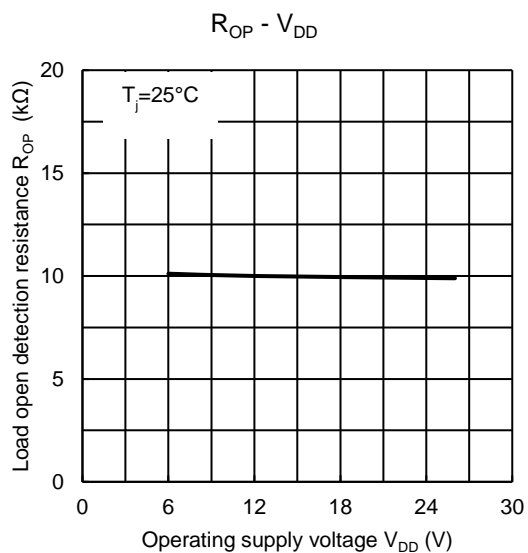
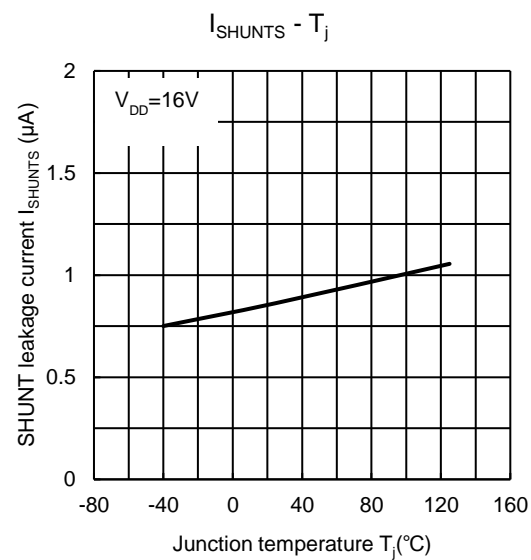
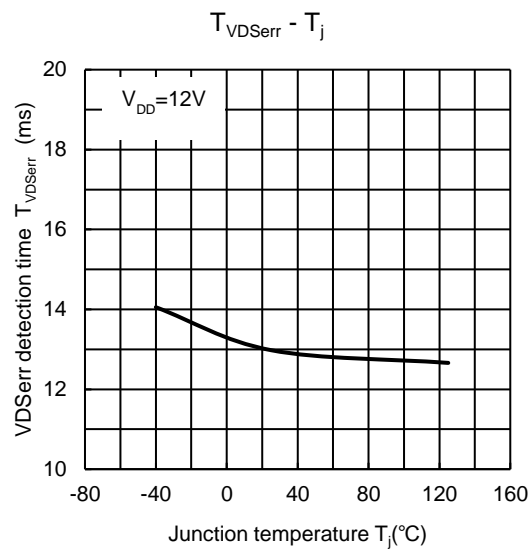
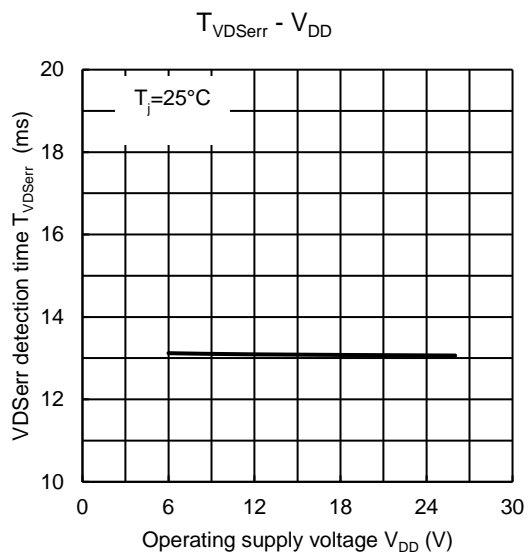


$V_{OC} - T_j$

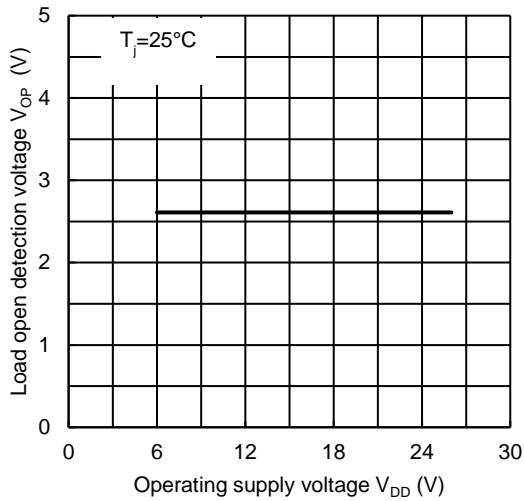




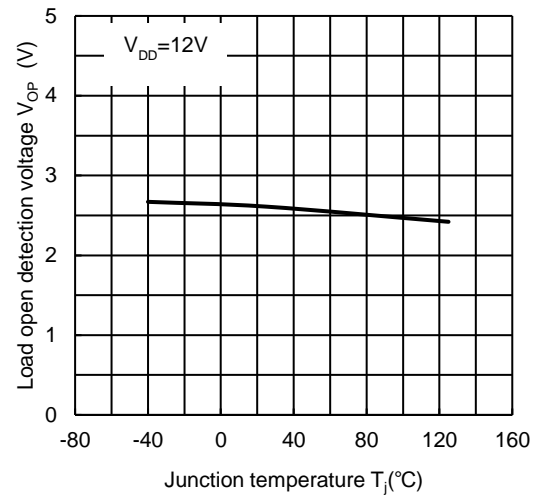




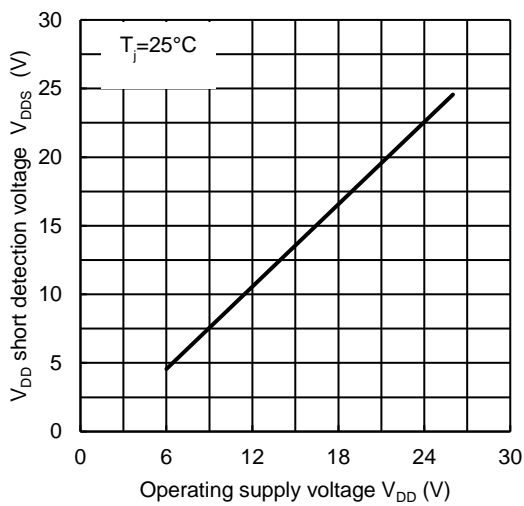
$V_{OP} - V_{DD}$



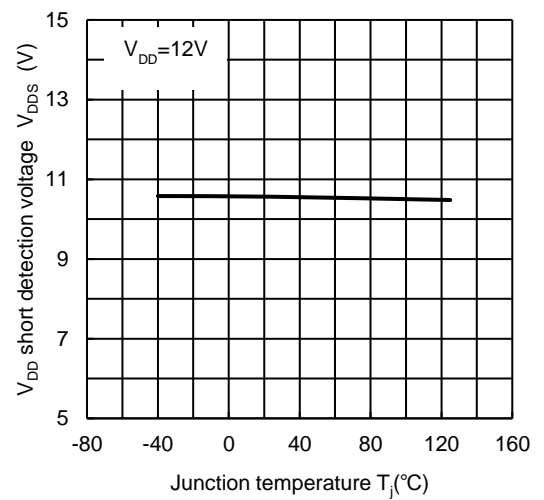
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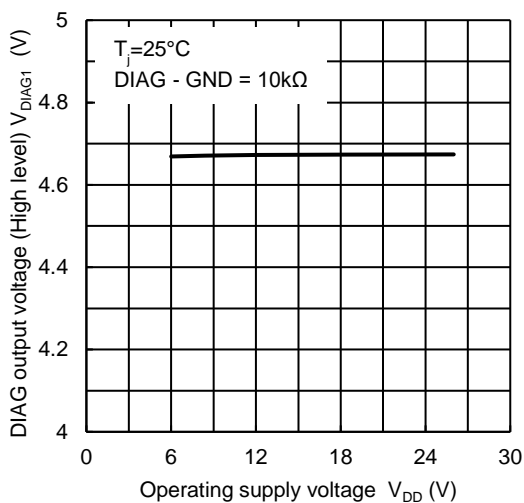
$V_{DDS} - V_{DD}$



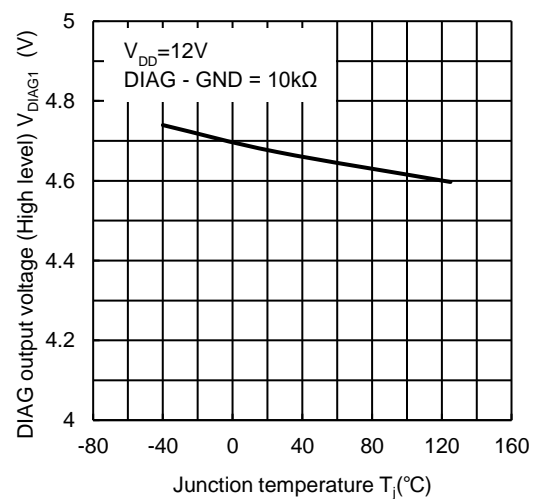
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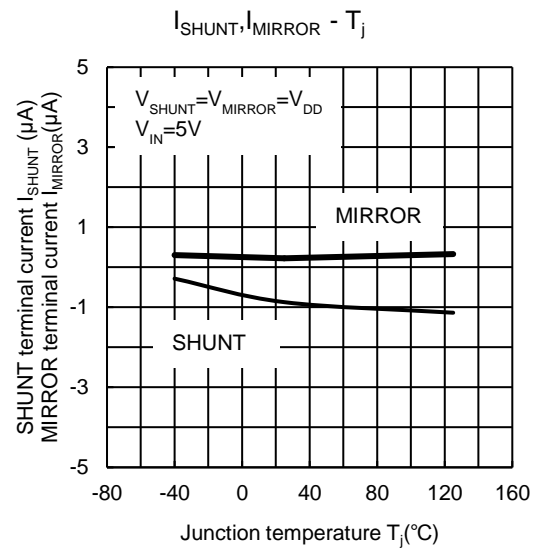
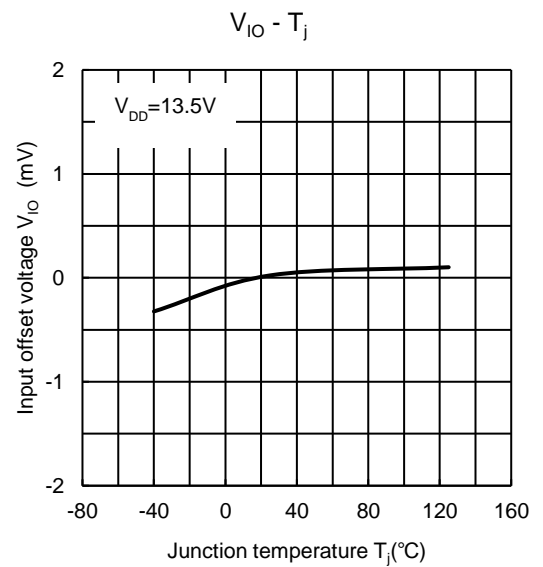
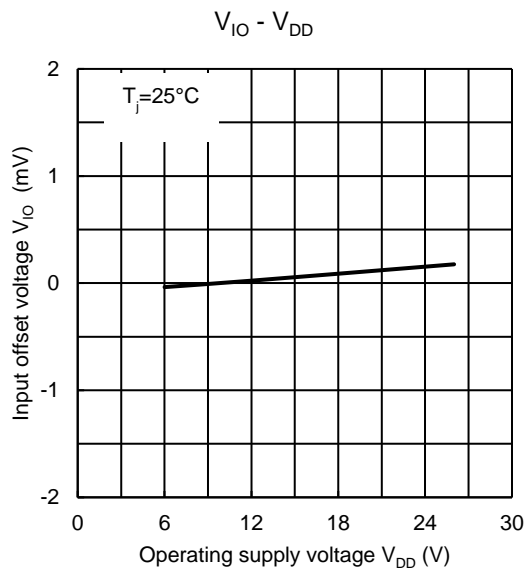
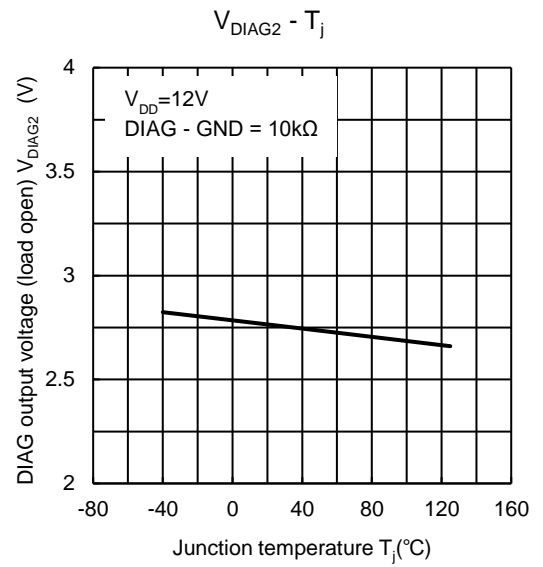
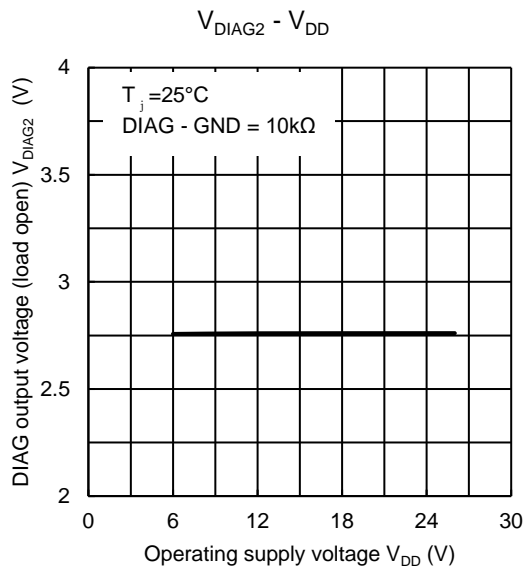


$V_{DIAG1} - V_{DD}$



$V_{DIAG1} - T_j$

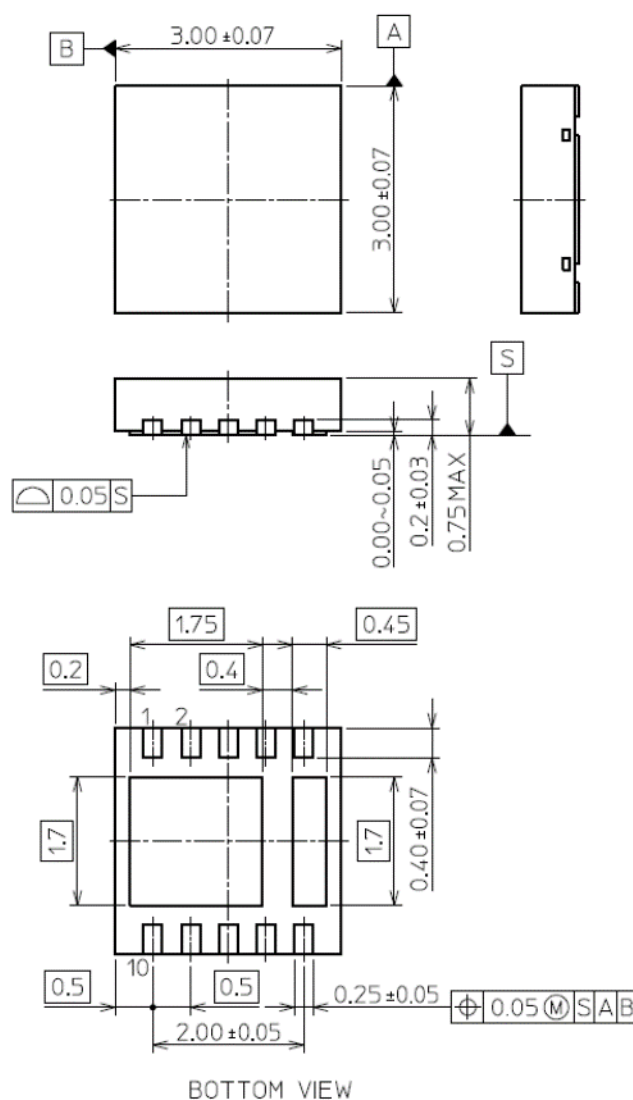




## 13. Package Information

### 13.1. Package Dimensions

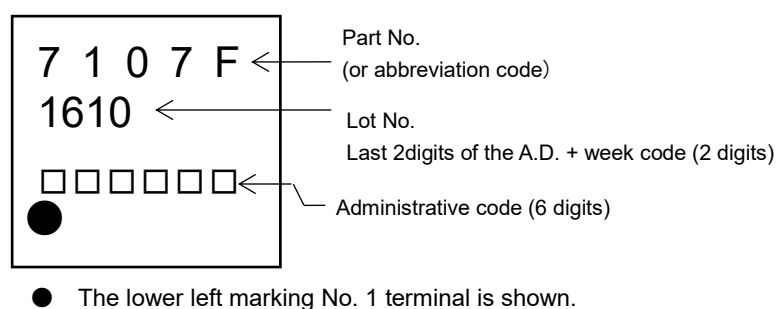
Unit: mm



Weight: 0.02 g (typ.)

Figure 13.1 Package Dimensions

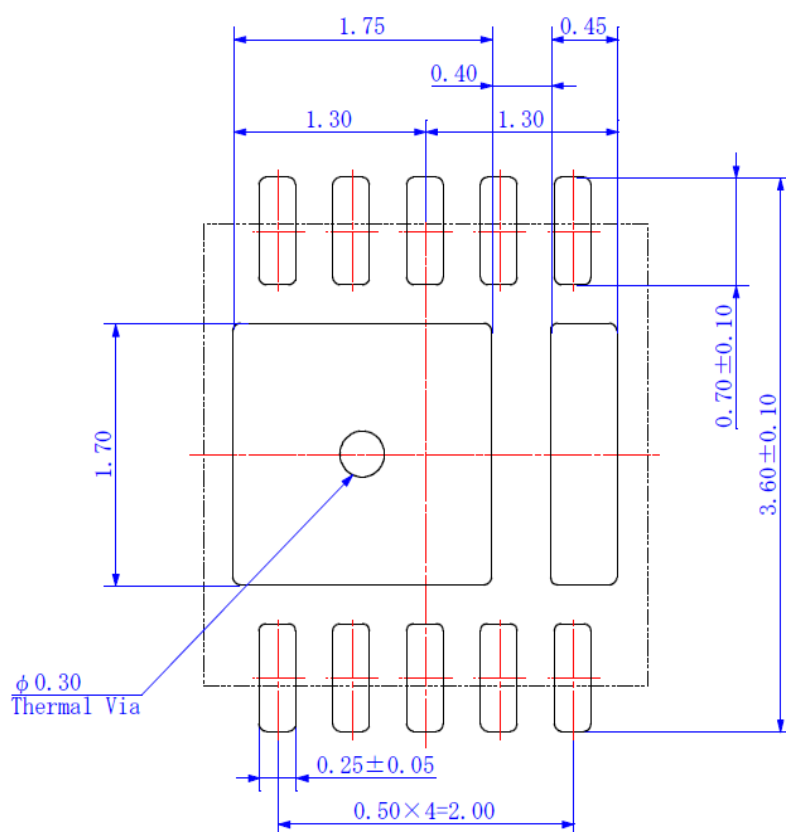
## 13.2. Marking



**Figure 13.2 Marking**

## 13.3. Land Pattern Dimensions for Reference only

Unit: mm



**Figure 13.3 Land Pattern Dimensions for Reference only**



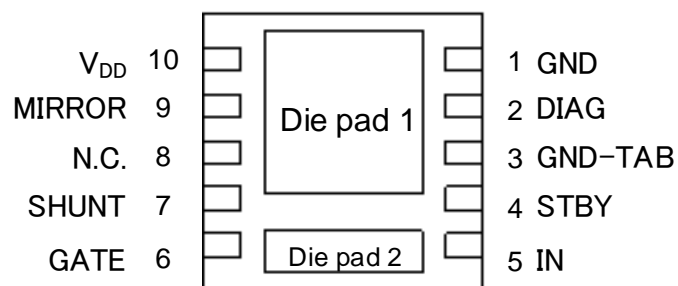
## 14. IC Usage Notes

### 14.1. Notes on Handling of ICs

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.
- (2) The voltage more than current sense voltage or diagnostic output voltage may be outputted to a DIAG output by the injection of a power supply, interception conditions, the input condition to current sense amplifier, etc. Please confirm problem existence by a set in the case of use. Moreover, please give me a measure by a capacitor etc. if needed.

### 14.2. Notes on mounting.

- (1) Please make Die pad 1 into GND and the potential.
- (2) Please make Die pad 2 into SHUNT (7pin) and the potential.



**Figure 14.1 Pin arrange (Bottom View)**

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