TOSHIBA Field Effect Transistor Silicon P-Channel MOS Type (U-MOSⅥ)

TPCC8105

Lithium Ion Battery Applications

Power Management Switch Applications

- Small footprint due to a small and thin package
- Low drain-source ON-resistance:
  $R_{DS\ (ON)}$ = 6.0 mΩ (typ.)(V_{GS} = −10 V)
- Low leakage current: I_{DSS} = −10 μA (max) (V_{DS} = −30 V)
- Enhancement mode: V_{th} = −0.8 to −2.0 V (V_{DS} = −10 V, I_D = −0.5 mA)

Absolute Maximum Ratings (T_a = 25°C)

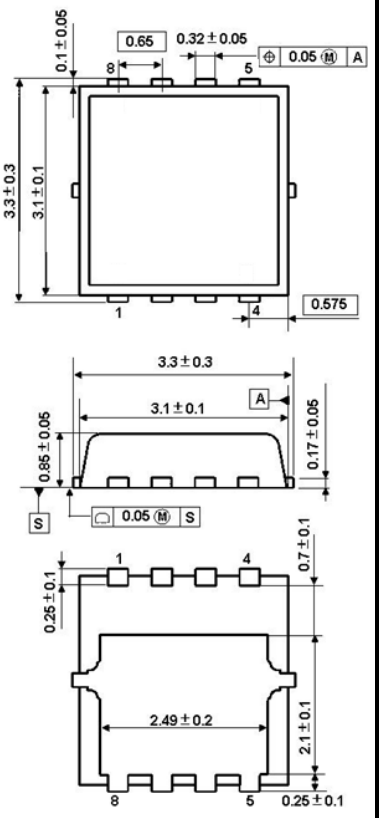
Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	−30	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−30	V
Gate-source voltage		V_{GSS}	−25/+20	V
Drain current	DC (Note 1)	I_D	−23	A
	Pulsed (Note 1)	I_{DP}	−69	
Drain power dissipation (T_c = 25°C)		P_D	30	W
Drain power dissipation (t = 10 s) (Note 2a)		P_D	1.9	W
Drain power dissipation (t = 10 s) (Note 2b)		P_D	0.7	W
Single-pulse avalanche energy (Note 3)		E_{AS}	138	mJ
Avalanche current		I_{AR}	−23	A
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: For Notes 1 to 4, refer to the next page.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.

Unit: mm

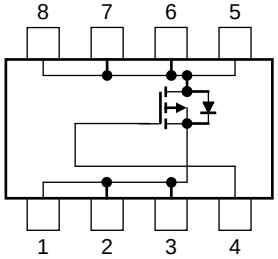


1,2,3 :SOURCE 4:GATE
5,6,7,8:DRAIN

JEDEC	—
JEITA	—
TOSHIBA	2-3X1A

Weight: 0.02 g (typ.)

Circuit Configuration



Start of commercial production
2009-11

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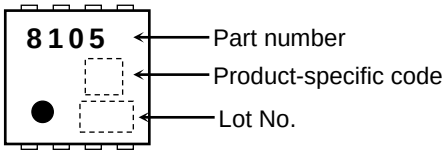
Thermal Characteristics

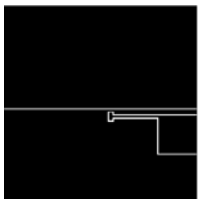
Characteristic	Symbol	Max	Unit
Thermal resistance, channel to case (T_c = 25°C)	$R_{th(ch-c)}$	4.16	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	$R_{th(ch-a)}$	65.7	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	$R_{th(ch-a)}$	178	°C/W

Marking



Note 1: Ensure that the channel temperature does not exceed 150°C.

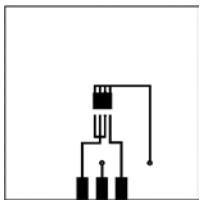
Note 2a: Device mounted on a glass-epoxy board (a)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

glass-epoxy board (a)

Note 2b: Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

glass-epoxy board (b)

Note 3: V_{DD} = −24 V, T_{ch} = 25°C (initial), L = 200 μH, R_G = 1 Ω, I_{AR} = −23 A

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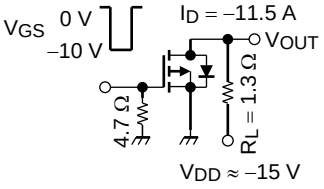
Electrical Characteristics (T_a = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±100	nA
Drain cutoff current		I_{DSS}	V_{DS} = −30 V, V_{GS} = 0 V	—	—	−10	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = −10 mA, V_{GS} = 0 V	−30	—	—	V
		$V_{(BR)DSX}$	I_D = −10 mA, V_{GS} = 10 V (Note 4)	−21	—	—	
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −0.5 mA	−0.8	—	−2.0	V
Drain-source on-resistance		$R_{DS(ON)}$	V_{GS} = −4 .5V, I_D = −11.5 A	—	8	10.4	mΩ
			V_{GS} = −10 V, I_D = −11.5 A	—	6	7.8	
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	3240	—	pF
Reverse transfer capacitance		C_{rss}		—	520	—	
Output capacitance		C_{oss}		—	580	—	
Switching time	Rise time	t_r		—	8	—	ns
	Turn-on time	t_{on}		—	14	—	
	Fall time	t_f		—	110	—	
	Turn-off time	t_{off}	Duty ≤ 1%, t_w = 10 μs	—	330	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ −24 V, V_{GS} = −10 V, I_D = −23 A	—	76	—	nC
Gate-source charge 1		Q_{gs1}		—	7.6	—	
Gate-drain (“Miller”) charge		Q_{gd}		—	20	—	

Source-Drain Ratings and Characteristics (T_a = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	−69	A
Forward voltage (diode)		V_{DSF}	I_{DR} = −23 A, V_{GS} = 0 V	—	—	1.2	V

Note 4: V_{DSX} mode (the application of a plus voltage between gate and source) may cause decrease in maximum rating of drain-source voltage.

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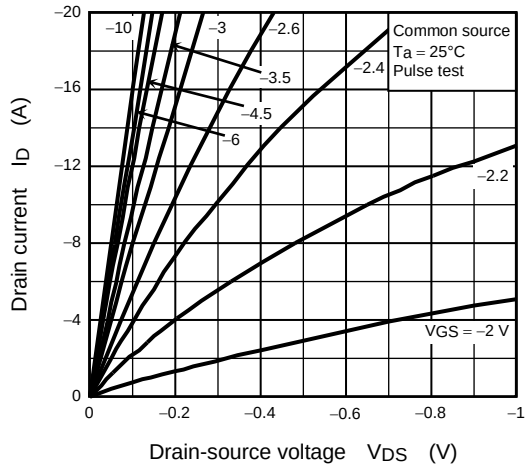
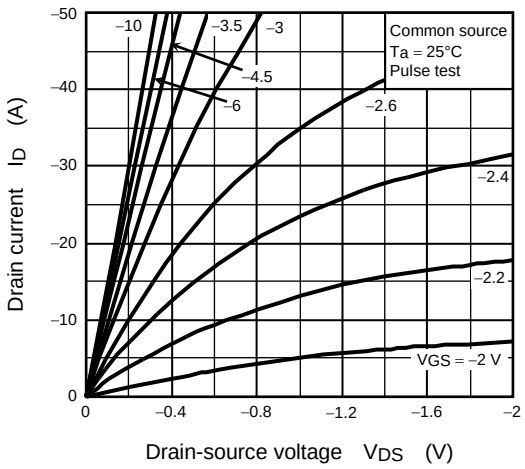
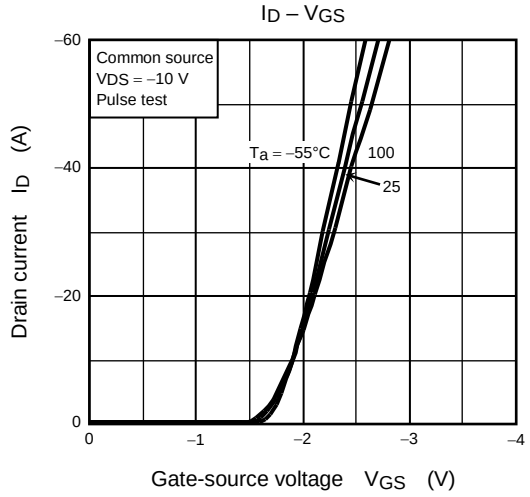
$I_D - V_{DS}$



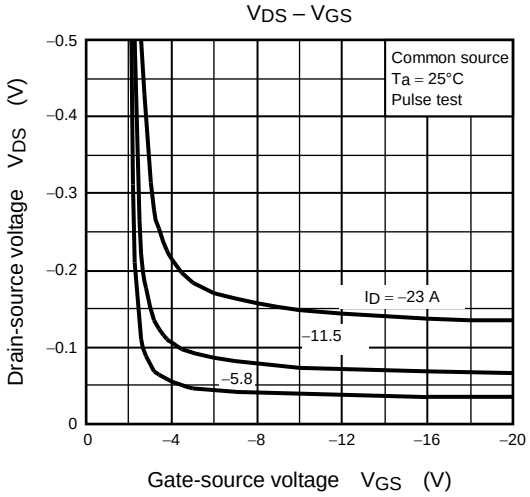
$I_D - V_{DS}$



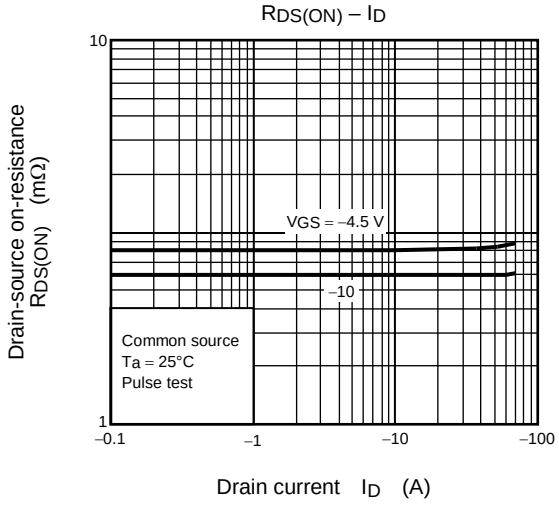
$I_D - V_{GS}$



$V_{DS} - V_{GS}$



$R_{DS(ON)} - I_D$



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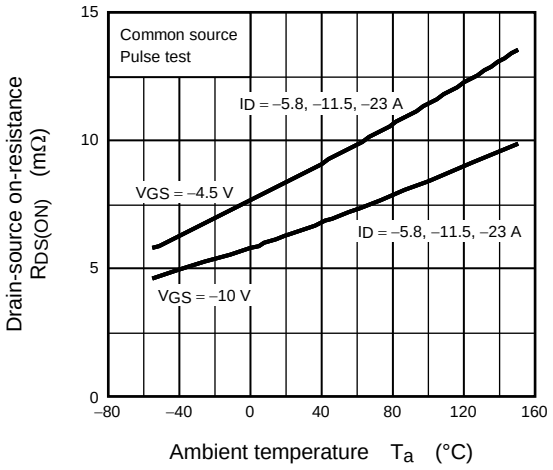
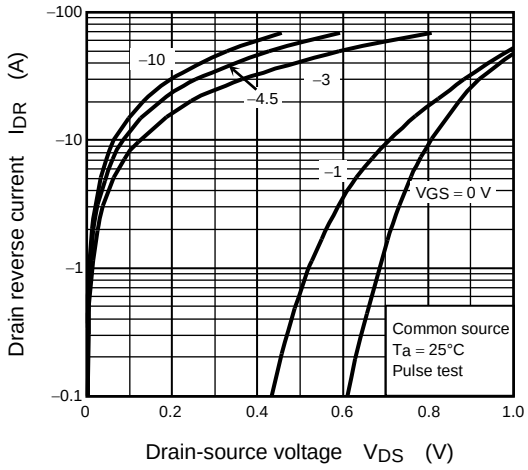
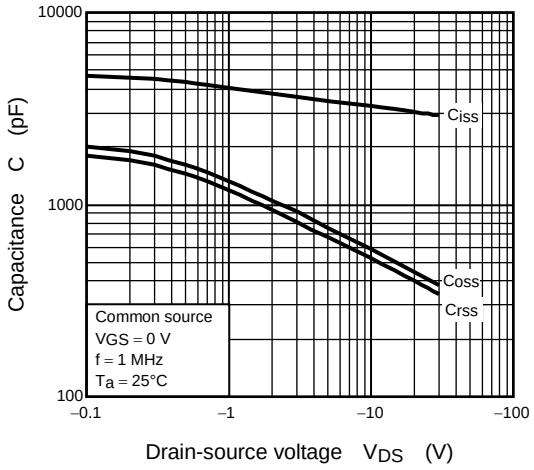
$R_{DS(ON)}$ – T_a



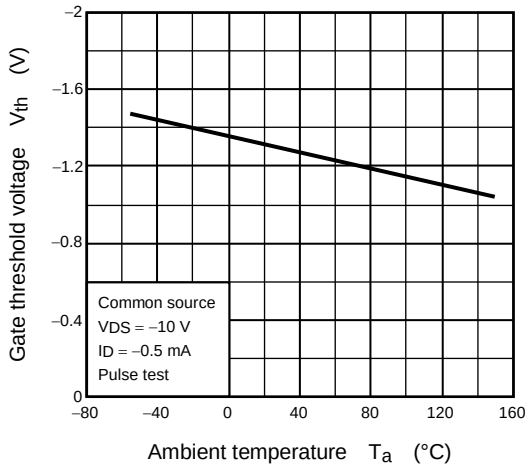
I_{DR} – V_{DS}



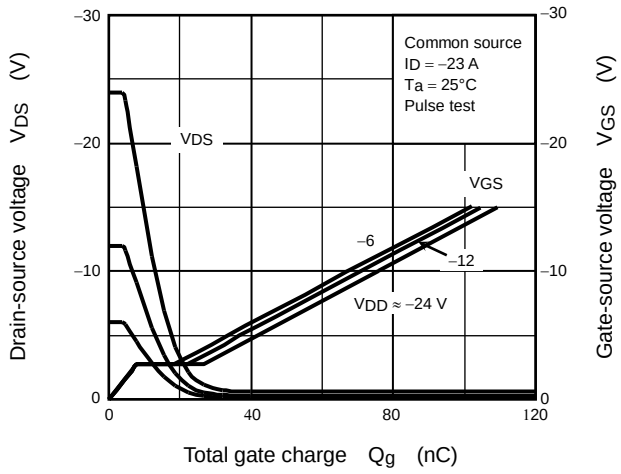
Capacitance – V_{DS}



V_{th} – T_a



Dynamic input/output characteristics



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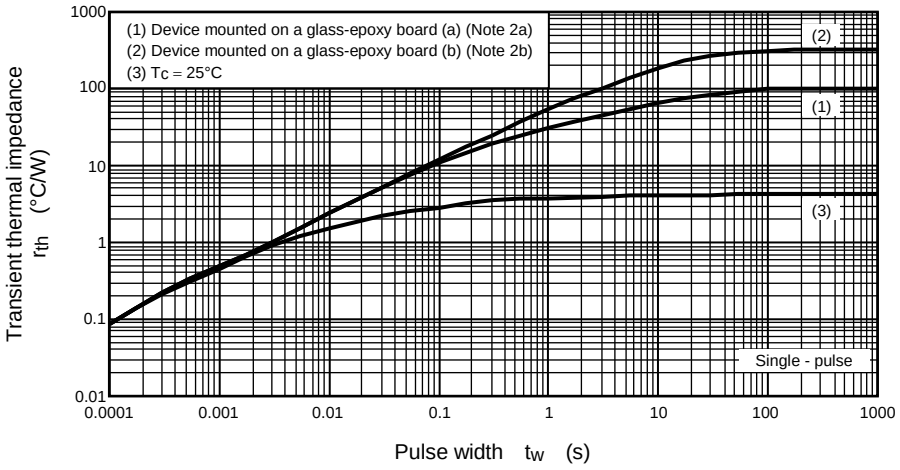
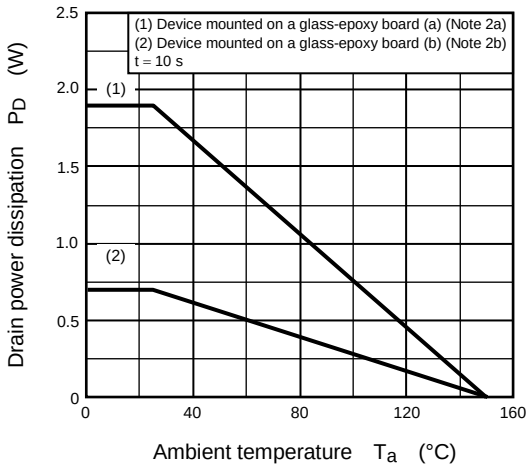
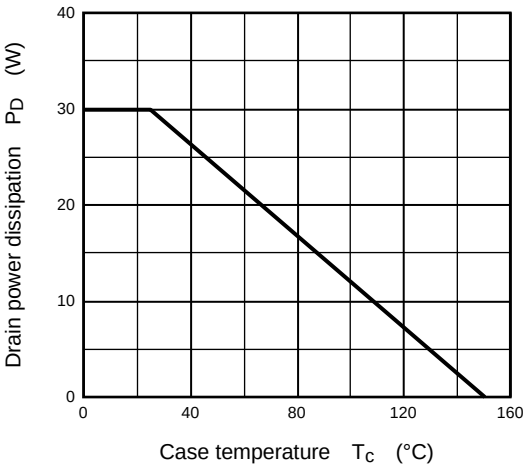
$r_{th} - t_w$



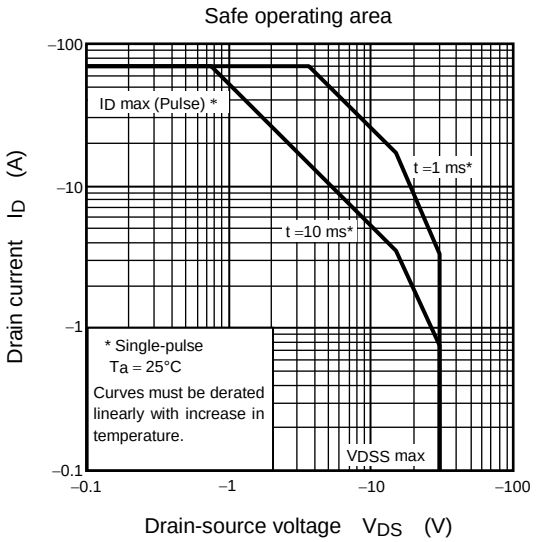
$P_D - T_a$



$P_D - T_c$



Safe operating area



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