TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOS VI)

TPCA8128

Lithium Ion Battery Applications Power Management Switch Applications

- Small footprint due to compact and slim package
- Low drain-source ON resistance : RDS (ON) = 3.7 m Ω (typ.)
- Low leakage current : $I_{DSS} = -10 \mu A \text{ (max) (V}_{DS} = -30 \text{ V)}$
- Enhancement mode

: $V_{th} = -0.8 \text{ to } -2.0 \text{ V } (V_{DS} = -10 \text{ V}, I_D = -0.5 \text{ m A})$

Absolute Maximum Ratings (Ta = 25°C)

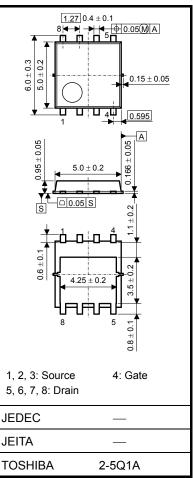
Characteristics			Symbol	Rating	Unit	
Drain-source voltage			V_{DSS}	-30	V	
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)			V_{DGR}	-30	V	
Gate-source v	Gate-source voltage			-25/+20	V	
Drain current	DC	(Note 1)	ID	-34	Α	
Diam current	Pulse	(Note 1)	I _{DP}	-102	A	
Drain power dissipation (Tc = 25°C)			P _D	45	W	
Drain power dissipation (t = 10 s) (Note 2a)			P _D	2.8		
Drain power dissipation (t = 10 s) (Note 2b)			P _D	1.6		
Single pulse avalanche energy (Note 3)			E _{AS}	150	mJ	
Avalanche current			I _{AR}	-34	Α	
Channel temperature			T _{ch}	150	°C	
Storage temperature range			T _{stg}	-55 to 150	°C	

Note: For (Note 1), (Note 2), (Note 3), refer to the next page.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

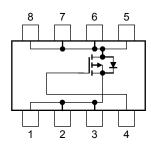
This transistor is an electrostatic-sensitive device. Handle with caution.

Unit: mm



Weight: 0.076 g (typ.)

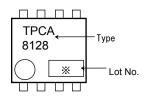
Circuit Configuration



Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case (Tc = 25 °C)	R _{th (ch-c)}	2.78	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	R _{th (ch-a)}	44.6	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	R _{th (ch-a)}	78.1	C/VV

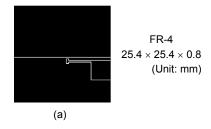
Marking (Note 4)

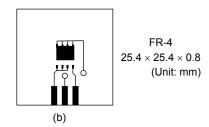


Note 1: The channel temperature should not exceed 150°C during use.

Note 2: (a) Device mounted on a glass-epoxy board (a)

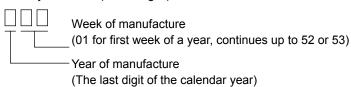
(b) Device mounted on a glass-epoxy board (b)





Note 3: $V_{DD} = -24~V,~T_{ch} = 25^{\circ}C$ (initial), L = 100 $\mu H,~R_{G} = 25~\Omega,~I_{AR} = -34~A$

Note 4: * Weekly code: (Three digits)



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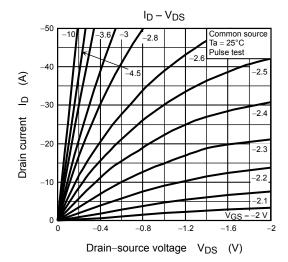
Electrical Characteristics (Ta = 25°C)

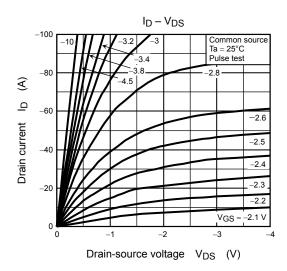
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage curi	rent	I _{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±100	nA
Drain cut-off curre			_	-10	μА		
Drain-source breakdown voltage		V _{(BR)DSS}	$I_D = -10 \text{ mA}, V_{GS} = 0 \text{ V}$	-30	_	_	V
		V _{(BR)DSX}	$I_D = -10 \text{ mA}, V_{GS} = 10 \text{ V (Note 5)}$	-21	_	_	
Gate threshold vo	ltage	V _{th}	$V_{DS} = -10 \text{ V}, I_{D} = -0.5 \text{mA}$	-0.8	_	-2.0	V
Drain-source ON resistance		D	$V_{GS} = -4.5 \text{ V}, I_D = -17 \text{ A}$		5.1	6.7	mΩ
Dialii-source ON	resistance	R _{DS} (ON)	V _{GS} = -10 V, I _D = -17 A	_	3.7	4.8	1115.2
Input capacitance		C _{iss}		_	4800	_	pF
Reverse transfer capacitance		C _{rss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	_	800	_	
Output capacitance		C _{oss}			900	_	
Switching time	Rise time	t _r	V _{GS} ₋₁₀ V		11	_	- ns
	Turn-on time	t _{on}		_	21	_	
	Fall time	t _f		_	135	_	
	Turn-off time	t _{off}	Duty \leq 1%, $t_W = 10 \mu s$		390	_	
Total gate charge (gate-source plus gate-drain)		Qg	V _{DD} ≈ -24 V, V _{GS} = -10 V	_	115	_	
Gate-source charge 1		Q _{gs1}	I _D = -34 A	_	11	_	nC
Gate-drain ("Miller") charge		Q _{gd}		_	30	_	

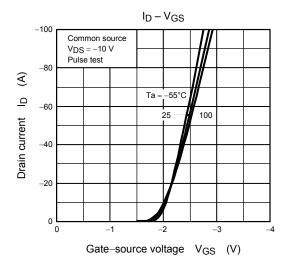
Source-Drain Ratings and Characteristics (Ta = 25°C)

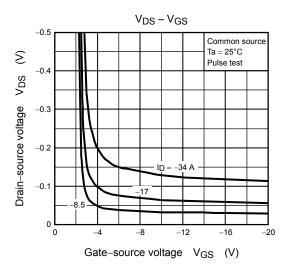
Characterist	ics	Symbol	Test Condition	Min	Тур.	Max	Unit
Drain reverse current	Pulse (Note 1)	I _{DRP}	_	_	_	-102	Α
Forward voltage (diode)		V_{DSF}	$I_{DR} = -34 \text{ A}, V_{GS} = 0 \text{ V}$	_	_	1.2	V

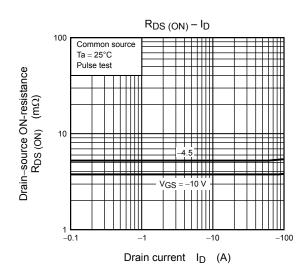
Note 5: V_{DSX} mode (the application of a plus voltage between gate and source) may cause decrease in maximum rating of drain-source voltage.



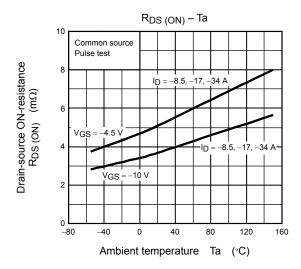


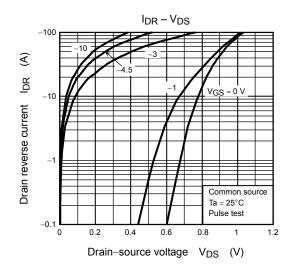


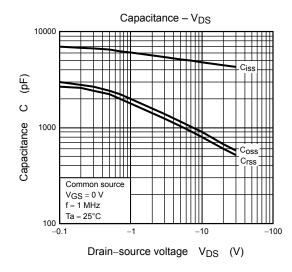


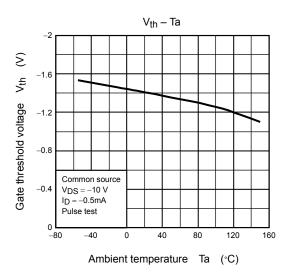


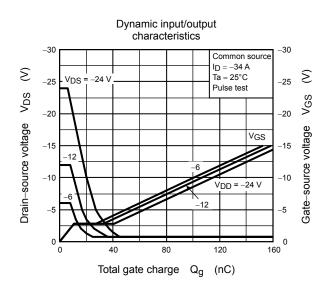
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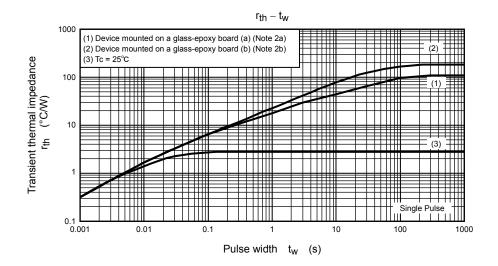


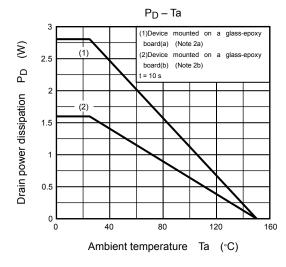


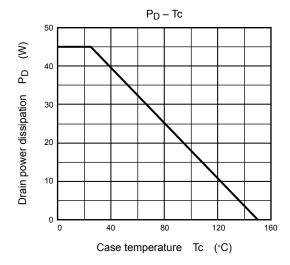


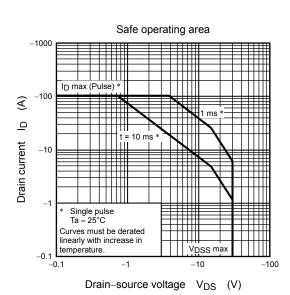












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