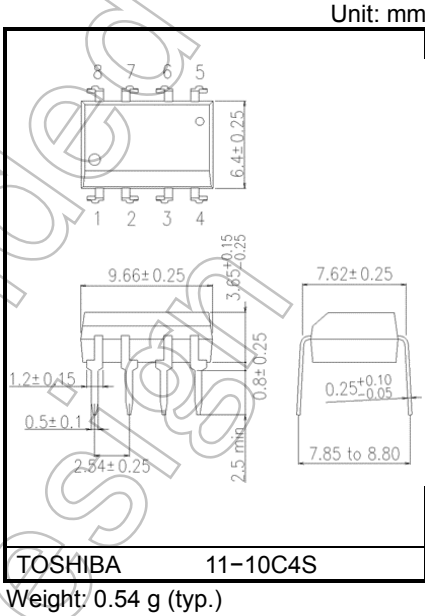


TLP2630

Digital Logic Isolation
Tele-Communication
Analog Data Equipment Control
Microprocessor System Interface

The TOSHIBA TLP2630 dual photocoupler consists of a pair of infrared emitting diode and integrated high gain, high speed photodetector.
The output of the detector circuit is an open collector, Schottky clamped transistor. This unit is 8-lead DIP.

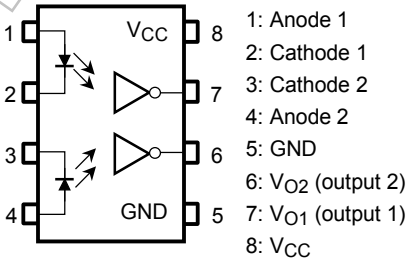
- Input current threshold: $I_F = 5\text{ mA}$ (max)
- Switching speed: 10MBd
- Guaranteed performance over temperature: 0 to 70°C
- Isolation voltage: 2500 V_{rms} (min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A
File No.E67349



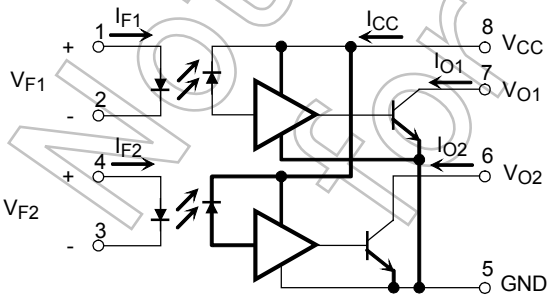
Truth Table
(positive logic)

Input	Output
H	L
L	H

Pin Configuration (top view)



Schematic



Note: A 0.1 μ F bypass capacitor must be connected between pins 8 and 5 (see Note 1).

Start of commercial production
1986-03

Absolute Maximum Ratings (no derating required up to 70°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current(each channel)	I_F	20	mA
	Pulse forward current (each channel)*	I_{FP}	30	mA
	Reverse voltage(each channel)	V_R	5	V
	Input power dissipation(each channel)	P_D	25	mW
	Input power dissipation derating ($T_a \geq 70^\circ\text{C}$) (each channel)	$\Delta P_D/^\circ\text{C}$	-0.45	mW/ $^\circ\text{C}$
Detector	Output current(each channel)	I_O	16	mA
	Output voltage(each channel)	V_O	-0.5 to 7	V
	Supply voltage (1 minute maximum)	V_{CC}	7	V
	Output power dissipation(each channel)	P_O	40	mW
	Output power dissipation derating ($T_a \geq 70^\circ\text{C}$) (each channel)	$\Delta P_O/^\circ\text{C}$	-0.75	mW/ $^\circ\text{C}$
Operating temperature range		T_{stg}	-55 to 125	$^\circ\text{C}$
Storage temperature range		T_{opr}	-40 to 85	$^\circ\text{C}$
Lead soldering temperature (10 s) (Note 1)		T_{sol}	260	$^\circ\text{C}$
Isolation voltage (AC, 60 s, R.H. $\leq 60\%$, Note 3)		BV_S	2500	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

* $t \leq 1$ ms duration.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Input current, low level, each channel	I_{FL}	0	—	250	μA
Input current, high level, each channel	I_{FH}	6.3*	—	20	mA
Supply voltage**	V_{CC}	4.5	5	5.5	V
Fan out(TTL load, each channel)	N	—	—	8	—
Operating temperature	T_{opr}	0	—	70	$^\circ\text{C}$

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

* 6.3 mA is a guard banded value which allows for at least 20 % CTR degradation.
Initial input current threshold value is 5 mA or less.

**This item denotes operating ranges, not meaning of recommended operating conditions.

Electrical Characteristics (Ta = 0~70°C, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ.*	Max	Unit
Input forward voltage (each channel)	V _F	I _F = 10 mA, Ta = 25 °C	—	1.65	1.75	V
Input diode temperature coefficient(each channel)	ΔV _F / ΔTa	I _F = 10 mA	—	-2.0	—	mV / °C
Input reverse breakdown voltage(each channel)	BV _R	I _R = 10 μA, Ta = 25 °C	5	—	—	V
Input capacitance (each channel)	C _T	V _F = 0 V, f = 1 MHz	—	45	—	pF
High level output current (each channel)	I _{OH}	V _{CC} = 5.5 V, V _O = 5.5 V I _F = 250 μA	—	1	250	μA
Low level output voltage (each channel)	V _{OL}	V _{CC} = 5.5 V, I _F = 5 mA I _{OL} (sinking) = 13 mA	—	0.4	0.6	V
High level supply current (both channels)	I _{CCH}	V _{CC} = 5.5 V, I _F = 0 mA	—	14	30	mA
Low level supply current (both channels)	I _{CCL}	V _{CC} = 5.5 V, I _F = 10 mA	—	24	36	mA
Isolation resistance	R _S	V _S = 500 V, R.H. ≤ 60 % (Note 3)	—	10 ¹⁴	—	Ω
Capacitance (input-output)	C _S	f = 1 MHz (Note 3)	—	0.6	—	pF
Input-input leakage current	I _{I-I}	R.H. ≤ 60 %, t = 5 s V _{I-I} = 500 V (Note 6)	—	0.005	—	μA
Resistance (input-input)	R _{I-I}	V _{I-I} = 500 V (Note 6)	—	10 ¹¹	—	Ω
Capacitance (input-input)	C _{I-I}	f = 1 MHz (Note 6)	—	0.25	—	pF

* All typical values are at V_{CC} = 5 V, Ta = 25 °C.

Switching Characteristics (Ta =25°C , Vcc=5V)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time to low output level	t_{pHL}	1	$I_F = 0 \rightarrow 7.5 \text{ mA}$, $R_L = 350 \Omega$ $C_L = 15 \text{ pF}$ (each channel)	—	60	75	ns
Propagation delay time to high output level	t_{pLH}	1	$I_F = 7.5 \rightarrow 0 \text{ mA}$, $R_L = 350 \Omega$ $C_L = 15 \text{ pF}$ (each channel)	—	60	75	ns
Output rise a time,output fall time(10~90%)	t_r, t_f	1	$I_F = 0 \rightarrow 7.5 \text{ mA}$, $R_L = 350 \Omega$ $C_L = 15 \text{ pF}$ (each channel)	—	30	—	ns
Common mode transient immunity at high output level	CM_H	2	$I_F = 0 \text{ mA}$, $R_L = 350 \Omega$ $V_{CM} = 200 \text{ V}$ $V_{O(min)} = 2 \text{ V}$ (each channel, Note 4)	—	200	—	V / μs
Common mode transient immunity at low output level	CM_L	2	$I_F = 7.5 \text{ mA}$, $R_L = 350 \Omega$ $V_{CM} = 200 \text{ V}$ $V_{O(max)} = 0.8 \text{ V}$ (each channel, Note 5)	—	—500	—	V / μs

(Note 1) 2 mm below seating plane.

(Note 2) The VCC supply voltage to each TLP2630 isolator must be bypassed by a 0.1 μF capacitor. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package VCC and GND pins each device.

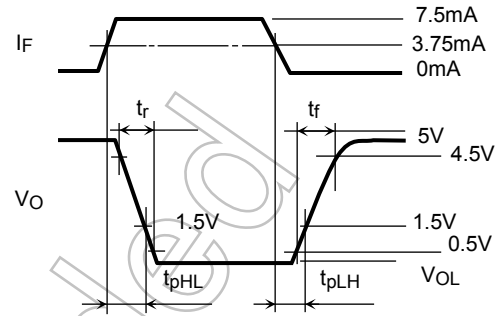
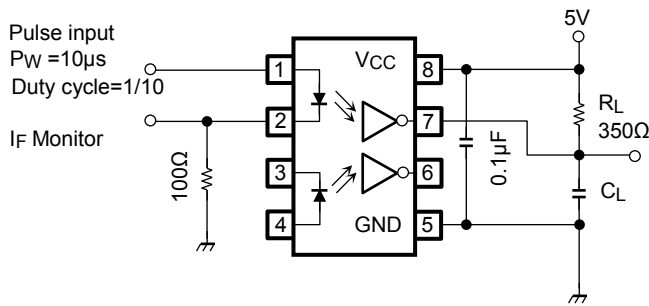
(Note 3) Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

(Note 4) CM_H the maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state(i.e. $V_{OUT} > 2.0 \text{ V}$) Measured in volts per microsecond(V / μs).

(Note 5) CM_L the maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state(i.e. $V_{OUT} < 0.8 \text{ V}$) Measured in volts per microsecond(V / μs).

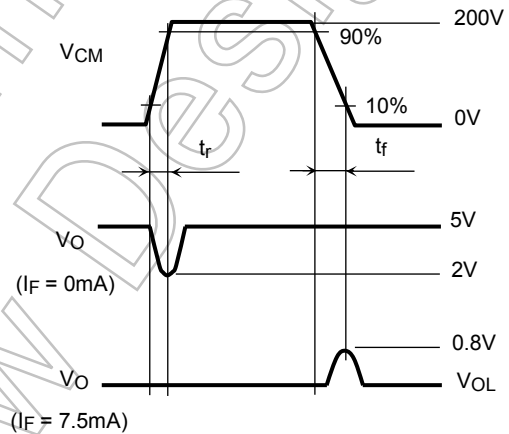
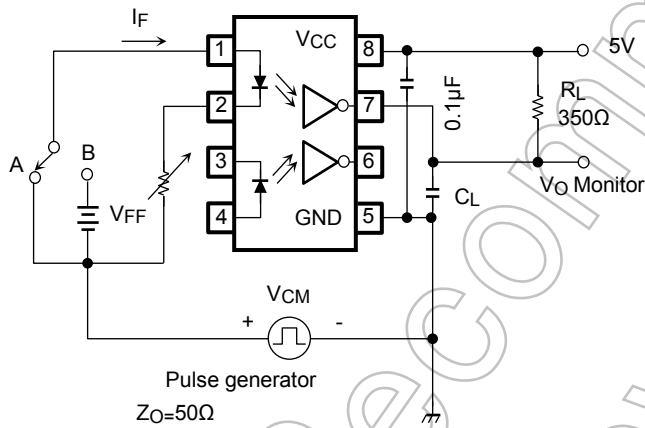
(Note 6) Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

Test Circuit 1. t_{pHL} and t_{pLH}



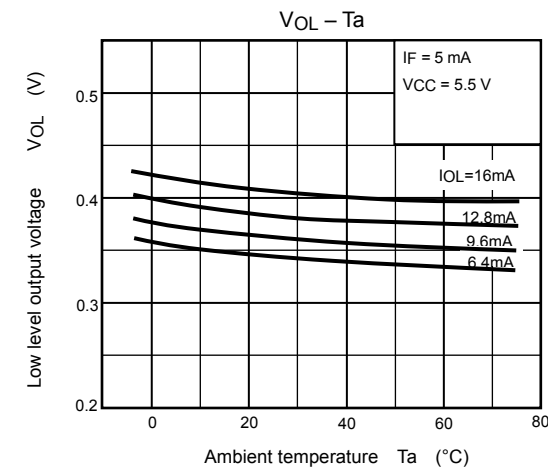
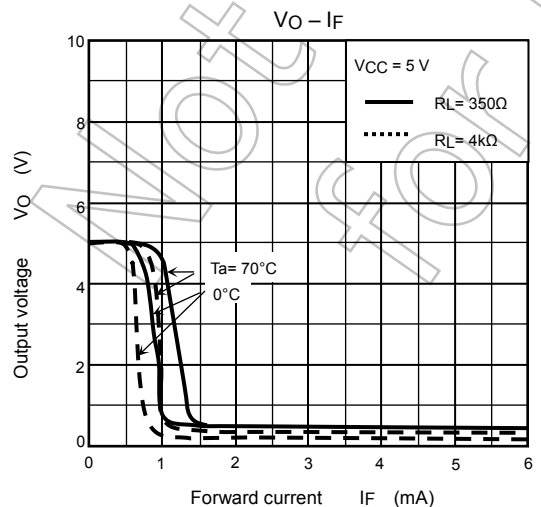
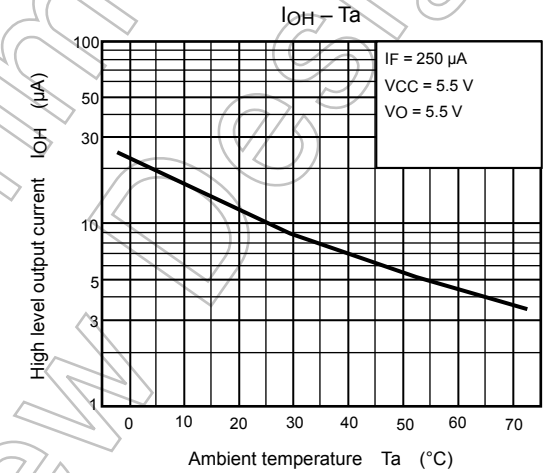
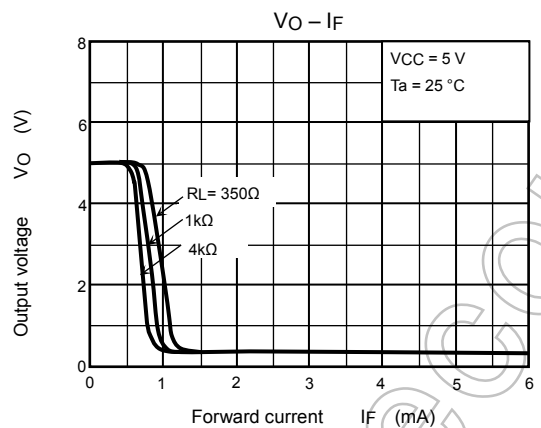
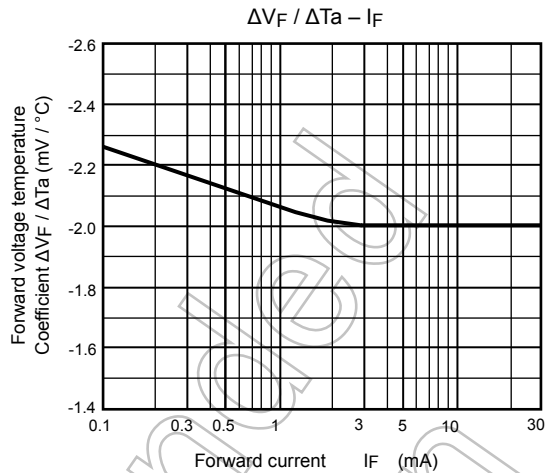
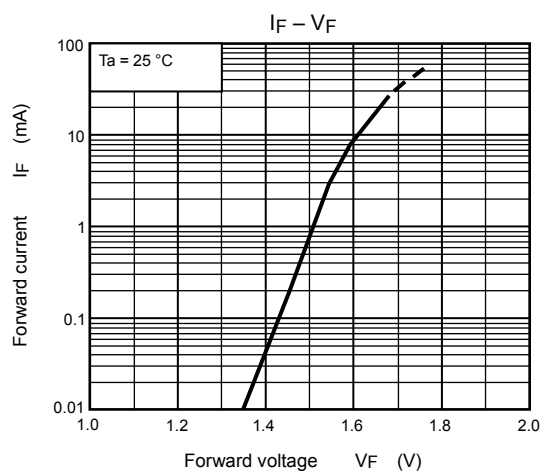
* C_L is approximately 15pF which includes probe and stray wiring capacitance.

Test Circuit 2. Transient Immunity and Typical Waveforms

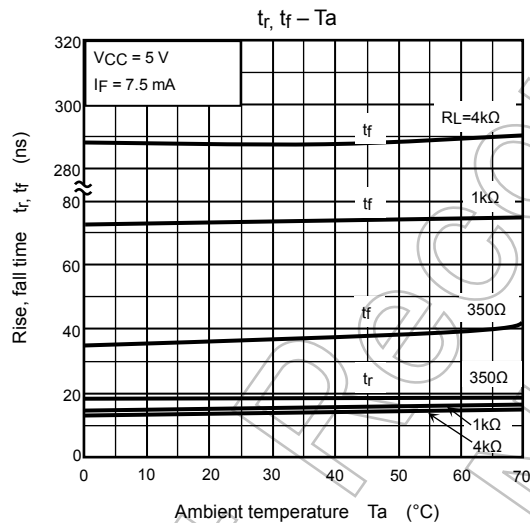
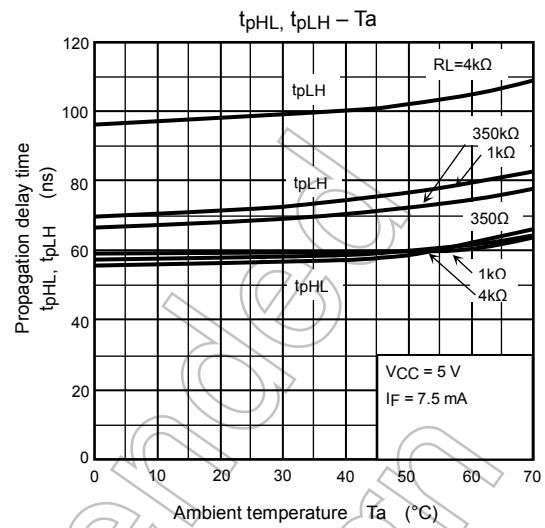
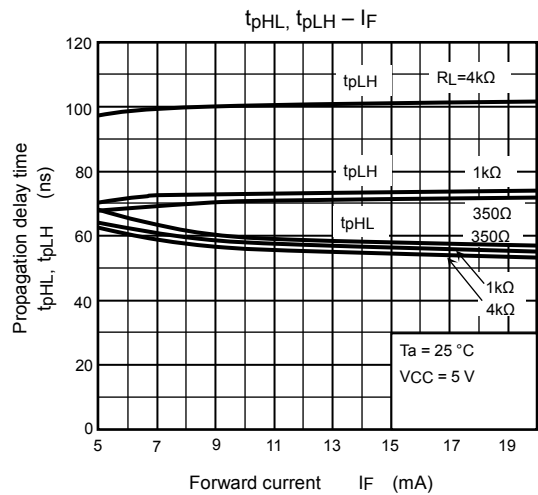


$$CM_H = \frac{160(V)}{t_r(\mu s)}, CM_L = \frac{160(V)}{t_f(\mu s)}$$

* C_L is approximately 15pF which includes probe and stray wiring capacitance.



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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