Unit: mm

6.0±0.2

11-5K1S

TOSHIBA PHOTOCOUPLER IRED & PHOTO-IC

TLP2418

PDP (Plasma Display Panel)

FA (Factory Automation)

Interfaces of measuring and control instruments Operate at high ambient temperatures up to 125°C

The Toshiba TLP2418 consists of an infrared emitting diode and integrated high-gain, high-speed photodetector.

The TLP2418 is housed in the SO8 package. The output stage is an open collector type.

The photodetector has an internal Faraday shield that provides a guaranteed common-mode transient immunity of ±15 kV/µs.

• Inverter logic type (Open collector output)

Package: SO8

Guaranteed performance over: -40 to 125°C

Power supply voltage: 4.5 to 5.5 V

Input threshold current: I_{FHL} = 5.0 mA (max)

Propagation delay time t_{pHL}/t_{pLH}: 75 ns (max)

Common-mode transient immunity: ±15 kV/μs (min)

Isolation voltage: 3750 Vrms (min)

• UL-recognized: UL 1577, File No.E67349

cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349

VDE-approved: EN 60747-5-5 (Note 1)

• CQC-approved: GB4943.1,GB8898 Japan Factory

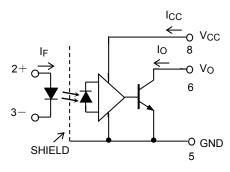


Note 1: When a VDE approved type is needed, please designate the Option (V4).

Truth Table

Input	LED	Output
H	ON	L
J	OEF	Η /

Schematic



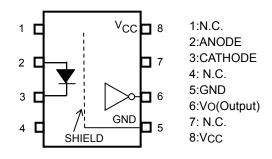
Pin Configuration (Top View)

0.38±0.1 1.27±0.15

JEDEC JEITA

TOSHIBA

Weight: 0.11 g (typ.)



A bypass capacitor of 0.1µF must be connected between pins 5 and 8.

Start of commercial production 2009-11

Absolute Maximum Ratings (Ta=25°C)

	Characteristic	Symbol	Rating	Unit
	Forward Current	lF	25	mA
	Forward Current Derating (Ta ≥ 110°C)	ΔI _F /°C	-0.67	mA/°C
	Peak Transient Forward Current (Note	1) I _{FPT}	50	mA
	Peak Transient Forward Current Derating (Ta ≥ 110°C)	ΔI _{FPT} /°C	-1.34	mA/°C
	Reverse Voltage	VR	5	V
	Input Power Dissipation	PD	40	mW
	Input Power Dissipation Derating (Ta ≥ 110°C)	ΔP _D /°C	-1.08	/mW/°C
	Output Current (Ta ≤ 125°C)	lo	25	/mA
tor	Output Voltage	Vo	6	V
Detector	Supply Voltage	V _{CC}	6	V
Ŏ	Output Power Dissipation	Po	80	mW /
	Output Power Dissipation Derating (Ta ≥ 110°C)	ΔP _O /°C	-2.0	mW/°C
Opera	ating Temperature Range	Topr	-40 to 125	°C
Stora	ge Temperature Range	T _{stg}	-55 to 150	(6)
Lead	Soldering Temperature (10 s)	Tsol	260	√°¢ ¬
Isolat	ion Voltage (AC, 60 s, R.H. ≤ 60 %) (Note	2) BVs	3750	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width \leq 1 ms, duty = 50 %.

Note 2: This device is regarded as a two terminal device: pins 1, 2, 3 and 4 are shorted together, as are pins 5, 6, 7 and 8.

Recommended Operating Conditions

Characteristic	Symbol	Min	Тур.	Max	Unit
Input Current, High Level	IFH	7.5	1	15	mA
Input Voltage, Low Level	V _{FL}	0	1	0.8	V
Supply Voltage*	Vcc	4.5	-	5.5	٧
Operating Temperature	Topr	-40	_	125	°C

^{*} This item denotes operating range, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.



Electrical Characteristics (Unless otherwise specified, Ta=-40 to 125°C, V_{CC}=4.5 to 5.5 V)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Input Forward Voltage	VF	-	I _F = 10 mA, Ta = 25 °C	1.40	1.57	1.80	٧
Temperature Coefficient of Forward Voltage	ΔV _F /ΔTa	-	I _F = 10 mA	1	-1.8	-	mV/°C
Input Reverse Current	IR	-	V _R = 5 V, Ta = 25 °C)\ <u>></u>	10	μА
Input Capacitance	CT	-	V = 0 V, f = 1 MHz, Ta = 25 °C	770	60	-	pF
Lania High Code d Company		4	V _F = 0.8 V, V _O = 5.5 V)	-	250	
Logic High Output Current	loh	1	Ta = 25 ℃	>-	0.5	10	μА
Logic Low Output Voltage	V _{OL}	2	I _F = 10 mA, I _O = 13 mA (Sinking)) -	0.2	0.6	٧
Logic Low Supply Current	ICCL	3	IF = 10 mA	-	1.5	5	mA
Logic High Supply Current	Іссн	4	I _F = 0 mA	- /	1.5	5	mA
"H Level Output to L Level Output" Input Current	I _{FHL}	-	I _O = 13 mA (Sinking), V _O < 0.6 V		1.0	5.0	mA

^{*}All typical values are at Ta=25°C, V_{CC}=5 V unless otherwise specified

Isolation Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Capacitance input to output	(C _S	V _S = 0 V,f = 1 MHz (Note 2)	_	0.8	_	pF
Isolation resistance	Rs	R.H. ≤ 60 %,V _S = 500 V (Note 2)	1×10 ¹²	10 ¹⁴	_	Ω
Isolation voltage	BVs	AC, 60 s (Note 2)	3750	ı	_	V _{rms}



Switching Characteristics

(Unless otherwise specified, Ta=-40 to 125 °C, Vcc=4.5 to 5.5V)

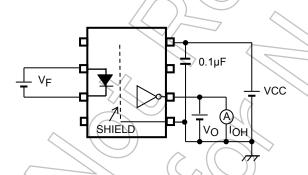
Characteristic	Symbol	Test Circuit	Test Cor	ndition	Min	Тур.	Max	Unit
Propagation delay time (H→L)	t _{pHL}		I _F = 0→7.5 mA	$R_L = 350 \Omega$ $C_L = 15 pF$		30	75	ns
Propagation delay time (L→H)	t _{pLH}		I _F = 7.5→0 mA	(Note 4)	-	35	75	ns
Switching Time Dispersion between ON and OFF	t _{pHL} - t _{pLH}	5	5 I _F = 0 ≠ 7.5 mA C _L	$R_L = 350 \Omega$, $C_L = 15 pF$			35	ns
Propagation Delay Skew (Note 5)	t _{psk}			(Note 4)	-50	-	50	ns
Fall Time (90 – 10 %)	t _f		I _F = 0→7.5 mA	$R_L = 350 \Omega$ $C_L = 15 pF$)	30	-	ns
Rise Time (10 – 90 %)	t _r		I _F = 7.5→0 mA	(Note 4)	J -	30	-	ns
Common Mode transient Immunity at High Level Output	СМн		$V_{CM} = 1000 V_{p-p},$ $V_{CC} = 5 V, Ta = 2$		15		// ¹ /	kV/μs
Common Mode transient Immunity at Low Level Output	CML	6	V _{CM} = 1000 V _{p-p,} V _{CC} = 5 V, Ta = 2	/ / /	\15	9)//) -	kV/μs

^{*}All typical values are at Ta = 25 °C

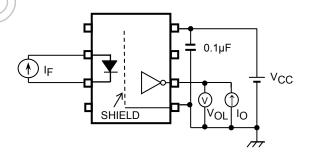
- Note 3: A ceramic capacitor $(0.1 \ \mu F)$ should be connected from pin 8 (VCC) to pin 5 (GND) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.
- Note 4: f = 5 MHz, duty = 50 %, input current tr = tf = less than 5 ns,

 CL is approximately 15 pF which includes probe and Jig/stray wiring capacitance.
- Note 5: Propagation delay skew is defined as the difference between the largest and smallest propagation delay times (i.e. tpHL or tpLH) of multiple samples. Evaluations of these samples are conducted under identical test conditions (supply voltage, input current, temperature, etc).

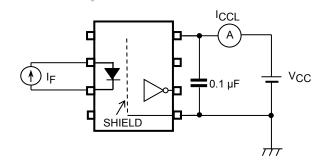
TEST CIRCUIT 1: IOH Test Circuit



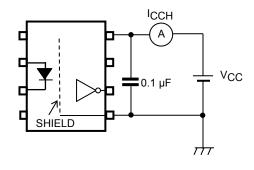
TEST CIRCUIT 2: VOL Test Circuit



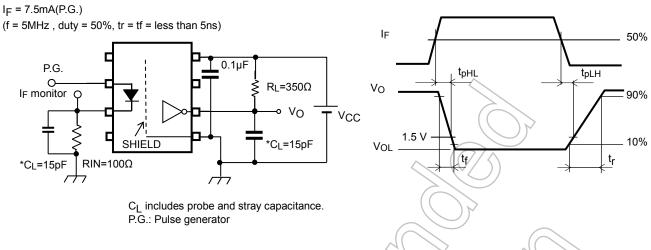
TEST CIRCUIT 3: ICCL Test Circuit



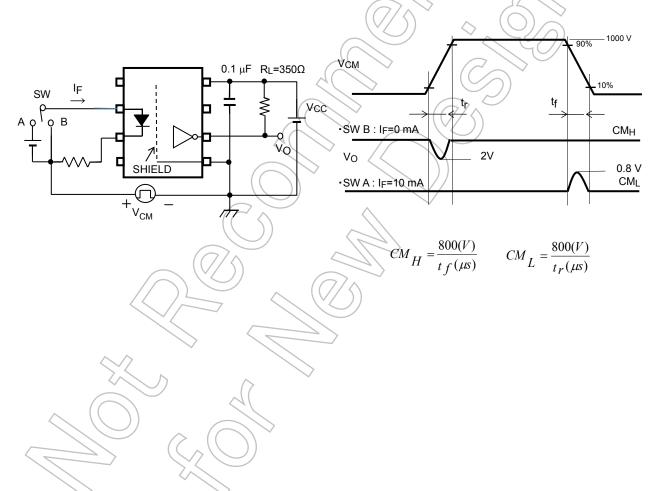
TEST CIRCUIT 4: ICCH Test Circuit

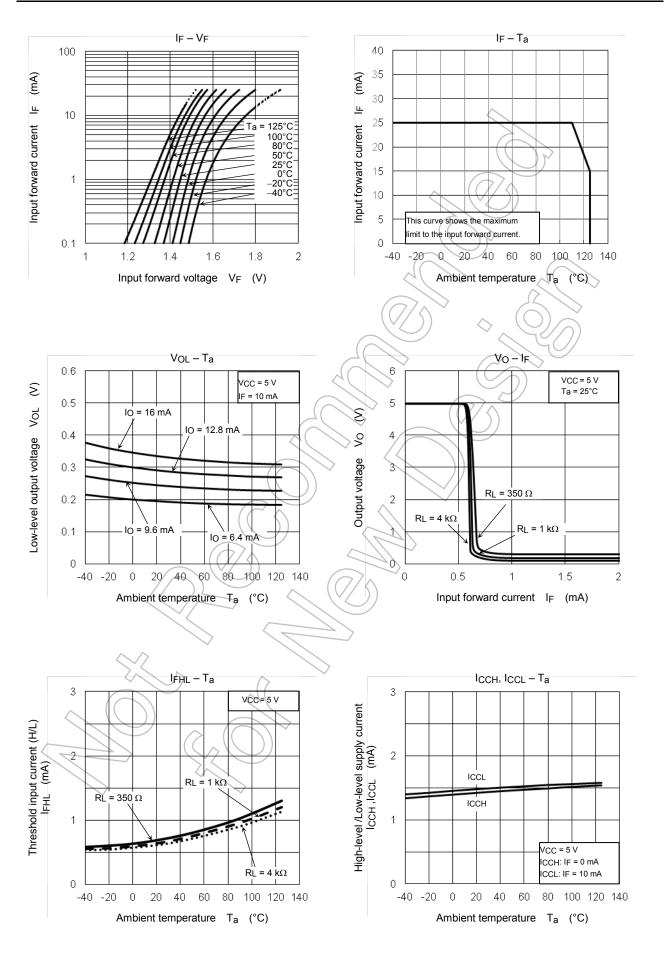


TEST CIRCUIT 5: Switching Time Test Circuit

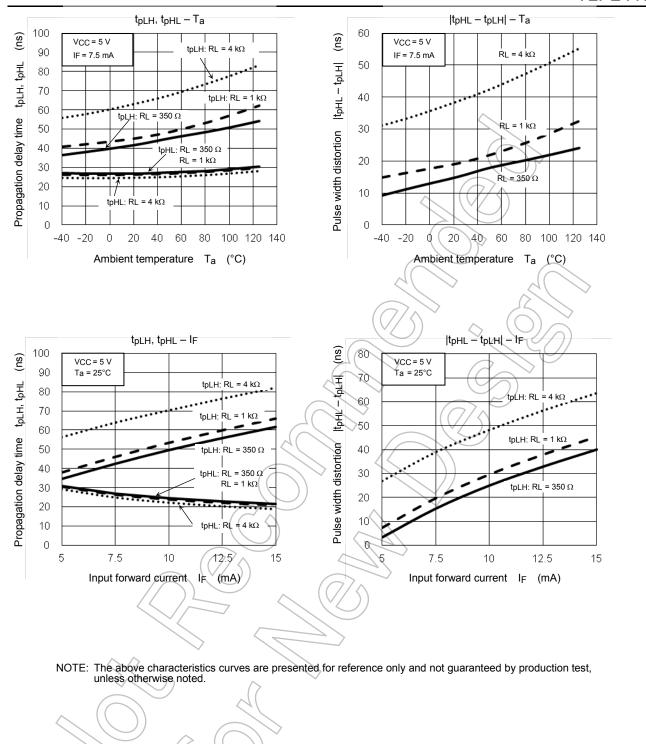


TEST CIRCUIT 6: Common-Mode Transient Immunity Test Circuit





NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

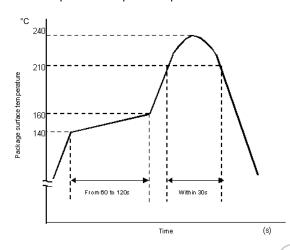


PRECAUTIONS OF SURFACE MOUNTING TYPE PHOTOCOUPLER SOLDERING & GENERAL STORAGE

(1) Precautions for Soldering

1) When Using Soldering Reflow

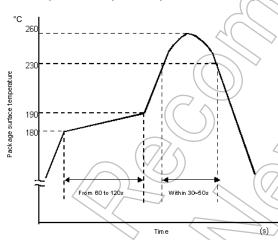
• An example of a temperature profile when Sn-Pb eutectic solder is used:



This profile is based on the device's maximum heat resistance guaranteed value.

Set the preheat temperature/heating temperature to the optimum temperature corresponding to the solder paste type used by the customer within the described profile.

• An example of a temperature profile when lead(Pb)-free solder is used



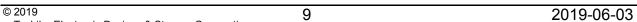
This profile is based on the device's maximum heat resistance guaranteed value.

Set the preheat temperature/heating temperature to the optimum temperature corresponding to the solder paste type used by the customer within the described profile.

- Reflow soldering must be performed once or twice.
- The mounting should be completed with the interval from the first to the last mountings being 2 weeks.
- 2) When using soldering Flow (Applicable to both eutectic solder and Lead(Pb)-Free solder)
 - Apply preheating of 150 °C for 60 to 120 seconds.
 - Mounting condition of 260 °C or less within 10 seconds is recommended.
 - Flow soldering must be performed once
- 3) When using soldering Iron (Applicable to both eutectic solder and Lead(Pb)-Free solder)
 - Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C.
 - Heating by soldering iron must be only once per 1 lead

(2) Precautions for General Storage

- 1) Do not store devices at any place where they will be exposed to moisture or direct sunlight.
- 2) When transportation or storage of devices, follow the cautions indicated on the carton box.
- 3) The storage area temperature should be kept within a temperature range of 5 °C to 35 °C, and relative humidity should be maintained at between 45% and 75%.
- 4) Do not store devices in the presence of harmful (especially corrosive)gases, or in dusty conditions.
- 5) Use storage areas where there is minimal temperature fluctuation. Because rapid temperature changes can cause condensation to occur on stored devices, resulting in lead oxidation or corrosion, as a result, the solderability of the leads will be degraded.
- 6) When repacking devices, use anti-static containers.
- 7) Do not apply any external force or load directly to devices while they are in storage.
- 8) If devices have been stored for more than two years, even though the above conditions have been followed, it is recommended that solderability of them should be tested before they are used.



Specification for Embossed-Tape Packing (TP) for SO8 Coupler

1. Applicable Package

Package	Product Type
SO8	Photocoupler

2. Product Naming System

Type of package used for shipment is denoted by a symbol suffix after a product number. The method of classification is as below.

(Example)



3. Tape Dimensions

3.1 Orientation of Device in Relation to Direction of Tape Movement

Device orientation in the recesses is as shown in Figure 1.

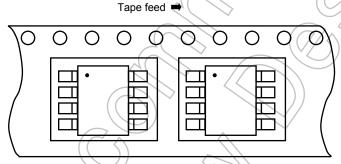


Figure 1 Device Orientation

3.2 Tape Packing Quantity: 2500 devices per reel

3.3 Empty Device Recesses Are as Shown in Table 1.

Table 1 Empty Device Recesses

	1 /	
	Standard	Remarks
Occurrences of 2 or more successive empty device recesses	0 device	Within any given 40-mm section of tape, not including leader and trailer
Single empty device recesses	6 devices (max) per reel	Not including leader and trailer

3.4 Start and End of Tape

The start of the tape has 50 or more empty holes. The end of tape has 50 or more empty holes and two empty turns only for a cover tape.

3.5 Tape Specification

- (1) Tape material: Plastic (protection against electrostatics)
- (2) Dimensions: The tape dimensions are as shown in Figure 2 and table 2.

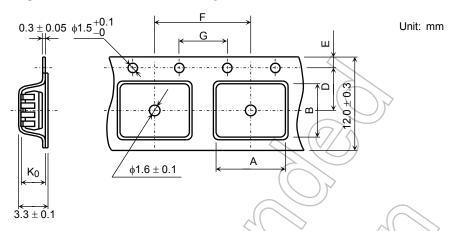


Figure 2 Tape Forms

Table 2 Tape Dimensions

Unit: mm Unless otherwise specified: ±0.1

		Chicos otherwise specifica: ±0.1
Symbol	Dimension	Remark
Α	6.5	
В	5.6	
D	5.5	Center line of indented square hole and sprocket hole
Е	1.75	Distance between tape edge and hole center
F	8.0	Cumulative error $^{+0.1}_{-0.3}$ (max) per 10 feed holes
G	4.0	Cumulative error $^{+0.1}_{-0.3}$ (max) per 10 feed holes
K ₀	3.1	Internal space

3.6 Reel

- (1) Material: Plastic
- (2) Dimensions: The reel dimensions are as shown in Figure 3 and Table 3.

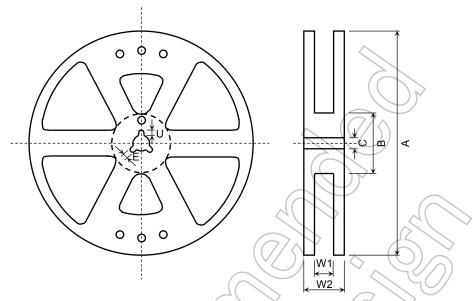


Figure 3 Reel Form

Table 3 Reel Dimensions

	UNICHIDA
Symbol	Dimension
Α ((Ф330 ±2
В	Ф80 ±1
¢())	Ф13 ±0.5
E	2.0 ±0.5
((//u))	4.0 ±0.5
W1	(13.5 ±0.5
Ŵ2	17.5 ±1.0

4. Packing

Packed in a shipping carton.

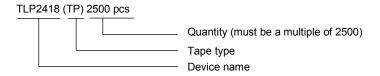
5. Label Indication

The carton bears a label indicating the product number, the symbol representing classification of standard, the quantity, the lot number and the Toshiba company name.

6. Ordering Method

When placing an order, please specify the product number, the tape type and the quantity as shown in the following example.

(Example)



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