

# TK40S06N1L

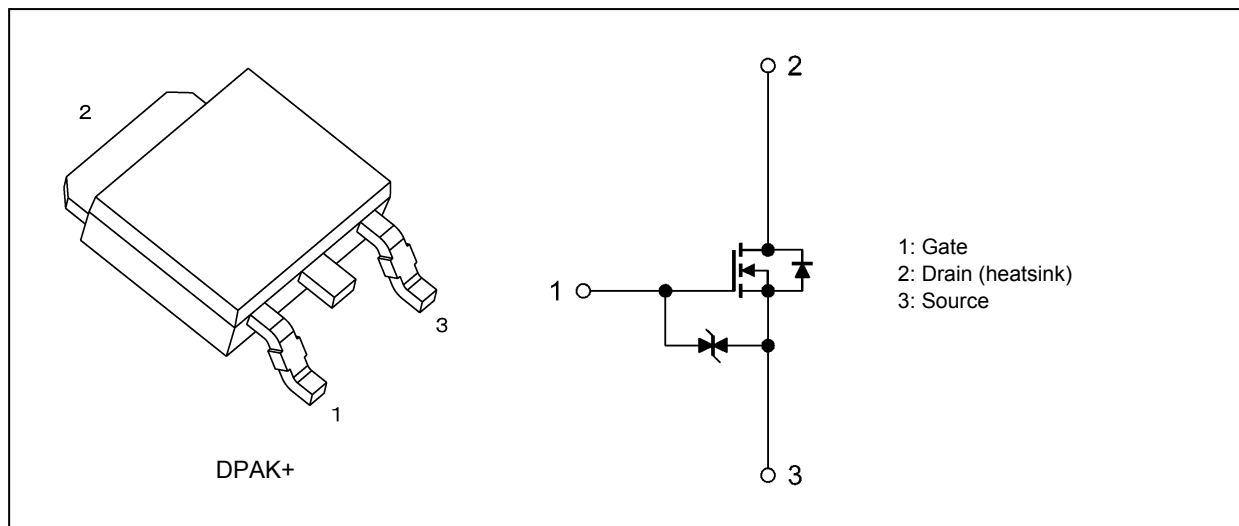
## 1. Applications

- Automotive
- Motor Drivers
- Switching Voltage Regulators

## 2. Features

- (1) AEC-Q101 qualified
- (2) Low drain-source on-resistance:  $R_{DS(ON)} = 8.7 \text{ m}\Omega$  (typ.) ( $V_{GS} = 10 \text{ V}$ )
- (3) Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = 60 \text{ V}$ )
- (4) Enhancement mode:  $V_{th} = 1.5 \text{ to } 2.5 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 0.2 \text{ mA}$ )

## 3. Packaging and Internal Circuit



Start of commercial production

2015-06

## 4. Absolute Maximum Ratings (Note) ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics   | Symbol              | Rating     | Unit             |
|---|---------------------|------------|------------------|
| Drain-source voltage                                    | $V_{\text{DSS}}$    | 60         | V                |
| Gate-source voltage                                     | $V_{\text{GSS}}$    | $\pm 20$   |                  |
| Drain current (DC) (Note 1)                             | $I_{\text{D}}$      | 40         | A                |
| Drain current (pulsed) (Note 1)                         | $I_{\text{DP}}$     | 80         |                  |
| Power dissipation ( $T_c = 25^\circ\text{C}$ ) (Note 2) | $P_{\text{D}}$      | 88.2       | W                |
| Single-pulse avalanche energy (Note 3)                  | $E_{\text{AS}}$     | 23.4       | mJ               |
| Single-pulse avalanche current                          | $I_{\text{AS}}$     | 40         | A                |
| Turn-off $dV_{\text{DS}}/dt$ ruggedness                 | $dV_{\text{DS}}/dt$ | 7.2        | V/ns             |
| Channel temperature (Note 4)                            | $T_{\text{ch}}$     | 175        | $^\circ\text{C}$ |
| Storage temperature (Note 4)                            | $T_{\text{stg}}$    | -55 to 175 |                  |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## 5. Thermal Characteristics

| Characteristics                    | Symbol                | Max | Unit               |
|------------------------------------|-----------------------|-----|--------------------|
| Channel-to-case thermal resistance | $R_{\text{th(ch-c)}}$ | 1.7 | $^\circ\text{C/W}$ |

Note 1: Ensure that the channel temperature does not exceed  $175^\circ\text{C}$ .

Note 2: The power dissipation value is calculated based on the channel-to-case thermal resistance. However, the safe operating area is not only limited to thermal limits but also the current concentration phenomenon. This device should not be used under conditions outside its safe operating area shown herein.

Note 3:  $V_{\text{DD}} = 48\text{ V}$ ,  $T_{\text{ch}} = 25^\circ\text{C}$  (initial),  $L = 11.3\text{ }\mu\text{H}$ ,  $R_{\text{G}} = 25\text{ }\Omega$ ,  $I_{\text{AS}} = 40\text{ A}$

Note 4: The definitions of the absolute maximum channel and storage temperatures are qualified per AEC-Q101.

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

## 6. Electrical Characteristics

### 6.1. Static Characteristics ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics                | Symbol        | Test Condition                                     | Min | Typ. | Max      | Unit             |
|--------------------------------|---------------|--|-----|------|----------|------------------|
| Gate leakage current           | $I_{GSS}$     | $V_{GS} = \pm 16\text{ V}$ , $V_{DS} = 0\text{ V}$ | —   | —    | $\pm 10$ | $\mu\text{A}$    |
| Drain cut-off current          | $I_{DSS}$     | $V_{DS} = 60\text{ V}$ , $V_{GS} = 0\text{ V}$     | —   | —    | 10       |                  |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $I_D = 10\text{ mA}$ , $V_{GS} = 0\text{ V}$       | 60  | —    | —        | V                |
| Drain-source breakdown voltage | $V_{(BR)DSX}$ | $I_D = 10\text{ mA}$ , $V_{GS} = -20\text{ V}$     | 40  | —    | —        |                  |
| Gate threshold voltage         | $V_{th}$      | $V_{DS} = 10\text{ V}$ , $I_D = 0.2\text{ mA}$     | 1.5 | —    | 2.5      |                  |
| Drain-source on-resistance     | $R_{DS(ON)}$  | $V_{GS} = 4.5\text{ V}$ , $I_D = 20\text{ A}$      | —   | 12.3 | 18       | $\text{m}\Omega$ |
|                                |               | $V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$       | —   | 8.7  | 10.5     |                  |

### 6.2. Dynamic Characteristics ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics                | Symbol    | Test Condition  | Min | Typ. | Max | Unit        |
|--------------------------------|-----------|---|-----|------|-----|-------------|
| Input capacitance              | $C_{iss}$ | $V_{DS} = 10\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$ | —   | 1650 | —   | $\text{pF}$ |
| Reverse transfer capacitance   | $C_{rss}$ |   | —   | 107  | —   |             |
| Output capacitance             | $C_{oss}$ |   | —   | 835  | —   |             |
| Switching time (rise time)     | $t_r$     | See Figure 6.2.1.   | —   | 7    | —   | $\text{ns}$ |
| Switching time (turn-on time)  | $t_{on}$  |   | —   | 16   | —   |             |
| Switching time (fall time)     | $t_f$     |   | —   | 11   | —   |             |
| Switching time (turn-off time) | $t_{off}$ |   | —   | 38   | —   |             |

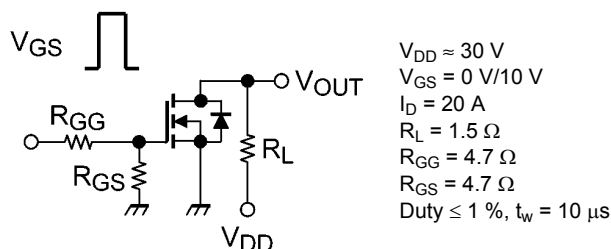


Fig. 6.2.1 Switching Time Test Circuit

### 6.3. Gate Charge Characteristics ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

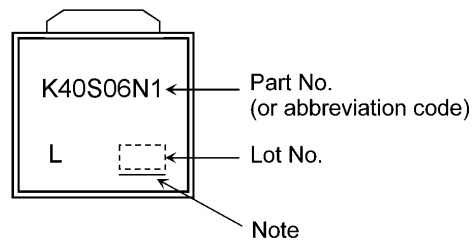
| Characteristics                                 | Symbol    | Test Condition  | Min | Typ. | Max | Unit        |
|---|-----------|---|-----|------|-----|-------------|
| Total gate charge (gate-source plus gate-drain) | $Q_g$     | $V_{DD} \approx 48\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 40\text{ A}$ | —   | 26   | —   | $\text{nC}$ |
| Gate-source charge 1                            | $Q_{gs1}$ |   | —   | 6    | —   |             |
| Gate-drain charge                               | $Q_{gd}$  |   | —   | 6    | —   |             |

### 6.4. Source-Drain Characteristics ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics                         | Symbol    | Test Condition  | Min | Typ. | Max  | Unit |
|---|-----------|---|-----|------|------|------|
| Reverse drain current (DC) (Note 5)     | $I_{DR}$  | —   | —   | —    | 40   | A    |
| Reverse drain current (pulsed) (Note 5) | $I_{DRP}$ |   | —   | —    | 80   |      |
| Diode forward voltage                   | $V_{DSF}$ | $I_{DR} = 40\text{ A}$ , $V_{GS} = 0\text{ V}$  | —   | —    | -1.2 | V    |
| Reverse recovery time                   | $t_{rr}$  | $I_{DR} = 40\text{ A}$ , $V_{GS} = 0\text{ V}$<br>$-dI_{DR}/dt = 50\text{ A}/\mu\text{s}$ | —   | 46   | —    | ns   |
| Reverse recovery charge                 | $Q_{rr}$  |   | —   | 23   | —    | nC   |

Note 5: Ensure that the channel temperature does not exceed  $175^\circ\text{C}$ .

## 7. Marking (Note)



**Fig. 7.1 Marking**

Note: A line under a Lot No. identifies the indication of product Labels.

Not underlined: [[Pb]]/INCLUDES > MCV

Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

## 8. Characteristics Curves (Note)

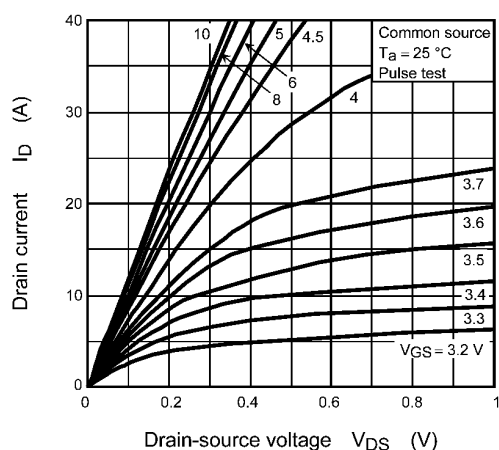


Fig. 8.1  $I_D - V_{DS}$

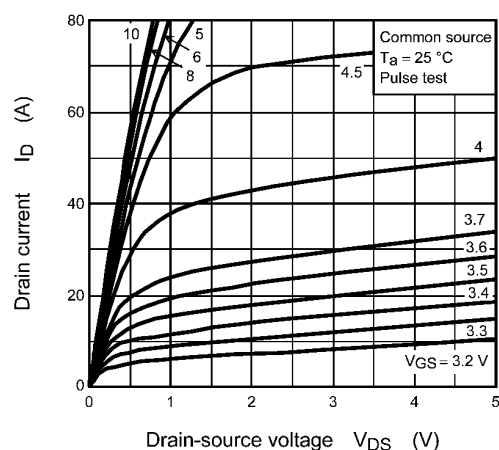


Fig. 8.2  $I_D - V_{DS}$

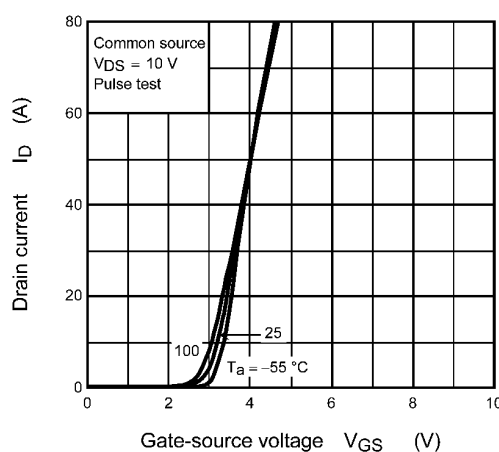


Fig. 8.3  $I_D - V_{GS}$

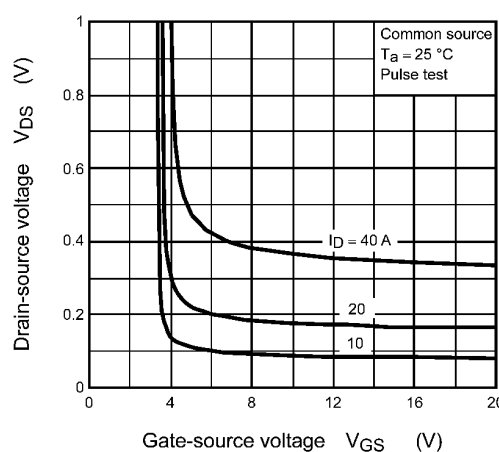


Fig. 8.4  $V_{DS} - V_{GS}$

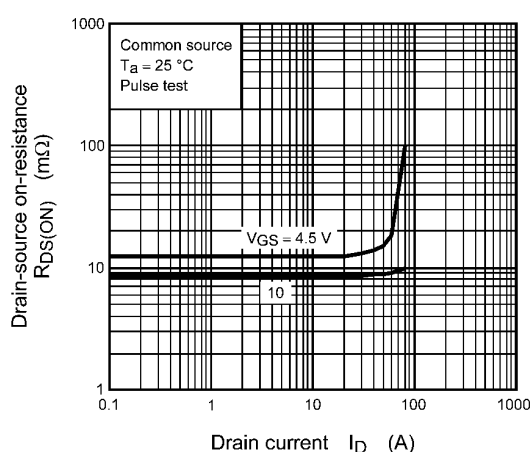


Fig. 8.5  $R_{DS(ON)} - I_D$

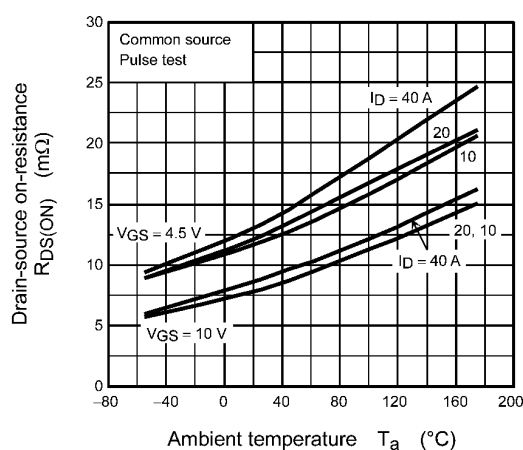


Fig. 8.6  $R_{DS(ON)} - T_a$

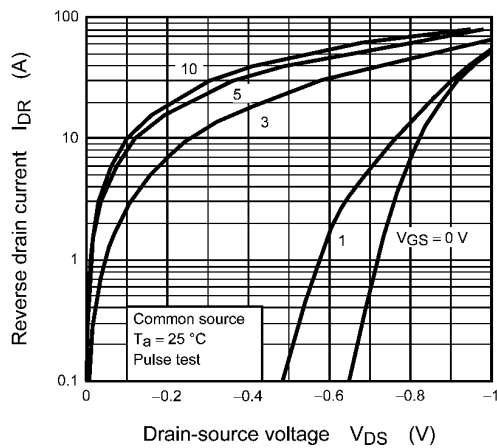


Fig. 8.7  $I_{DR} - V_{DS}$

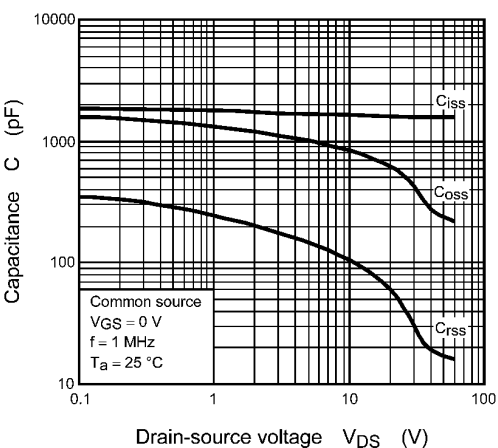


Fig. 8.8 Capacitance -  $V_{DS}$

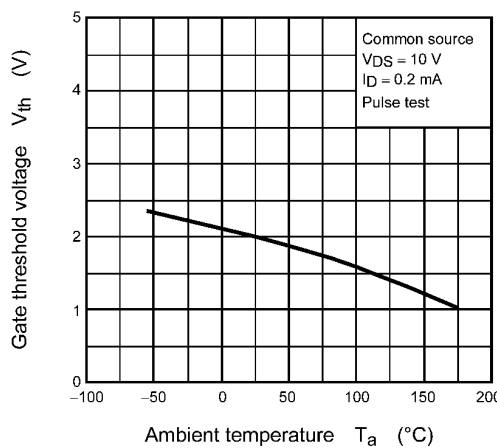


Fig. 8.9  $V_{th} - T_a$

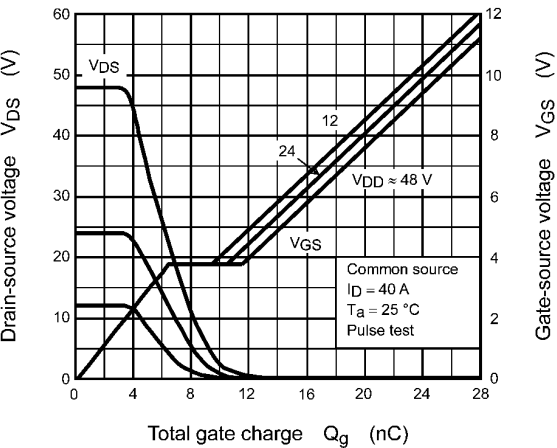


Fig. 8.10 Dynamic Input/Output Characteristics

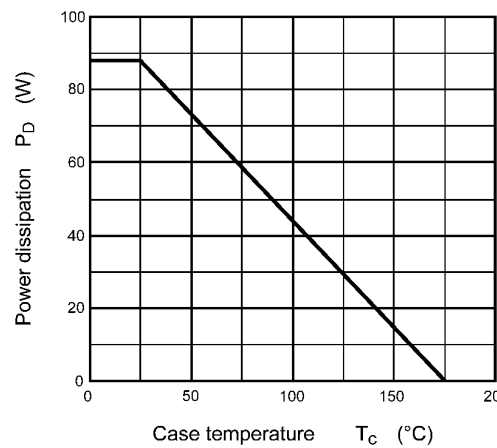
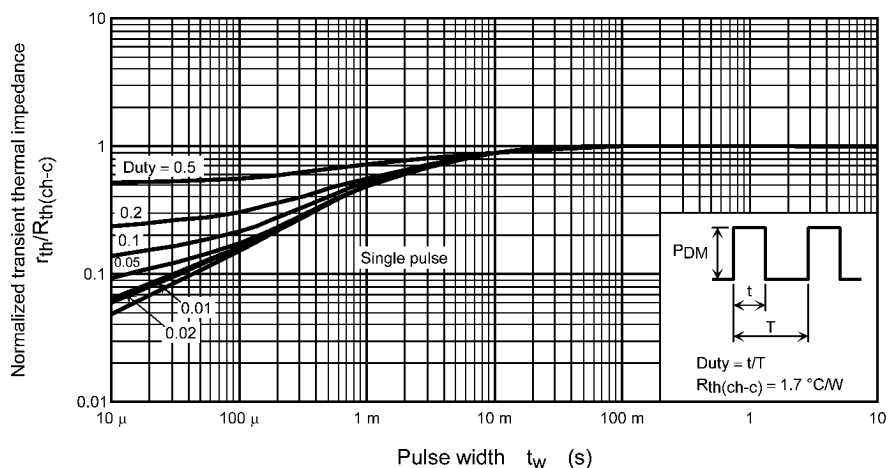
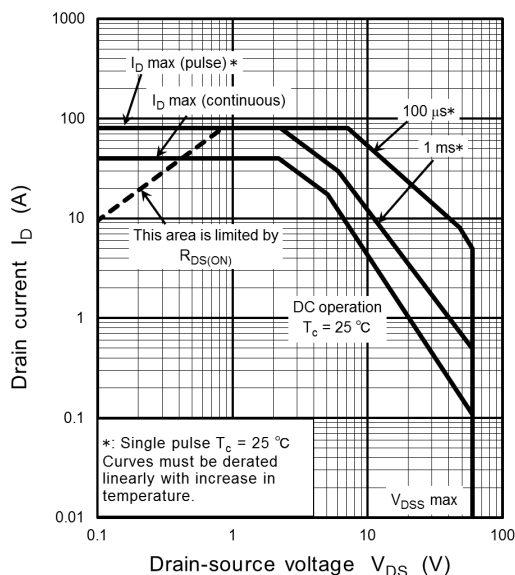


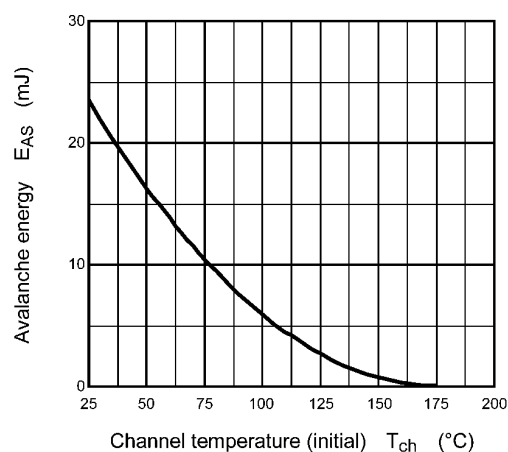
Fig. 8.11  $P_D - T_c$   
(Guaranteed Maximum)



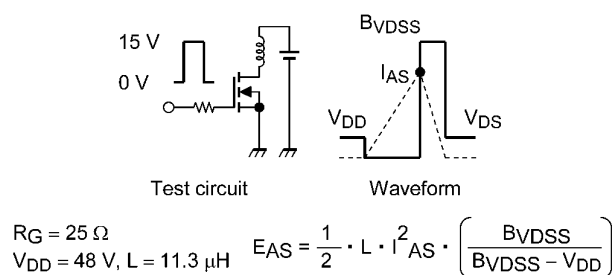
**Fig. 8.12  $r_{th}/R_{th(ch-c)} - t_w$**   
(Guaranteed Maximum)



**Fig. 8.13 Safe Operating Area**  
(Guaranteed Maximum)



**Fig. 8.14  $E_{AS} - T_{ch}$**   
(Guaranteed Maximum)

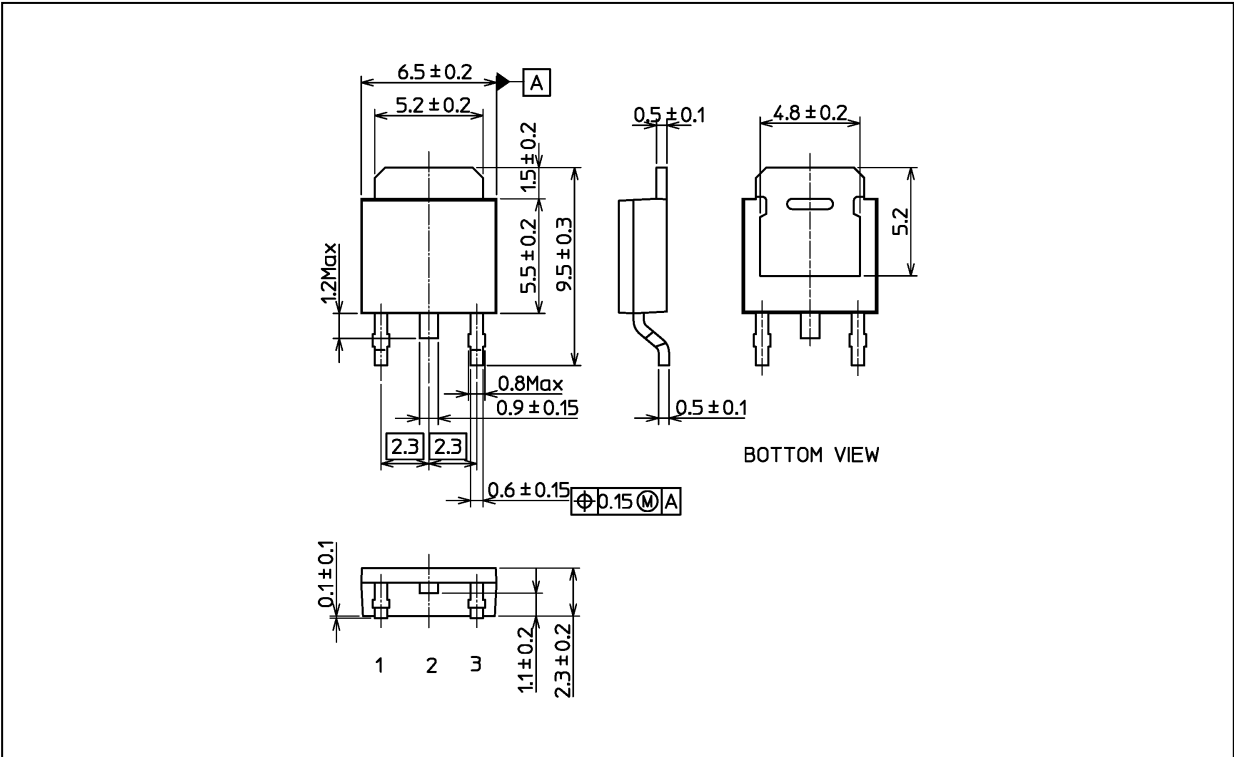


**Fig. 8.15 Test Circuit/Waveform**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.36 g (typ.)

| Package Name(s) |
|-----------------|
| TOSHIBA: 2-7M1A |
| Nickname: DPAK+ |



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