Unit: mm

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π-MOS VII)

TK12A55D

Switching Regulator Applications

• Low drain-source ON-resistance: RDS (ON) = $0.48 \Omega(\text{typ.})$

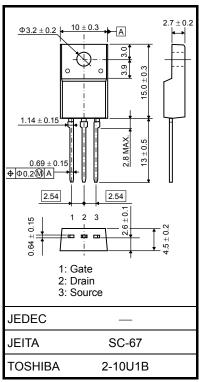
• High forward transfer admittance: $|Y_{fs}| = 6.0 \text{ S (typ.)}$

• Low leakage current: $I_{DSS} = 10 \mu A \text{ (max) (V}_{DS} = 550 \text{ V)}$

• Enhancement mode: $V_{th} = 2.0 \text{ to } 4.0 \text{ V (V}_{DS} = 10 \text{ V, I}_{D} = 1 \text{ mA)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	550	V
Gate-source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I _D	12	Α
	Pulse (Note 1)	I _{DP}	48	A
Drain power dissipati	on (Tc = 25°C)	PD	45	W
Single pulse avalance	ne energy (Note 2)	E _{AS}	317	mJ
Avalanche current		I _{AR}	12	Α
Repetitive avalanche	energy (Note 3)	E _{AR}	4.5	mJ
Channel temperature		T _{ch}	150	°C
Storage temperature range		T _{stg}	-55 to 150	°C



Weight: 1.7 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

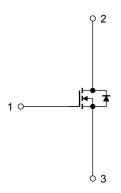
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	R _{th (ch-c)}	2.78	°C/W
Thermal resistance, channel to ambient	R _{th (ch-a)}	62.5	°C/W



Note 2: $V_{DD} = 90 \text{ V}$, $T_{ch} = 25^{\circ}\text{C}(\text{initial})$, L = 3.8 mH, $R_G = 25 \Omega$, $I_{AR} = 12 \text{ A}$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.



Start of commercial production 2009-02

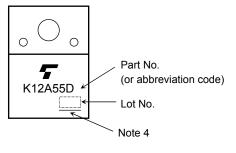
Electrical Characteristics (Ta = 25°C)

Chara	acteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cur	rent	I _{GSS}	$V_{GS}=\pm30~V,~V_{DS}=0~V$	_	_	±1	μА
Drain cut-off curre	ent	I _{DSS}	V _{DS} = 550 V, V _{GS} = 0 V	_	_	10	μА
Drain-source brea	akdown voltage	V (BR) DSS	I _D = 10 mA, V _{GS} = 0 V	550	_	_	V
Gate threshold vo	oltage	V _{th}	V _{DS} = 10 V, I _D = 1 mA	2.0	_	4.0	V
Drain-source ON	resistance	R _{DS} (ON)	V _{GS} = 10 V, I _D = 6 A	_	0.48	0.57	Ω
Forward transfer	admittance	Y _{fs}	V _{DS} = 10 V, I _D = 6 A	1.5	6.0	_	S
Input capacitance)	C _{iss}		_	1550	_	
Reverse transfer capacitance		C _{rss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	_	7	_	рF
Output capacitance		Coss		_	165	_	
Switching time	Rise time	t _r	10 V ID = 6 A VOUT	_	25	_	
	Turn-on time	t _{on}	$\begin{array}{c} 0 \text{ V} \\ \hline \\ 50 \Omega \end{array} \end{array} \Longrightarrow \begin{array}{c} \text{RL} = 33 \Omega \\ \text{V}_{DD} \approx 200 \text{ V} \end{array}$	_	60	_	
	Fall time	t _f		_	15	_	ns
	Turn-off time	t _{off}	V _{DD} ≈ 200 V Duty ≤ 1%, t _W = 10 μs	_	110	_	
Total gate charge		Qg		_	28	_	
Gate-source charge		Q _{gs}	$V_{DD} \approx 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$	_	18	_	nC
Gate-drain charge		Q _{gd}		_	10	_	

Source-Drain Ratings and Characteristics (Ta = 25°C)

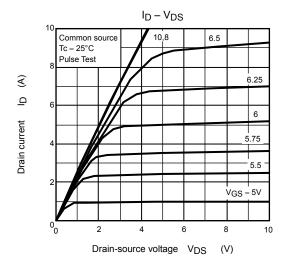
Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1)	I _{DR}	_	_	_	12	Α
Pulse drain reverse current (Note 1)	I _{DRP}	_	_	_	48	Α
Forward voltage (diode)	V _{DSF}	I _{DR} = 12 A, V _{GS} = 0 V	_	_	-1.7	V
Reverse recovery time	t _{rr}	I _{DR} = 12 A, V _{GS} = 0 V,	_	1300	_	ns
Reverse recovery charge	Q _{rr}	dl _{DR} /dt = 100 A/μs	_	13	_	μС

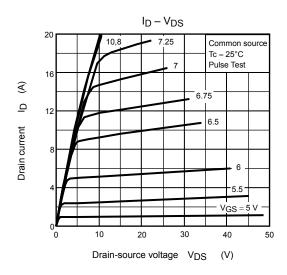
Marking

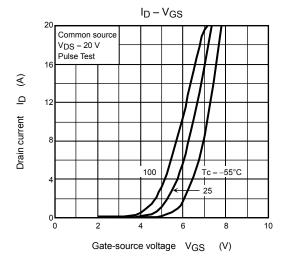


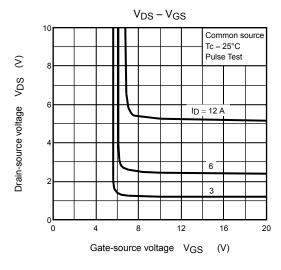
Note 4: A line under a Lot No. identifies the indication of product Labels $\hbox{[[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]}$

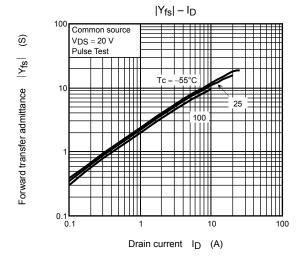
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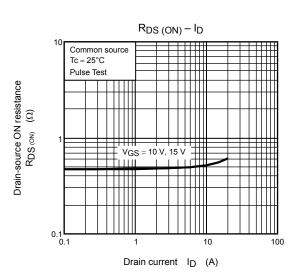




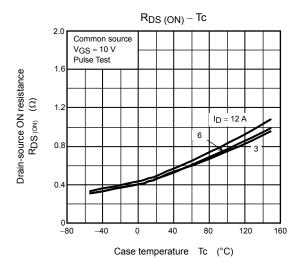


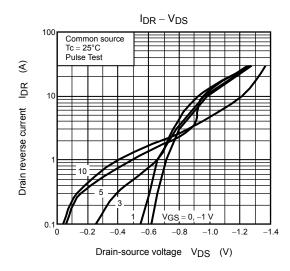


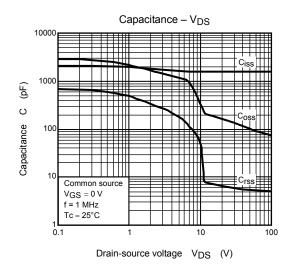


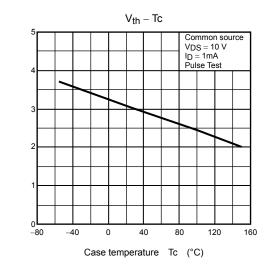


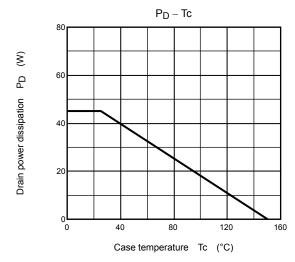
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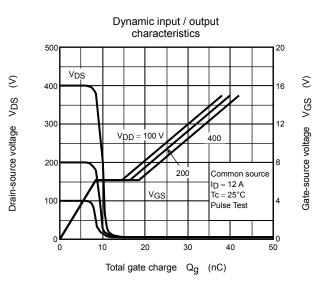








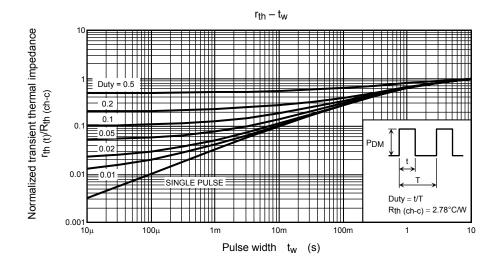


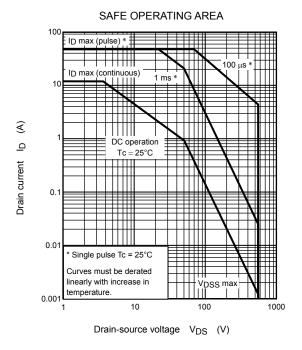


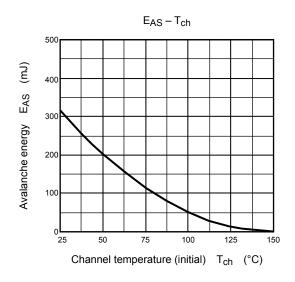
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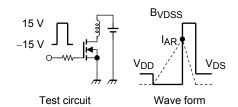
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Gate threshold voltage









$$R_G = 25~\Omega$$

$$V_{DD} = 90~V,~L = 3.8~mH$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{BVDSS}{BVDSS - VDD} \right)$$

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