CMOS Digital Integrated Circuits Silicon Monolithic

# TC7WB66CFK,TC7WB67CFK

## 1. Functional Description

- Dual SPST Bus Switch

## 2. General

The TC7WB66CFK and TC7WB67CFK are low ON-resistance, high-speed CMOS 2-bit bus switches. These bus switches allow connections or disconnections to be made with minimal propagation delay while maintaining Low power dissipation which is the feature of CMOS.

TC7WB66CFK requires the output enable (OE) input to be set low to place the output into the high impedance state,whereas the TC7WB67CFK requires the output enable ($\overline{OE}$) input to be set high to place the output into the high impedance.

These Bus switches consist of P-MOS and N-MOS structure, meaning these devices are suitable for analog signal transmission.

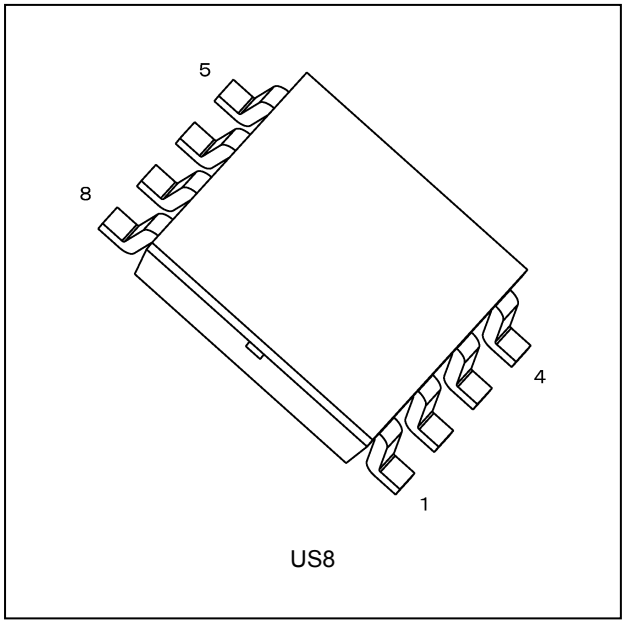
All inputs are equipped with protector circuits to protect the device from static discharge.

## 3. Features

(1) AEC-Q100 (rev.H) Grade 1 qualified (Note 1)
(2) Wide operating temperature range: $T_{opr}$ = -40 to 125 °C (Note 2)
(3) Operating voltage: $V_{CC}$ = 1.65 to 5.5 V
(4) ON capacitance: $C_{I/O}$ = 10 pF Switch On (typ.) @$V_{CC}$ = 5.0 V
(5) ON resistance: $R_{ON}$ = 4 Ω (typ.) @$V_{CC}$ = 4.5 V, $V_{IS}$ = 0 V
(6) Package: US8

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.
Note 2: For devices with the ordering part number ending in (CT. $T_{opr}$ = -40 to 85 °C for the other devices.

## 4. Packaging

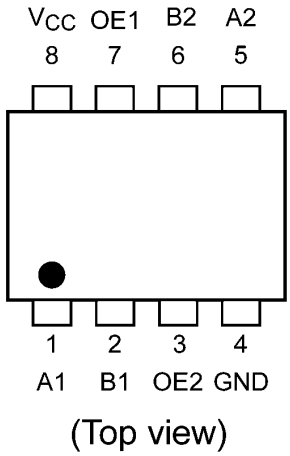



US8

Start of commercial production
2020-09

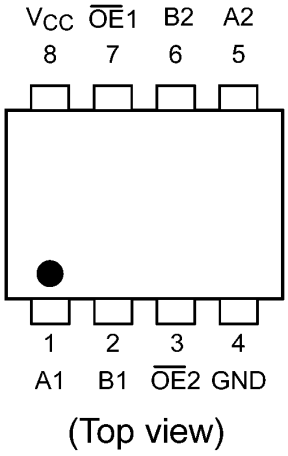
## 5. Pin Assignment

TC7WB66CFK




(Top view)

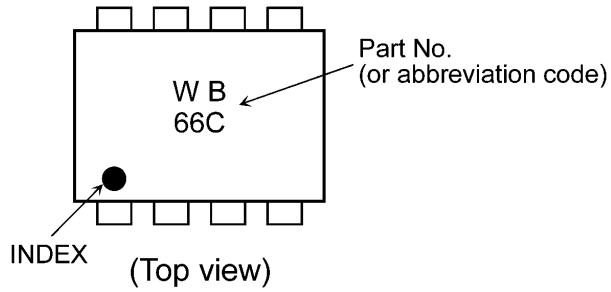
TC7WB67CFK




(Top view)

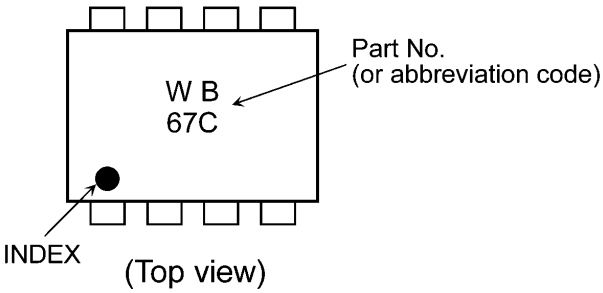
## 6. Marking

TC7WB66CFK




(Top view)

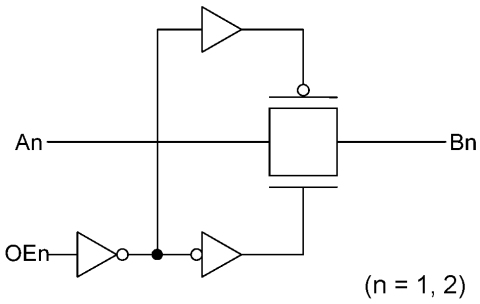
TC7WB67CFK




(Top view)

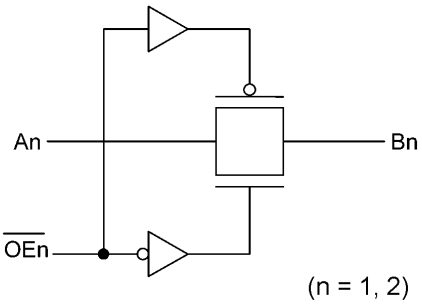
## 7. Block Diagram

TC7WB66CFK




(n = 1, 2)

TC7WB67CFK




(n = 1, 2)

## 8. Principle of Operation

### 8.1. Truth Table

| Inputs OE (TC7WB66CFK) | Inputs $\overline{OE}$ (TC7WB67CFK) | Function |
|---|---|---|
| H | L | A port = B port |
| L | H | Disconnect |

## 9. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a$ = 25 °C)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | -0.5 to 7.0 | V |
| Input voltage (OE, $\overline{OE}$) | $V_{IN}$ | -0.5 to 7.0 | V |
| Switch I/O voltage | $V_S$ | -0.5 to $V_{CC}$ +0.5 | V |
| Clamp diode current | $I_{IK}$ | -50 | mA |
| Switch I/O current | $I_S$ | 50 | mA |
| Power dissipation | $P_D$ | 200 | mW |
| $V_{CC}$/ground current | $I_{CC}/I_{GND}$ | ±100 | mA |
| Storage temperature | $T_{stg}$ | -65 to 150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## 10. Operating Ranges (Note)

| Characteristics | Symbol | Note | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 1.65 to 5.5 | V |
| Input voltage (OE, $\overline{OE}$) | $V_{IN}$ | | 0 to 5.5 | V |
| Switch I/O voltage | $V_S$ | | 0 to $V_{CC}$ | V |
| Operating temperature | $T_{opr}$ | (Note 1) | -40 to 125 | °C |
| | | (Note 2) | -40 to 85 | |
| Input rise time | dt/dv | | 0 to 10 | ns/V |
| Input fall time | | | 0 to 10 | |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused control inputs must be tied to either $V_{CC}$ or GND.
Note 1: For devices with the ordering part number ending in (CT.
Note 2: For devices except those with the ordering part number ending in (CT.

## 11. Electrical Characteristics

### 11.1. DC Characteristics (Unless otherwise specified, $T_a$ = -40 to 85 °C)

| Characteristics | Symbol | Note | Test Condition | $V_{CC}$ (V) | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| High-level input voltage (OE, $\overline{OE}$) | $V_{IH}$ | | — | 1.65 to 1.95 | 0.8 × $V_{CC}$ | — | — | V |
| | | | | 2.3 to 5.5 | 0.7 × $V_{CC}$ | — | — | |
| Low-level input voltage (OE, $\overline{OE}$) | $V_{IL}$ | | — | 1.65 to 1.95 | — | — | 0.2 × $V_{CC}$ | V |
| | | | | 2.3 to 5.5 | — | — | 0.3 × $V_{CC}$ | |
| Input leakage current (OE, $\overline{OE}$) | $I_{IN}$ | | $V_{IN}$ = 0 to 5.5 V | 1.65 to 5.5 | — | — | ±1.0 | μA |
| Switch OFF-state leakage current | $I_{SZ}$ | | A, B = 0 to $V_{CC}$, $\overline{OE}$ = GND (TC7WB66CFK) $\overline{OE}$ = $V_{CC}$ (TC7WB67CFK) | 1.65 to 5.5 | — | — | ±10 | μA |
| ON-resistance | $R_{ON}$ | (Note 1), (Note 2) | $V_{IS}$ = 0 V, $I_{IS}$ = 30 mA | 4.5 | — | 4 | 7 | Ω |
| | | | $V_{IS}$ = 2.4 V, $I_{IS}$ = 30 mA | 4.5 | — | 5 | 12 | |
| | | | $V_{IS}$ = 4.5 V, $I_{IS}$ = 30 mA | 4.5 | — | 6 | 10 | |
| | | | $V_{IS}$ = 0 V, $I_{IS}$ = 24 mA | 3.0 | — | 5 | 9 | |
| | | | $V_{IS}$ = 3.0 V, $I_{IS}$ = 24 mA | 3.0 | — | 7 | 14 | |
| | | | $V_{IS}$ = 0 V, $I_{IS}$ = 8 mA | 2.3 | — | 6 | 12 | |
| | | | $V_{IS}$ = 2.3 V, $I_{IS}$ = 8 mA | 2.3 | — | 9 | 18 | |
| | | | $V_{IS}$ = 0 V, $I_{IS}$ = 4 mA | 1.65 | — | 8 | 20 | |
| | | | $V_{IS}$ = 1.65 V, $I_{IS}$ = 4 mA | 1.65 | — | 15 | 30 | |
| Quiescent supply current | $I_{CC}$ | | $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0 A | 5.5 | — | — | 10 | μA |
| | $\Delta I_{CC}$ | | $V_{IN}$ = $V_{CC}$ - 0.6 V | 5.5 | — | — | 50 | μA |

Note 1: All typical values are at $T_a$ = 25 °C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On-resistance is determined by the lower of the voltages on the two (A or B) pins.

## 11.2. DC Characteristics (Unless otherwise specified, $T_a$ = -40 to 125 °C)

| Characteristics | Symbol | Note | Test Condition | $V_{CC}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| High-level input voltage (OE, $\overline{OE}$) | $V_{IH}$ | | — | 1.65 to 1.95 | 0.8 × $V_{CC}$ | — | V |
| | | | | 2.3 to 5.5 | 0.7 × $V_{CC}$ | — | |
| Low-level input voltage (OE, $\overline{OE}$) | $V_{IL}$ | | — | 1.65 to 1.95 | — | 0.2 × $V_{CC}$ | V |
| | | | | 2.3 to 5.5 | — | 0.3 × $V_{CC}$ | |
| Input leakage current (OE, $\overline{OE}$) | $I_{IN}$ | | $V_{IN}$ = 0 to 5.5 V | 1.65 to 5.5 | — | ±2.0 | μA |
| Switch OFF-state leakage current | $I_{SZ}$ | | A, B = 0 to $V_{CC}$, $\overline{OE}$ = GND (TC7WB66CFK) $\overline{OE}$ = $V_{CC}$ (TC7WB67CFK) | 1.65 to 5.5 | — | ±20 | μA |
| ON-resistance | $R_{ON}$ | (Note 1) | $V_{IS}$ = 0 V, $I_{IS}$ = 30 mA | 4.5 | — | 9 | Ω |
| | | | $V_{IS}$ = 2.4 V, $I_{IS}$ = 30 mA | 4.5 | — | 14 | |
| | | | $V_{IS}$ = 4.5 V, $I_{IS}$ = 30 mA | 4.5 | — | 12 | |
| | | | $V_{IS}$ = 0 V, $I_{IS}$ = 24 mA | 3.0 | — | 11 | |
| | | | $V_{IS}$ = 3.0 V, $I_{IS}$ = 24 mA | 3.0 | — | 16 | |
| | | | $V_{IS}$ = 0 V, $I_{IS}$ = 8 mA | 2.3 | — | 15 | |
| | | | $V_{IS}$ = 2.3 V, $I_{IS}$ = 8 mA | 2.3 | — | 21 | |
| | | | $V_{IS}$ = 0 V, $I_{IS}$ = 4 mA | 1.65 | — | 23 | |
| | | | $V_{IS}$ = 1.65 V, $I_{IS}$ = 4 mA | 1.65 | — | 33 | |
| Quiescent supply current | $I_{CC}$ | | $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0 A | 5.5 | — | 100 | μA |
| | $\Delta I_{CC}$ | | $V_{IN}$ = $V_{CC}$ - 0.6 V | 5.5 | — | 100 | μA |

Note 1: Measured by the voltage drop between A and B pins at the indicated current through the switch. On-resistance is determined by the lower of the voltages on the two (A or B) pins.

## 11.3. AC Characteristics (Unless otherwise specified, $T_a$ = -40 to 85 °C)

| Characteristics | Symbol | Note | Test Condition | $V_{CC}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| Output enable time | $t_{PZL}$,$t_{PZH}$ | | See Fig. 11.2.1, 11.2.2, Table 11.2.1 | 5.0 ± 0.5 | — | 4 | ns |
| | | | | 3.3 ± 0.3 | — | 6 | |
| | | | | 2.5 ± 0.2 | — | 9 | |
| | | | | 1.8 ± 0.15 | — | 18 | |
| Output disable time | $t_{PLZ}$,$t_{PHZ}$ | | See Fig. 11.2.1, 11.2.2, Table 11.2.1 | 5.0 ± 0.5 | — | 4.5 | ns |
| | | | | 3.3 ± 0.3 | — | 7 | |
| | | | | 2.5 ± 0.2 | — | 9 | |
| | | | | 1.8 ± 0.15 | — | 18 | |

## 11.4. AC Characteristics (Unless otherwise specified, $T_a$ = -40 to 125 °C)

| Characteristics | Symbol | Note | Test Condition | $V_{CC}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| Output enable time | $t_{PZL}$,$t_{PZH}$ | | See Fig. 11.2.1, 11.2.2, Table 11.2.1 | 5.0 ± 0.5 | — | 6 | ns |
| | | | | 3.3 ± 0.3 | — | 8 | |
| | | | | 2.5 ± 0.2 | — | 11 | |
| | | | | 1.8 ± 0.15 | — | 20 | |
| Output disable time | $t_{PLZ}$,$t_{PHZ}$ | | See Fig. 11.2.1, 11.2.2, Table 11.2.1 | 5.0 ± 0.5 | — | 6.5 | ns |
| | | | | 3.3 ± 0.3 | — | 9 | |
| | | | | 2.5 ± 0.2 | — | 11 | |
| | | | | 1.8 ± 0.15 | — | 20 | |

## 11.5. Capacitive Characteristics (Note) (Unless otherwise specified, $T_a$ = 25 °C)

| Characteristics | Part Number | Symbol | Note | Test Condition | $V_{CC}$ (V) | Typ. | Unit |
|---|---|---|---|---|---|---|---|
| Input capacitance (OE, $\overline{OE}$) | | $C_{IN}$ | | $V_{IN}$ = 0 V | 5.0 | 4 | pF |
| Switch terminal OFF-capacitance | TC7WB66CFK | $C_{I/O}$ | | OE = GND, $V_{I/O}$ = 0 V | 5.0 | 5 | pF |
| | TC7WB67CFK | | | $\overline{OE}$ = $V_{CC}$, $V_{I/O}$ = 0 V | 5.0 | 5 | |
| Switch terminal ON-capacitance | TC7WB66CFK | $C_{I/O}$ | | OE = $V_{CC}$, $V_{I/O}$ = 0 V | 5.0 | 10 | pF |
| | TC7WB67CFK | | | $\overline{OE}$ = GND, $V_{I/O}$ = 0 V | 5.0 | 10 | |

Note: Parameter guaranteed by design.

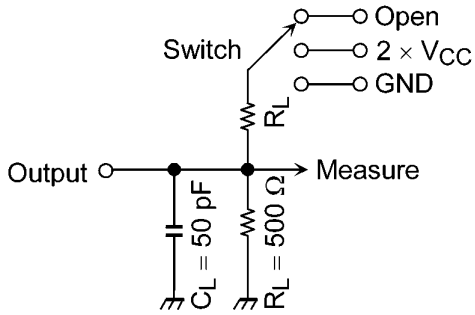



**Fig. 11.2.1 AC Test Circuit**

**Table 11.2.1 Parameter for AC Test Circuit**

| Parameter | Switch |
|---|---|
| $t_{PLZ}$, $t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}$, $t_{PZH}$ | GND |

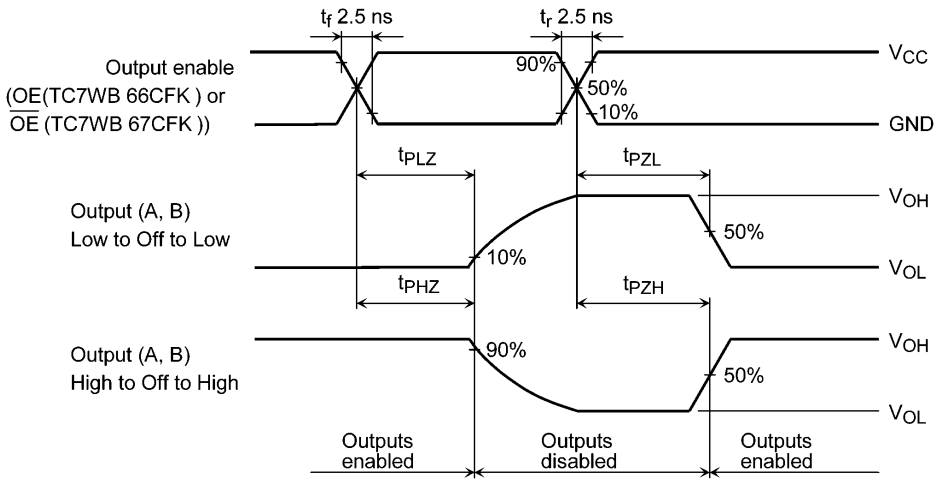



**Fig. 11.2.2 AC Waveform $t_{PLZ}$, $t_{PHZ}$, $t_{PZL}$, $t_{PZH}$**

## 12. Rise and Fall Time ($t_r/t_f$)

The $t_r$ and $t_{f(out)}$ values of the output signals are affected by the CR time constant of the input, which consists of the switch terminal capacitance ($C_{I/O}$) and the on-resistance ($R_{ON}$) of the input.
In practice, the $t_r$ and $t_{f(out)}$ values are also affected by the circuit's capacitance and resistance components other than the capacitance of TC7WB66CFK, TC7WB67CFK
The $t_r/t_{f(out)}$ values can be approximated as follows.
(Figure 12.1, Table 12.1 shows the test circuit.)

$t_r/t_{f(out)}$ (approx) = - ($C_{I/O}$ + $C_L$) · ($R_{DRIVE}$ + $R_{ON}$) · ln ((($V_{OH}$ - $V_{OL}$) - $V_M$) / ($V_{OH}$ - $V_{OL}$))
Where, $R_{DRIVE}$ is the output impedance of the previous-stage circuit.

Calculation example:

$t_{r(out)}$ (approx) = - (10 + 15) E - 12 · (120 + 4) · ln ((((4.5 - 0) - 2.25) / (4.5 - 0)) = ≈2.1 ns

Calculation conditions:

$V_{CC}$ = 4.5 V, $C_L$ = 15 pF, $R_{DRIVE}$ = 120 Ω (output impedance of the previous IC), $V_M$ = 2.25 V ($V_{CC}$/2)
Output of the previous IC = digital (i.e., high-level voltage = $V_{CC}$, low-level voltage = GND)

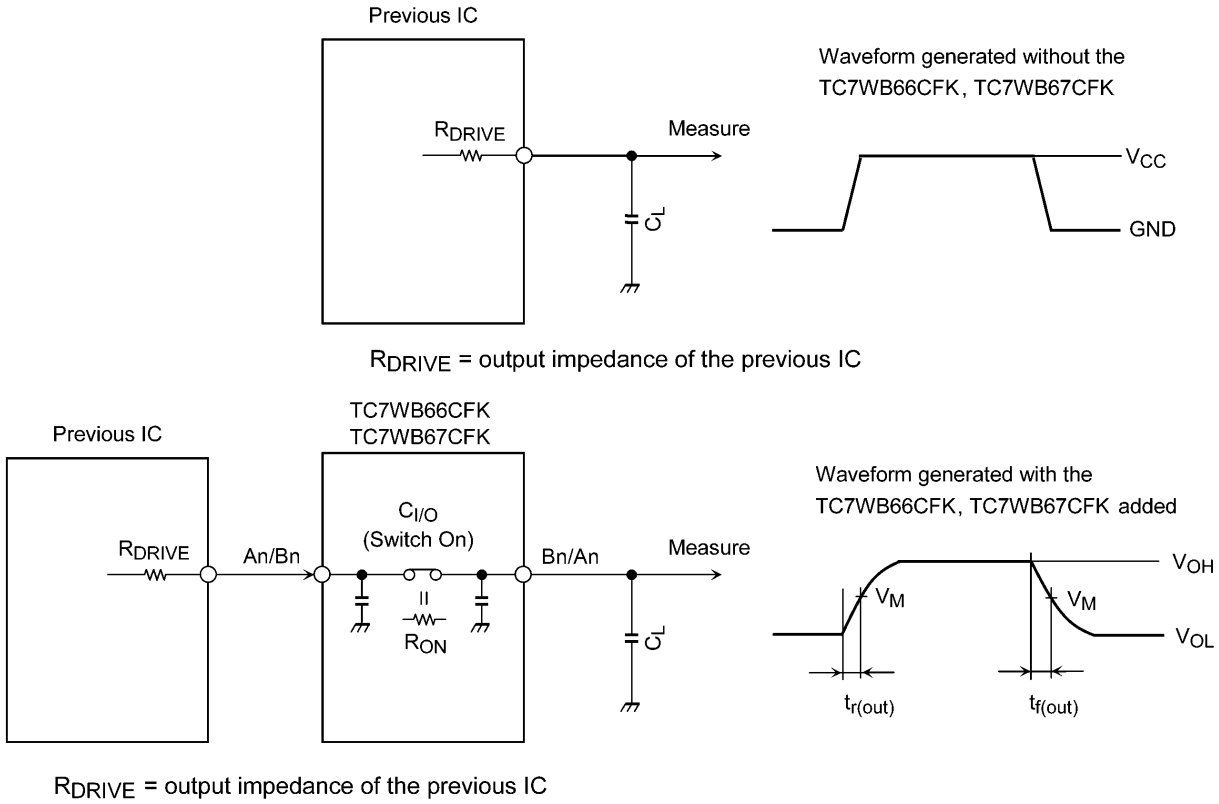



**Fig. 12.1 Calculation Circuit**

**Table 12.1 Calculation Circuit**

| Characteristics | $V_{CC}$ = 5.0 ± 0.5 V | $V_{CC}$ = 3.3 ± 0.3 V | $V_{CC}$ = 2.5 ± 0.2 V | $V_{CC}$ = 1.8 ± 0.15 V |
|---|---|---|---|---|
| $V_M$ | $V_{CC}$/2 | $V_{CC}$/2 | $V_{CC}$/2 | $V_{CC}$/2 |

## 13. Characteristics Curves (Note)

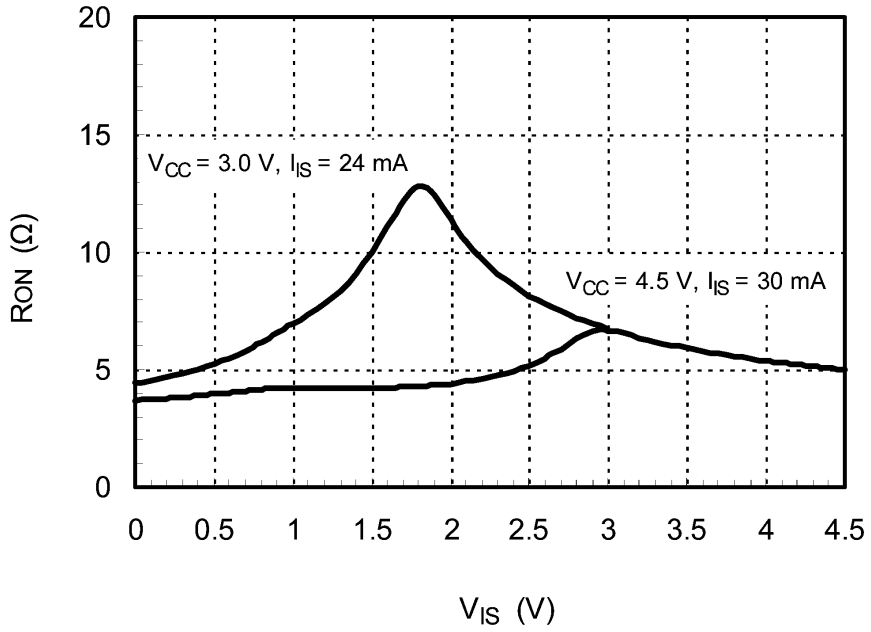
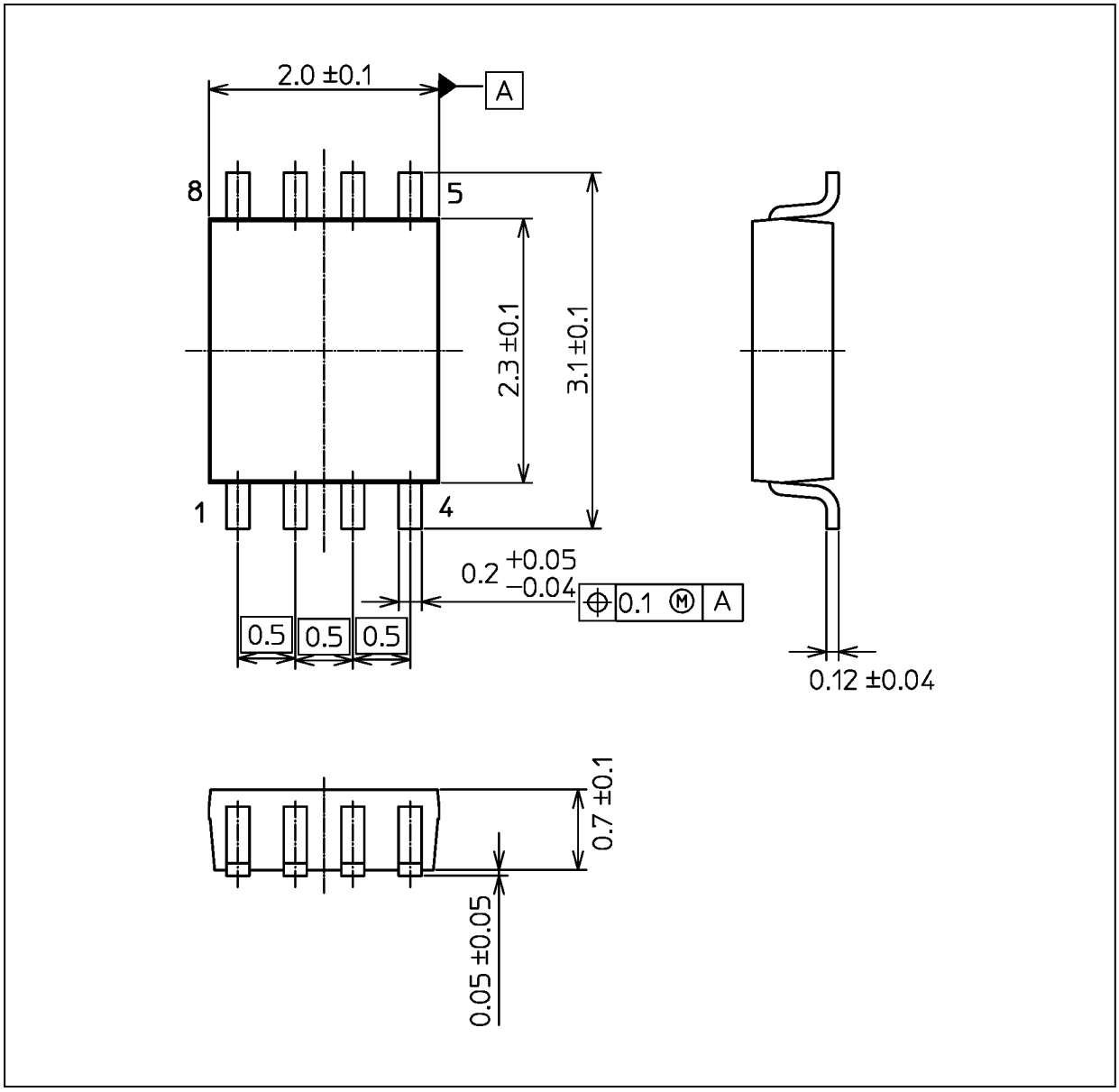



**Fig. 13.1 $R_{ON}$ - $V_{IS}$ (typ.) ($T_a$ = 25 °C)**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## Package Dimensions

Unit: mm




Weight: 0.01 g (typ.)

| Package Name(s) |
| --- |
| Nickname: US8 |

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