

CMOS Digital Integrated Circuits Silicon Monolithic

# TC7WB66CFK, TC7WB66CL8X TC7WB67CFK, TC7WB67CL8X

## 1. Functional Description

- Dual SPST Bus Switch

## 2. General

The TC7WB66CFK/L8X and TC7WB67CFK/L8X are low ON-resistance, high-speed CMOS 2-bit bus switches. These bus switches allow connections or disconnections to be made with minimal propagation delay while maintaining Low power dissipation which is the feature of CMOS.

TC7WB66CFK/L8X requires the output enable (OE) input to be set low to place the output into the high impedance state, whereas the TC7WB67CFK/L8X requires the output enable ( $\overline{\text{OE}}$ ) input to be set high to place the output into the high impedance.

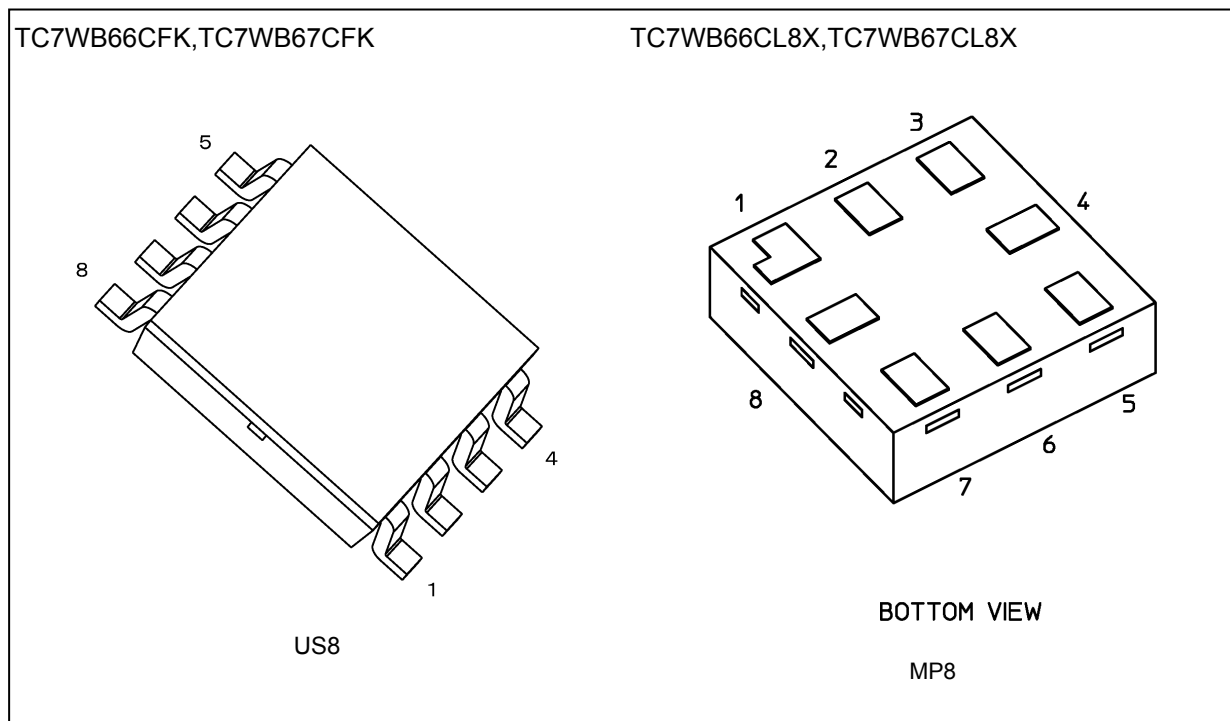
These Bus switches consist of P-MOS and N-MOS structure, meaning these devices are suitable for analog signal transmission.

All inputs are equipped with protector circuits to protect the device from static discharge.

## 3. Features

- (1) Operating voltage:  $V_{CC} = 1.65$  to  $5.5$  V
- (2) ON capacitance:  $C_{IO} = 10$  pF Switch On (typ.) @  $V_{CC} = 5.0$  V
- (3) ON resistance:  $R_{ON} = 4 \Omega$  (typ.) @  $V_{CC} = 4.5$  V,  $V_{IS} = 0$  V
- (4) ESD performance: Machine model  $\geq \pm 200$  V, Human body model  $\geq \pm 2000$  V
- (5) Package: US8, MP8

## 4. Packaging

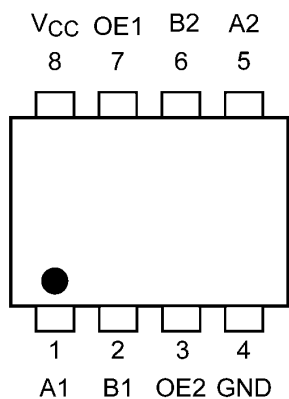


Start of commercial production

2012-10

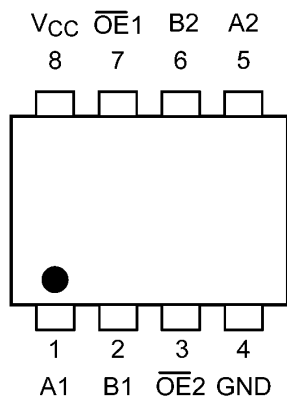
### 5. Pin Assignment

TC7WB66CFK



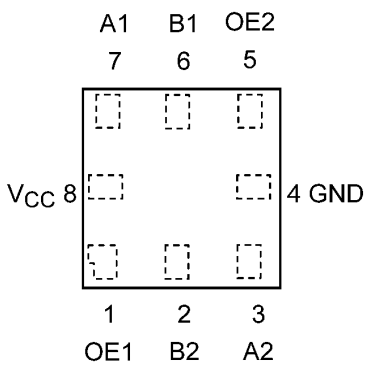
(Top view)

TC7WB67CFK



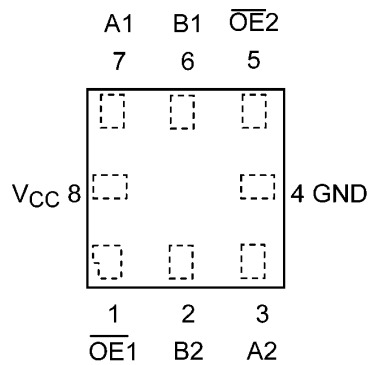
(Top view)

TC7WB66CL8X



(Top view)

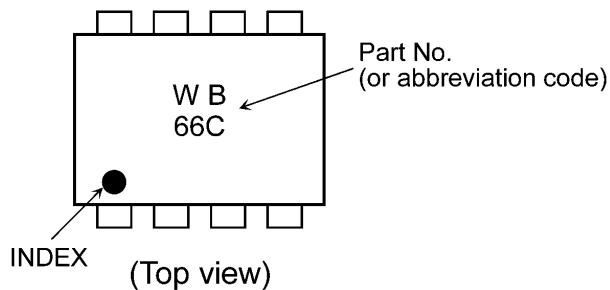
TC7WB67CL8X



(Top view)

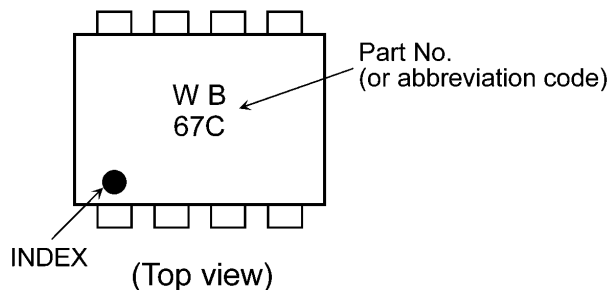
### 6. Marking

TC7WB66CFK



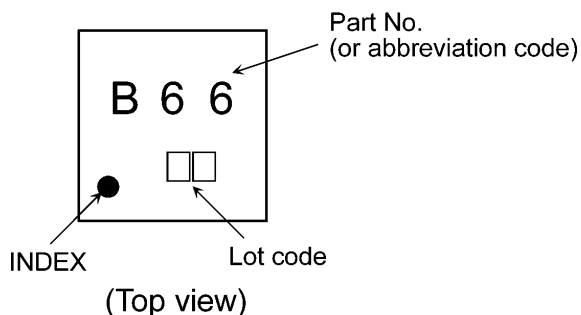
(Top view)

TC7WB67CFK



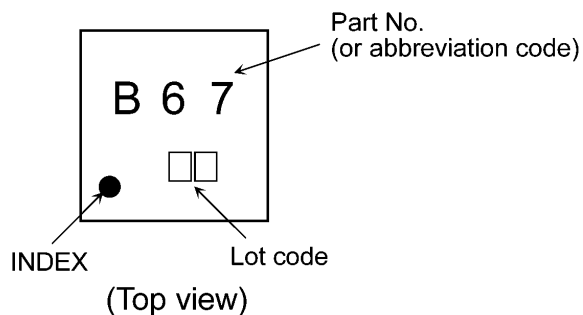
(Top view)

TC7WB66CL8X



(Top view)

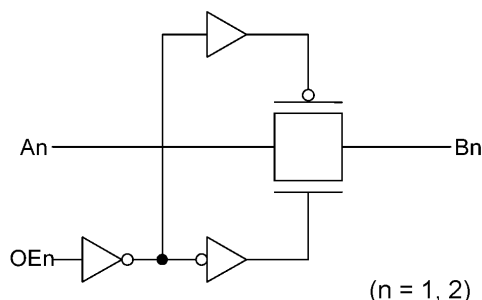
TC7WB67CL8X



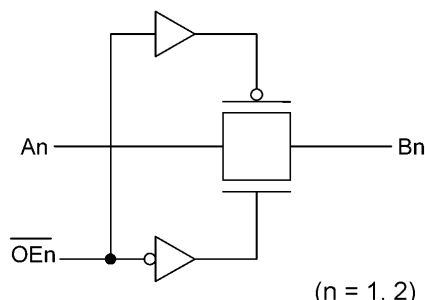
(Top view)

### 7. Block Diagram

TC7WB66CFK, TC7WB66CL8X



TC7WB67CFK, TC7WB67CL8X



### 8. Principle of Operation

#### 8.1. Truth Table

Inputs OE (TC7WB66CFK/L8X)	Inputs $\overline{\text{OE}}$ (TC7WB67CFK/L8X)	Function
H	L	A port = B port
L	H	Disconnect

### 9. Absolute Maximum Ratings (Note)

Characteristics	Part Number	Symbol	Note	Rating	Unit
Supply voltage		$V_{CC}$		-0.5 to 7.0	V
Input voltage ( $\text{OE}$ , $\overline{\text{OE}}$ )		$V_{IN}$		-0.5 to 7.0	
Switch I/O voltage		$V_S$		-0.5 to $V_{CC} + 0.5$	
Clamp diode current		$I_{IK}$		-50	mA
Switch I/O current		$I_S$		50	
Power dissipation	TC7WB66CFK, TC7WB67CFK	$P_D$		200	mW
	TC7WB66CL8X, TC7WB67CL8X		(Note 1)	300	
$V_{CC}$ /ground current		$I_{CC}/I_{GND}$		$\pm 100$	mA
Storage temperature		$T_{stg}$		-65 to 150	$^{\circ}\text{C}$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on an FR4 board

### 10. Operating Ranges (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		1.65 to 5.5	V
Input voltage ( $\text{OE}$ , $\overline{\text{OE}}$ )	$V_{IN}$		0 to 5.5	
Switch I/O voltage	$V_S$		0 to $V_{CC}$	
Operating temperature	$T_{opr}$		-40 to 85	$^{\circ}\text{C}$
Input rise time	$dt/dv$		0 to 10	ns/V
Input fall time	$dt/dv$		0 to 10	

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused control inputs must be tied to either  $V_{CC}$  or GND.

### 11. Electrical Characteristics

#### 11.1. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $85\text{ }^{\circ}\text{C}$ )

Characteristics	Part Number	Symbol	Note	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit
High-level input voltage (OE, $\overline{\text{OE}}$ )		$V_{IH}$		—	1.65 to 1.95	$0.8 \times V_{CC}$	—	—	V
					2.3 to 5.5	$0.7 \times V_{CC}$	—	—	
Low-level input voltage (OE, $\overline{\text{OE}}$ )		$V_{IL}$		—	1.65 to 1.95	—	—	$0.2 \times V_{CC}$	V
					2.3 to 5.5	—	—	$0.3 \times V_{CC}$	
Input leakage current (OE, $\overline{\text{OE}}$ )		$I_{IN}$		$V_{IN} = 0$ to $5.5\text{ V}$	1.65 to 5.5	—	—	$\pm 1.0$	$\mu\text{A}$
Switch OFF-state leakage current	TC7WB66-CFK, TC7WB66-CL8X	$I_{SZ}$		A, B = 0 to $V_{CC}$ , OE = GND	1.65 to 5.5	—	—	$\pm 10$	$\mu\text{A}$
	TC7WB67-CFK, TC7WB67-CL8X			A, B = 0 to $V_{CC}$ , OE = $V_{CC}$	1.65 to 5.5	—	—	$\pm 10$	
ON-resistance		$R_{ON}$	(Note 1), (Note 2)	$V_{IS} = 0\text{ V}$ , $I_{IS} = 30\text{ mA}$	4.5	—	4	7	$\Omega$
				$V_{IS} = 2.4\text{ V}$ , $I_{IS} = 30\text{ mA}$	4.5	—	5	12	
				$V_{IS} = 4.5\text{ V}$ , $I_{IS} = 30\text{ mA}$	4.5	—	6	10	
				$V_{IS} = 0\text{ V}$ , $I_{IS} = 24\text{ mA}$	3.0	—	5	9	
				$V_{IS} = 3.0\text{ V}$ , $I_{IS} = 24\text{ mA}$	3.0	—	7	14	
				$V_{IS} = 0\text{ V}$ , $I_{IS} = 8\text{ mA}$	2.3	—	6	12	
				$V_{IS} = 2.3\text{ V}$ , $I_{IS} = 8\text{ mA}$	2.3	—	9	18	
				$V_{IS} = 0\text{ V}$ , $I_{IS} = 4\text{ mA}$	1.65	—	8	20	
				$V_{IS} = 1.65\text{ V}$ , $I_{IS} = 4\text{ mA}$	1.65	—	15	30	
Quiescent supply current		$I_{CC}$		$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\text{ A}$	5.5	—	—	10	$\mu\text{A}$
		$\Delta I_{CC}$		$V_{IN} = V_{CC} - 0.6\text{ V}$	5.5	—	—	50	

Note 1: All typical values are at  $T_a = 25\text{ }^{\circ}\text{C}$ .

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On-resistance is determined by the lower of the voltages on the two (A or B) pins.

#### 11.2. AC Characteristics (Unless otherwise specified, $T_a = -40$ to $85\text{ }^{\circ}\text{C}$ )

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	Min	Max	Unit
3-state output enable time	$t_{PZL}/t_{PZH}$		See Fig. 11.2.1, 11.2.2, Table 11.2.1	$5.0 \pm 0.5$	—	4	ns
				$3.3 \pm 0.3$	—	6	
				$2.5 \pm 0.2$	—	9	
				$1.8 \pm 0.15$	—	18	
3-state output disable time	$t_{PLZ}/t_{PHZ}$		See Fig. 11.2.1, 11.2.2, Table 11.2.1	$5.0 \pm 0.5$	—	4.5	ns
				$3.3 \pm 0.3$	—	7	
				$2.5 \pm 0.2$	—	9	
				$1.8 \pm 0.15$	—	18	

### 11.3. Capacitive Characteristics (Note) (Unless otherwise specified, $T_a = 25\text{ }^{\circ}\text{C}$ )

Characteristics	Part Number	Symbol	Note	Test Condition	$V_{CC}$ (V)	Typ.	Unit
Input capacitance ( $\overline{\text{OE}}$ , $\overline{\text{OE}}$ )		$C_{IN}$		$V_{IN} = 0\text{ V}$	5.0	4	pF
Switch terminal OFF-capacitance	TC7WB66CFK, TC7WB66CL8X	$C_{I/O}$		$\text{OE} = \text{GND}, V_{I/O} = 0\text{ V}$	5.0	5	pF
	TC7WB67CFK, TC7WB67CL8X			$\overline{\text{OE}} = V_{CC}, V_{I/O} = 0\text{ V}$	5.0	5	
Switch terminal ON-capacitance	TC7WB66CFK, TC7WB66CL8X	$C_{I/O}$		$\text{OE} = V_{CC}, V_{I/O} = 0\text{ V}$	5.0	10	
	TC7WB67CFK, TC7WB67CL8X			$\overline{\text{OE}} = \text{GND}, V_{I/O} = 0\text{ V}$	5.0	10	

Note: Parameter guaranteed by design.

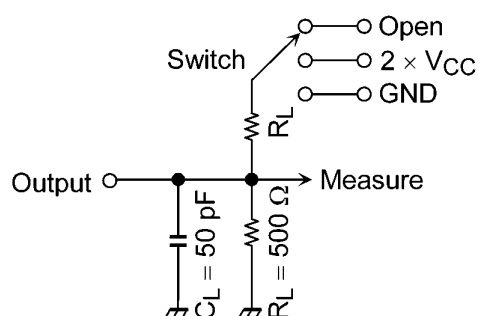


Fig. 11.2.1 AC Test Circuit

Table 11.2.1 Parameter for AC Test Circuit

Parameter	Switch
$t_{PLZ}$ , $t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}$ , $t_{PZH}$	GND

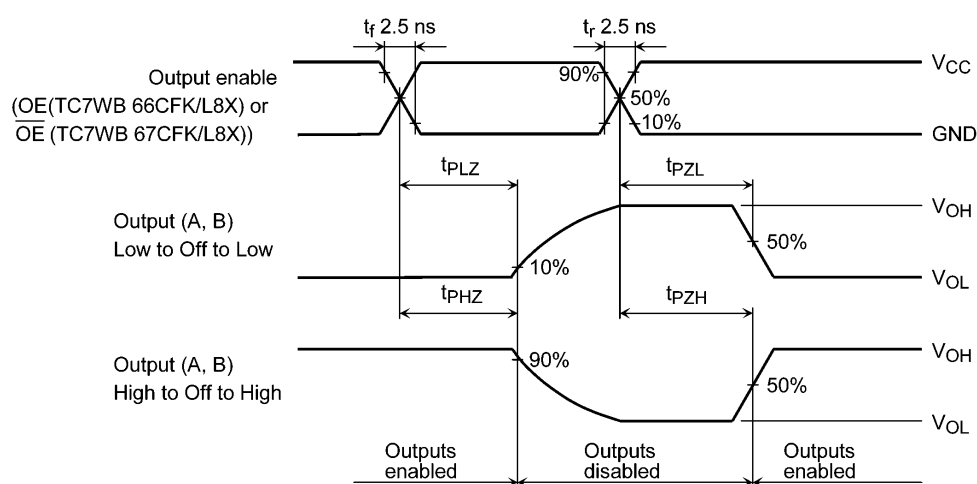


Fig. 11.2.2 AC Waveform  $t_{PLZ}$ ,  $t_{PHZ}$ ,  $t_{PZL}$ ,  $t_{PZH}$

### 12. Rise and Fall Time ( $t_r/t_f$ )

The  $t_{r(out)}$  and  $t_{f(out)}$  values of the output signals are affected by the CR time constant of the input, which consists of the switch terminal capacitance ( $C_{I/O}$ ) and the on-resistance ( $R_{ON}$ ) of the input.

In practice, the  $t_{r(out)}$  and  $t_{f(out)}$  values are also affected by the circuit's capacitance and resistance components other than the capacitance of TC7WB66CFK/L8X, TC7WB67CFK/L8X

The  $t_r/t_{f(out)}$  values can be approximated as follows.

(Figure 12.1, Table 12.1 shows the test circuit.)

$$t_r/t_{f(out)} (\text{approx}) = - (C_{I/O} + C_L) \cdot (R_{DRIVE} + R_{ON}) \cdot \ln (((V_{OH} - V_{OL}) \cdot V_M) / (V_{OH} - V_{OL}))$$

Where,  $R_{DRIVE}$  is the output impedance of the previous-stage circuit.

Calculation example:

$$t_{r(out)} (\text{approx}) = - (10 + 15) \text{ E } - 12 \cdot (120 + 4) \cdot \ln (((4.5 - 0) \cdot 2.25) / (4.5 - 0)) = \approx 2.1 \text{ ns}$$

Calculation conditions:

$V_{CC} = 4.5 \text{ V}$ ,  $C_L = 15 \text{ pF}$ ,  $R_{DRIVE} = 120 \Omega$  (output impedance of the previous IC),  $V_M = 2.25 \text{ V}$  ( $V_{CC}/2$ )

Output of the previous IC = digital (i.e., high-level voltage =  $V_{CC}$ , low-level voltage = GND)

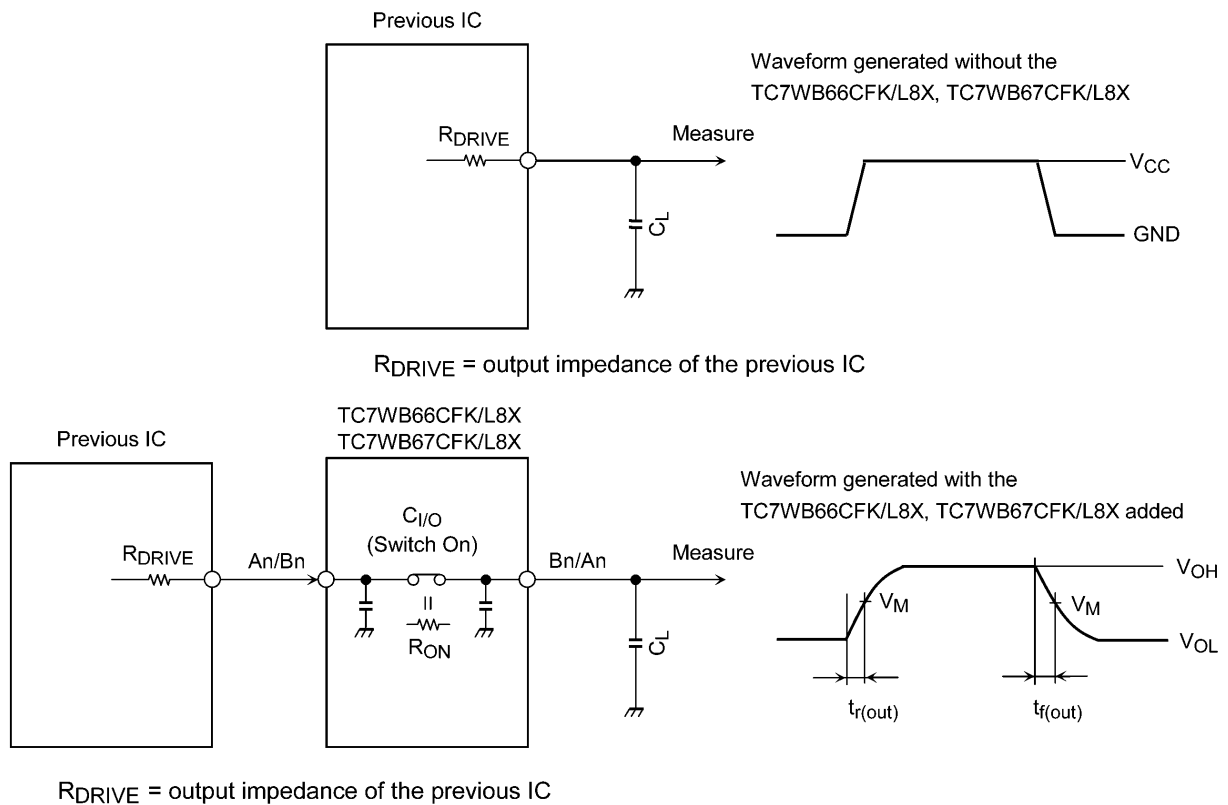


Fig. 12.1 Calculation Circuit

Table 12.1 Calculation Circuit

Characteristics	$V_{CC} = 5.0 \pm 0.5 \text{ V}$	$V_{CC} = 3.3 \pm 0.3 \text{ V}$	$V_{CC} = 2.5 \pm 0.2 \text{ V}$	$V_{CC} = 1.8 \pm 0.15 \text{ V}$
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$

## 13. Characteristics Curves (Note)

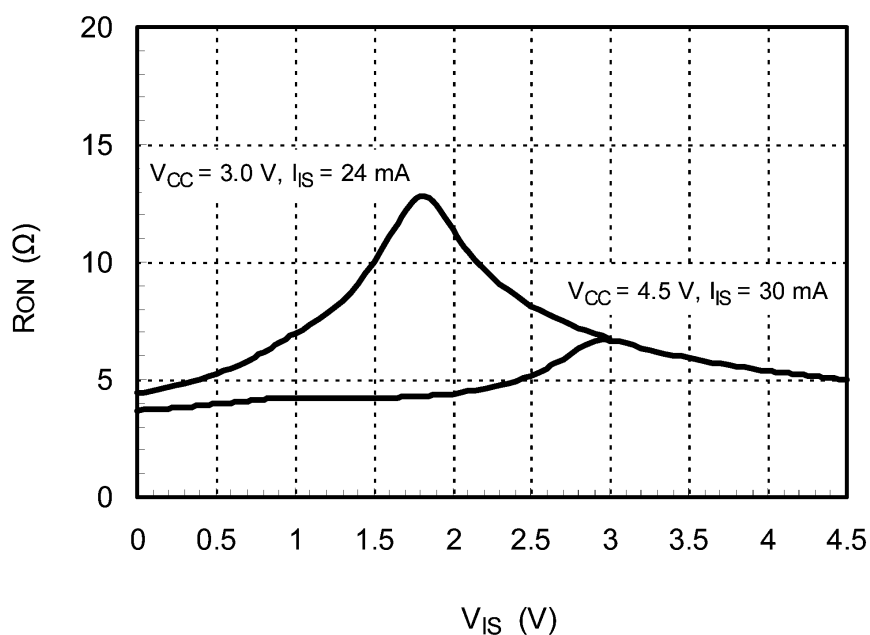
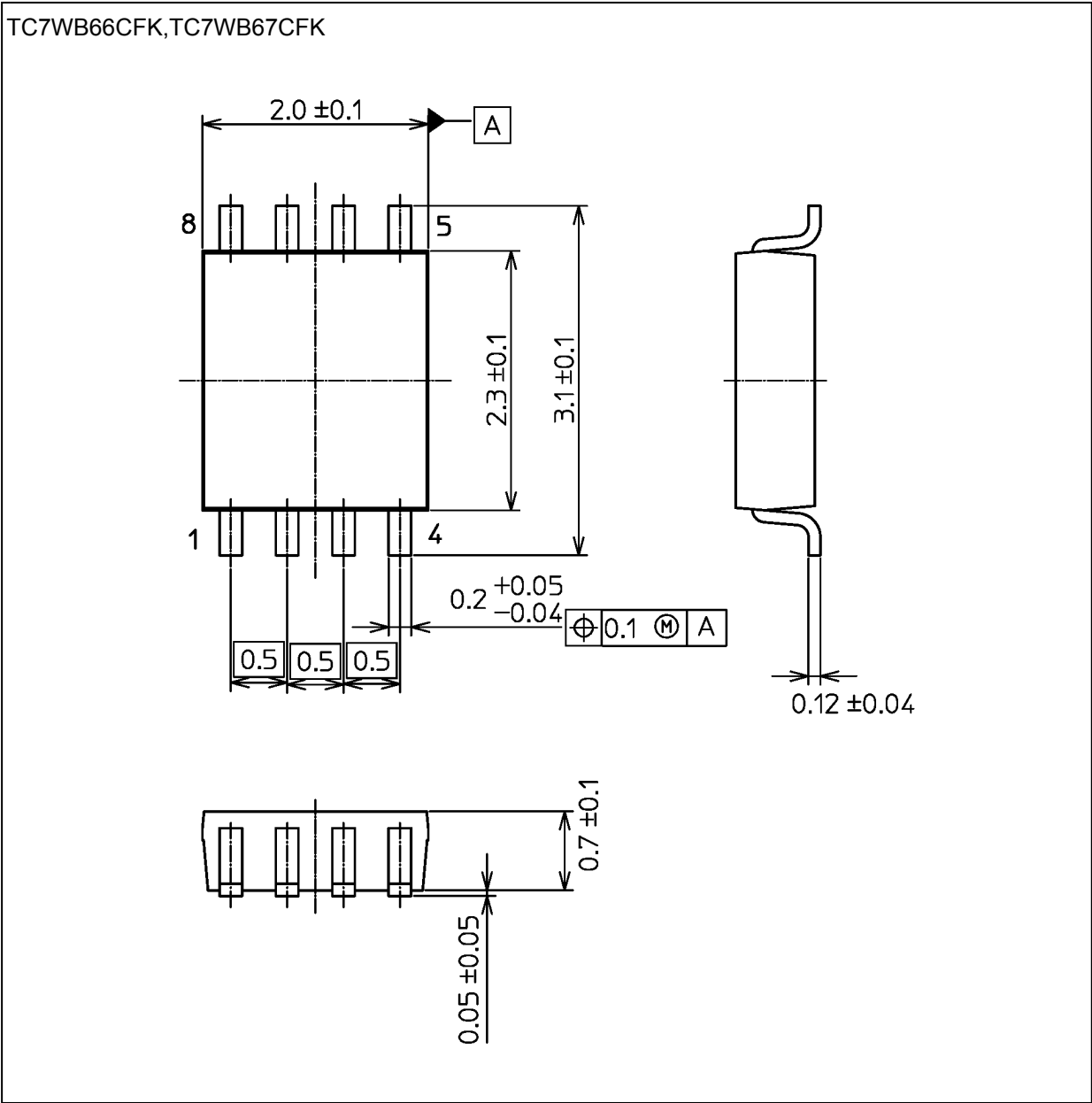


Fig. 13.1  $R_{ON} - V_{IS}$

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



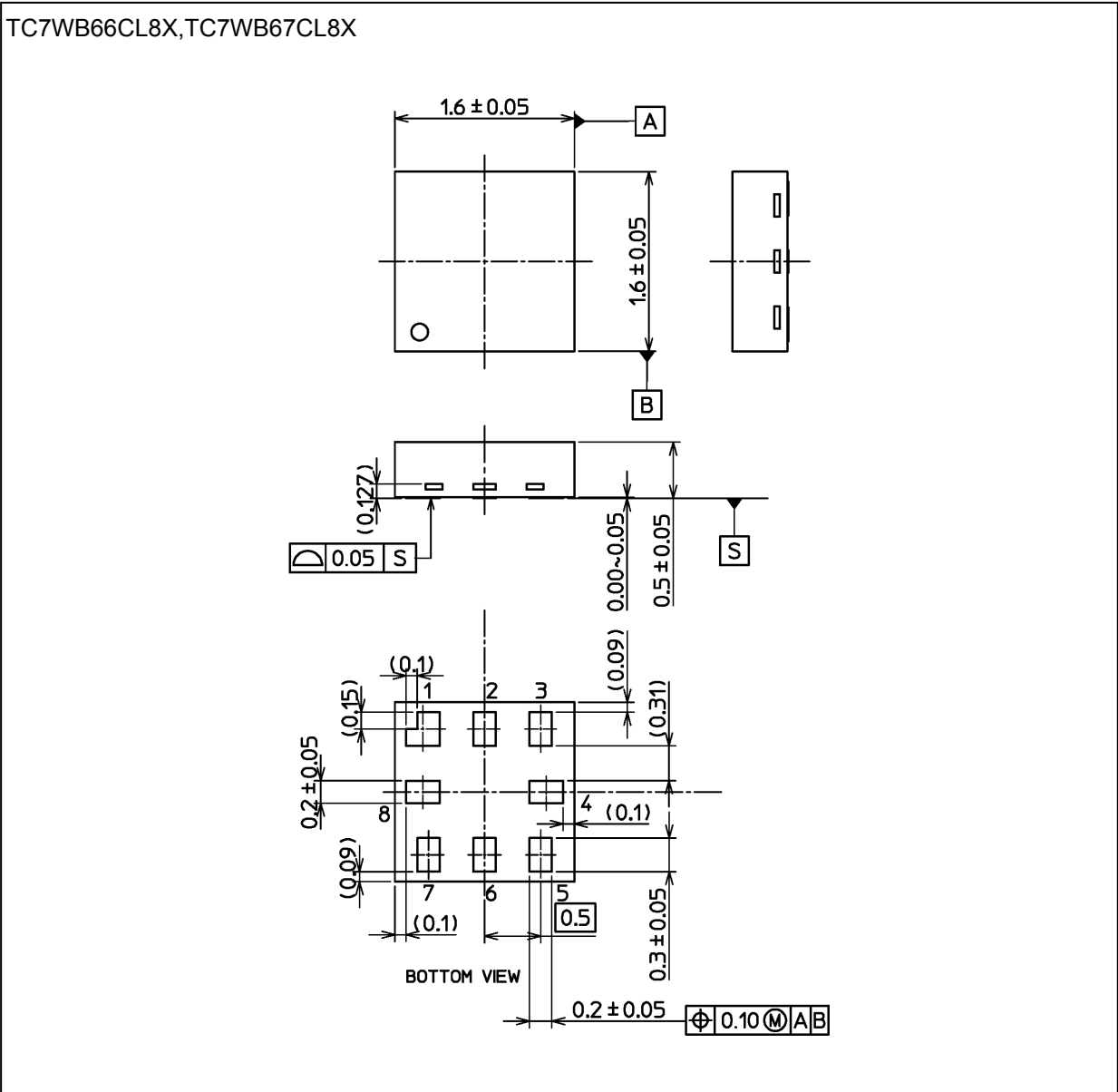
Weight: 0.01 g (typ.)

Package Name(s)
Nickname: US8



Package Dimensions

Unit: mm



Weight: 0.0039 g (typ.)

Package Name(s)
Nickname: MP8

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