

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC7W126FU

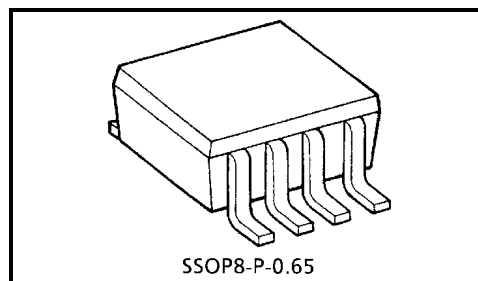
## Dual BUS Buffer

The TC7W126FU is a high speed C<sup>2</sup>MOS Dual BUS Buffers fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the C<sup>2</sup>MOS low power dissipation.

The require 3-state control input G to be set low to place the output into the high impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



SSOP8-P-0.65

Weight: 0.02 g (typ.)

## Features

- High speed:  $t_{pd} = 10 \text{ ns}$  (typ.) at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 2 \text{ } \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 6 \text{ mA}$  (min)
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} \text{ (opr)} = 2 \text{ to } 6 \text{ V}$

## Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

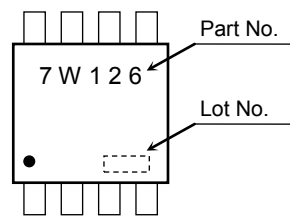
Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 35$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 37.5$	mA
Power dissipation	$P_D$	300	mW
Storage temperature range	$T_{stg}$	-65 to 150	$^\circ\text{C}$
Lead temperature (10 s)	$T_L$	260	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

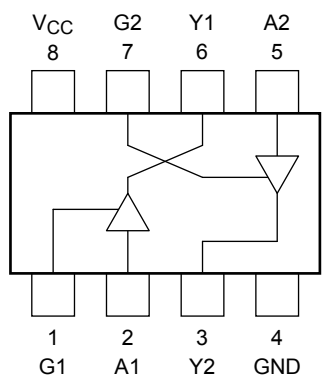
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production  
1993-07

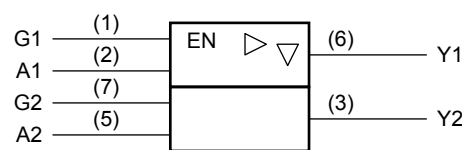
Marking



Pin Configuration (top view)



Logic Diagram



Truth Table

Inputs		Output
G	A	Y
L	X	Z
H	L	L
H	H	H

X: Don't care  
Z: High impedance

Operating Ranges

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	2 to 6	V
Input voltage	V <sub>IN</sub>	0 to V <sub>CC</sub>	V
Output voltage	V <sub>OUT</sub>	0 to V <sub>CC</sub>	V
Operating temperature range	T <sub>opr</sub>	-40 to 85	°C
Input rise and fall time	t <sub>r</sub> , t <sub>f</sub>	0 to 1000 (V <sub>CC</sub> = 2.0 V)	ns
		0 to 500 (V <sub>CC</sub> = 4.5 V)	
		0 to 400 (V <sub>CC</sub> = 6.0 V)	

**Electrical Characteristics**
**DC Electrical Characteristics**

Characteristics		Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit				
					V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max			
Input voltage	High level	V <sub>IH</sub>	—		2.0	1.5	—	—	1.5	—	V			
					4.5	3.15	—	—	3.15	—				
					6.0	4.2	—	—	4.2	—				
	Low level	V <sub>IL</sub>	—		2.0	—	—	0.5	—	0.5				
					4.5	—	—	1.35	—	1.35				
					6.0	—	—	1.8	—	1.8				
Output voltage	High level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub>	I <sub>OH</sub> = -20 μA	2.0	1.9	2.0	—	1.9	—	V			
					4.5	4.4	4.5	—	4.4	—				
					6.0	5.9	6.0	—	5.9	—				
				I <sub>OH</sub> = -6 mA	4.5	4.18	4.31	—	4.13	—				
					I <sub>OH</sub> = -7.8 mA	6.0	5.68	5.80	—	5.63		—		
						Low level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2.0		—	0	0.1
	4.5	—	0	0.1						—		0.1		
	6.0	—	0	0.1	—					0.1				
	I <sub>OL</sub> = 6 mA	4.5	—	0.17	0.26				—	0.33				
		I <sub>OL</sub> = 7.8 mA	6.0	—	0.18				0.26	—		0.33		
			3-state output off-state current		I <sub>OZ</sub>				V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND			6.0	—	—
	Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	±0.1	—		±1.0	μA	
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	2.0	—	20.0	μA			

**AC Electrical Characteristics (input  $t_r = t_f = 6$  ns)**

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
			C <sub>L</sub>	V <sub>CC</sub> (V)	Min	Typ.	Max	Min	Max	
Output transition time	$t_{TLH}$ $t_{THL}$	—	50	2.0	—	20	60	—	75	ns
				4.5	—	6	12	—	15	
				6.0	—	5	10	—	13	
Propagation delay time	$t_{pLH}$ $t_{pHL}$	—	50	2.0	—	30	90	—	115	ns
				4.5	—	11	18	—	23	
				6.0	—	10	15	—	20	
			150	2.0	—	42	130	—	165	
				4.5	—	14	26	—	33	
				6.0	—	12	22	—	28	
Output enable time	$t_{pZL}$ $t_{pZH}$	$R_L = 1$ k $\Omega$	50	2.0	—	30	90	—	115	ns
				4.5	—	11	18	—	23	
				6.0	—	10	15	—	20	
			150	2.0	—	42	130	—	165	
				4.5	—	14	26	—	33	
				6.0	—	12	22	—	28	
Output disable time	$t_{pLZ}$ $t_{pHZ}$	$R_L = 1$ k $\Omega$	50	2.0	—	24	100	—	125	ns
				4.5	—	12	20	—	25	
				6.0	—	10	17	—	21	
Input capacitance	C <sub>IN</sub>	—	—	—	—	5	10	—	10	pF
Output capacitance	C <sub>OUT</sub>	—	—	—	—	10	—	—	—	pF
Power dissipation capacitance	C <sub>PD</sub>	(Note)	—	—	—	41	—	—	—	pF

Note: C<sub>PD</sub> is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load.

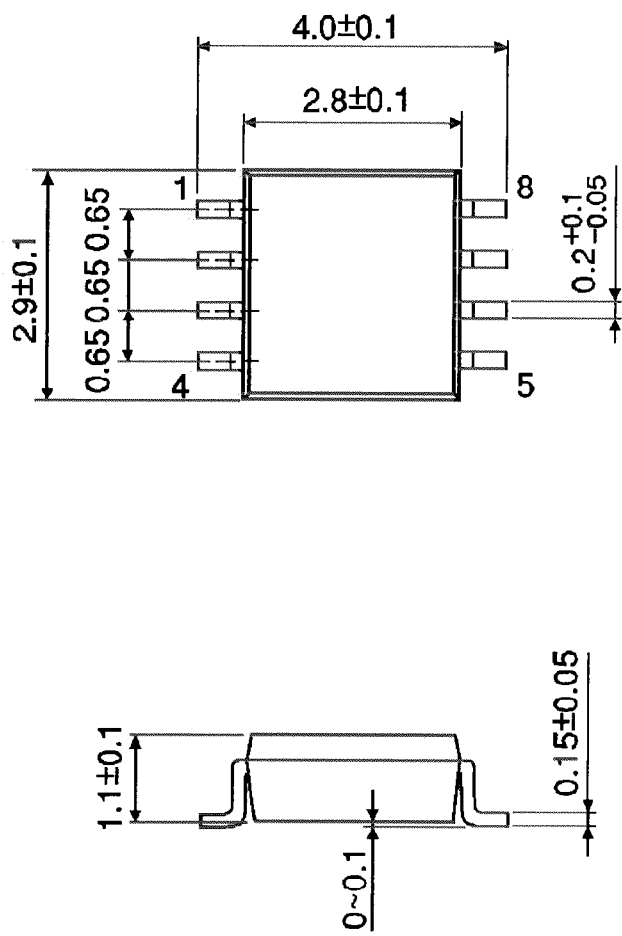
Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per gate)}$$

Package Dimensions

SSOP8-P-0.65

Unit : mm



Weight: 0.02 g (typ.)

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