

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7QPB9306FK, TC7QPB9307FK

Low Voltage / Low Power 4-Bit Dual Supply Bus Switch

The TC7QPB9306FK and TC7QPB9307FK are CMOS 4-bit dual-supply bus switches that can provide an interface between two nodes at different voltage levels. These devices can be connected to two independent power supplies. V_{CCA} supports 1.8 V, 2.5 V and 3.3 V power supplies, whereas V_{CCB} supports 2.5 V, 3.3 V and 5.0 V power supplies.

Bidirectional level-shifting is possible by simply adding external pull-up resistors between the An/Bn data lines and the V_{CCA} / V_{CCB} supplies. There is no restriction on the relative magnitude of the An and Bn voltages; both the An and Bn data lines can be pulled up to arbitrary power supplies.

The enable signal can be used to disable the device so that the buses are effectively isolated.

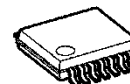
The Output Enable (OE:TC7QPB9306FK, \overline{OE} :TC7QPB9307FK) input is common for all the 4-bits of the data lines; thus these device are used as a single 4-bits bus switch. For the TC7QPB9306FK, Output Enable (OE) is active-High: When OE is High, the switch is on; when Low, the switch is off. For the TC7QPB9307FK, Output Enable (\overline{OE}) is active-Low: When \overline{OE} is Low, the switch is on; when High, the switch is off.

The TC7QPB9306FK and TC7QPB9307FK supports power-down protection at the \overline{OE} , OE input, with \overline{OE} , OE being 5.5 V tolerant.

The channels consist of n-type MOSFETs.

All the inputs provide protection against electrostatic discharge.

TC7QPB9306FK, TC7QPB9307FK



VSSOP14-P-0030-0.50

Weight

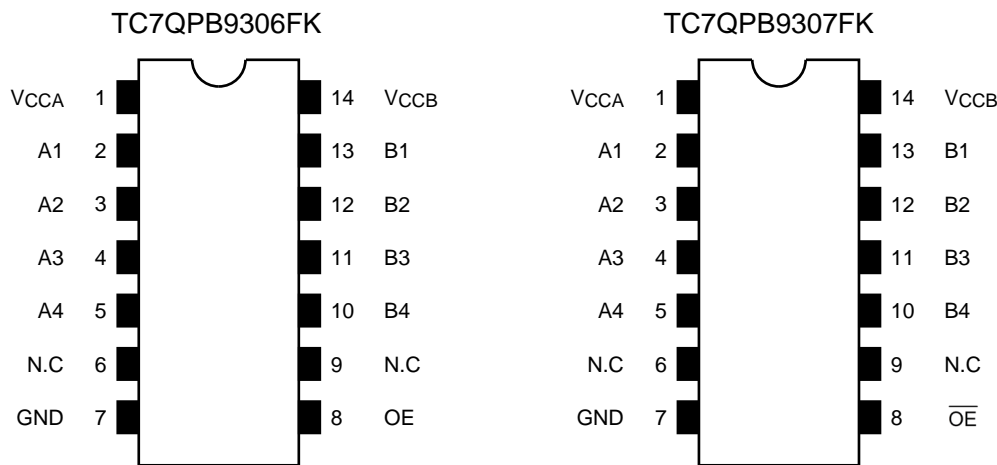
VSSOP14-P-0030-0.50 : 0.02 g (typ.)

Features

- Operating voltage: 1.8 V to 2.5 V, 1.8 V to 3.3 V, 1.8 V to 5.0 V, 2.5 V to 3.3 V, 2.5 V to 5.0 V, 3.3 V to 5.0 V bidirectional interface
- Operating voltage: V_{CCA} = 1.65 to 5.0 V, V_{CCB} = 2.3 to 5.5 V
- Low ON-resistance: R_{ON} = 5.0 Ω (typ.) @ V_{IS} = 0 V, I_{IS} = 30 mA, V_{CCA} = 3.0 V, V_{CCB} = 4.5 V
- ESD performance: Machine model $\geq \pm 200$ V
Human body model $\geq \pm 2000$ V
- 5.5 V tolerance and power-down protection at the Output Enable input.
- Packages: VSSOP14(US14)

Start of commercial production
2009-09

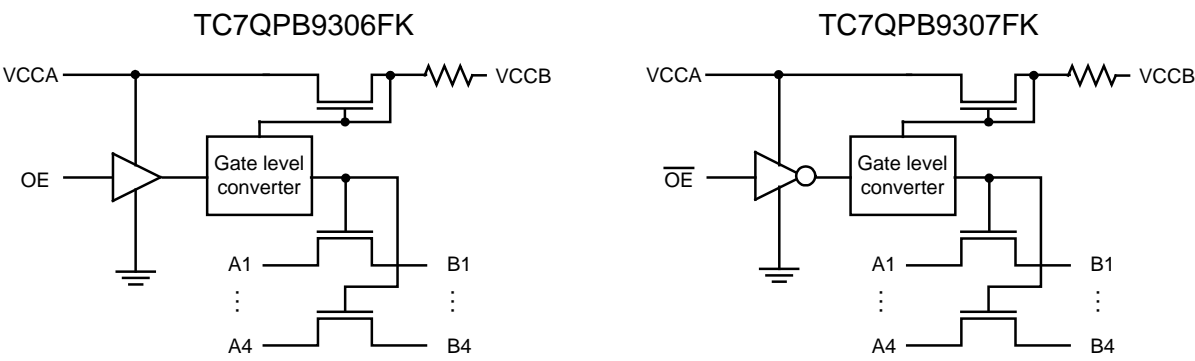
Pin Assignment (top view)



Truth Table

Inputs(9306)	Function	Inputs(9307)	Function
OE		$\overline{\text{OE}}$	
L	Disconnect	L	A port = B port
H	A port = B port	H	Disconnect

Circuit Schematic



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CCA}	-0.5 to 7.0	V
	V _{CCB}	-0.5 to 7.0	
Control input voltage	V _{IN}	-0.5 to 7.0	V
Switch input/output voltage	V _S	-0.5 to 7.0	V
Clamp diode current	I _{IK}	-50	mA
Switch input/output current	I _S	64	mA
DC V _{CC} /ground current per supply pin	I _{CCA}	±25	mA
	I _{CCB}	±25	
Power dissipation	P _D	180	mW
Storage temperature	T _{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Power supply voltage (Note 1)	V _{CCA}	1.65 to 5.0	V
	V _{CCB}	2.3 to 5.5	
Control input voltage	V _{IN}	0 to 5.5	V
Switch input/output voltage	V _S	0 to 5.5	V
Operating temperature	T _{opr}	-40 to 85	°C
Control input rise and fall times	dt/dv	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either V_{CCA} or GND.

Note 1: The V_{CCA} voltage must be lower than the V_{CCB} voltage.

Application Circuit

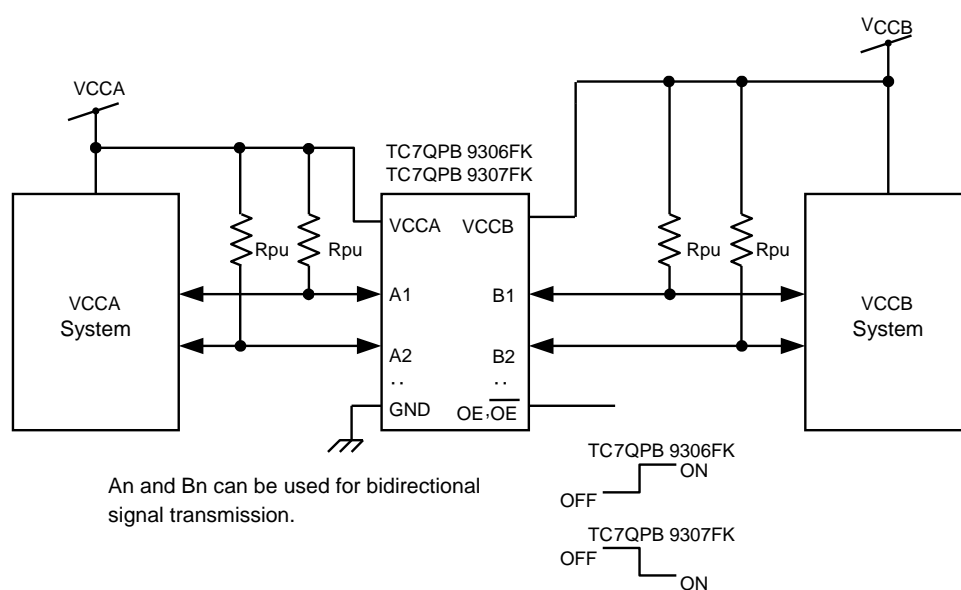


Figure 1 Application Circuit Diagram

The V_{CCA} voltage must be lower than the V_{CCB} voltage.

Level-shifting functionality is enabled by adding pull-up resistors from A_n to V_{CCA} or V_{CCB} and from B_n to V_{CCB} or V_{CCA} , respectively.

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

Characteristics		Symbol	Test Condition	V _{CCA} (V)	V _{CCB} (V)	Min	Max	Unit
Control input voltage	High-level	V _{IH}	—	1.65 ≤ V _{CCA} < 2.3	V _{CCA} to 5.5	0.8 × V _{CCA}	—	V
				2.3 ≤ V _{CCA} < 5.0	V _{CCA} to 5.5	0.7 × V _{CCA}	—	
	Low-level	V _{IL}	—	1.65 ≤ V _{CCA} < 2.3	V _{CCA} to 5.5	—	0.2 × V _{CCA}	
				2.3 ≤ V _{CCA} < 5.0	V _{CCA} to 5.5	—	0.3 × V _{CCA}	
ON-resistance (Note 1)	R _{ON}	V _{IS} = 0 V, I _{IS} = 30 mA (Figure 2)	—	1.65	2.3	—	16.0	Ω
				2.3	3.0	—	11.0	
				3.0	4.5	—	8.0	
Power off leakage current	I _{OFF}	An, Bn = 0 to 5.5 V (per circuit)	—	0	0	—	±1.0	μA
Switch-off leakage current	I _{SZ}	An, Bn = 0 to 5.5 V $\overline{\text{OE}} = \text{V}_{\text{CCA}}, \text{OE} = \text{GND}$	—	1.65 to 5.0	V _{CCA} to 5.5	—	±1.0	μA
Control input current	I _{IN}	OE, $\overline{\text{OE}}$ = 0 to 5.5V	—	1.65 to 5.0	V _{CCA} to 5.5	—	±1.0	μA
leakage current from V _{CCB} to V _{CCA}	I _{CCBA}	OE, $\overline{\text{OE}}$ = GND or V _{CCA} V _{CCB} → V _{CCA}	—	3.3	5.0	—	20.0	μA
Quiescent supply current	I _{CCA1}	OE, $\overline{\text{OE}}$ = V _{CCA} or GND, I _{IS} = 0 A	—	1.65 to 5.0	V _{CCA}	—	4.0	μA
	I _{CCB1}	OE, $\overline{\text{OE}}$ = V _{CCA} or GND, I _{IS} = 0 A	—	1.65 to 5.0	V _{CCA}	—	4.0	
	I _{CCA2}	V _{CCA} ≤ OE, $\overline{\text{OE}}$ ≤ 5.5 V, I _{IS} = 0 A	—	1.65 to 5.0	V _{CCA}	—	±4.0	
	I _{CCB2}	V _{CCA} ≤ OE, $\overline{\text{OE}}$ ≤ 5.5 V, I _{IS} = 0 A	—	1.65 to 5.0	V _{CCA}	—	±4.0	

Note 1: ON-resistance is measured by measuring the voltage drop across the switch at the indicated current.

Level Shift Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition	V _{CCA} (V)	V _{CCB} (V)	Min	Max	Unit
Input/Output Characteristics (Up Translation) (Note 1)	V _{OHU}	An = V _{IN} SW = ON (Figure 7)	1.65	3.0 to 5.5	1.4	—	V
			2.3	4.5 to 5.5	2.05	—	
			3.0	4.5 to 5.5	2.7	—	
Input/Output Characteristics (Down Translation) (Note 2)	V _{OHD}	An = V _{CCA} SW = ON (Figure 9)	1.65	3.0 to 5.5	1.3	1.65	
			2.3	4.5 to 5.5	1.95	2.3	
			3.0	4.5 to 5.5	2.6	3.0	

Note 1: The Input/Output Characteristics for up translation indicate the input voltages required to provide V_{CCA} + 0.5 V on the outputs when measured using the test circuitry shown in Figure 7.

Note 2: The Input/Output Characteristics for down translation indicate the voltages that cause the output voltages to saturate when measured using the test circuitry shown in Figure 9.

AC Characteristics (Ta = -40 to 85°C, Input: tr = tr = 2.0 ns, f = 10 kHz)

VCCA = 3.3 ± 0.3 V, VCCB = 5.0 ± 0.5 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bus to Bus)	tpLH	Figure 3, Figure 5 (Note 1)	—	0.3	ns
Propagation delay time (Bus to Bus)	tpHL	Figure 3, Figure 5 (Note 1)	—	1.2	
Output enable time	tpZL	Figure 4, Figure 6	—	9.0	
Output disable time	tpLZ	Figure 4, Figure 6	—	11.0	

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

VCCA = 2.5 ± 0.2 V, VCCB = 5.0 ± 0.5 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bus to Bus)	tpLH	Figure 3, Figure 5 (Note 1)	—	0.35	ns
Propagation delay time (Bus to Bus)	tpHL	Figure 3, Figure 5 (Note 1)	—	1.8	
Output enable time	tpZL	Figure 4, Figure 6	—	13.0	
Output disable time	tpLZ	Figure 4, Figure 6	—	15.0	

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

VCCA = 2.5 ± 0.2 V, VCCB = 3.3 ± 0.3 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bus to Bus)	tpLH	Figure 3, Figure 5 (Note 1)	—	0.45	ns
Propagation delay time (Bus to Bus)	tpHL	Figure 3, Figure 5 (Note 1)	—	2.2	
Output enable time	tpZL	Figure 4, Figure 6	—	17.0	
Output disable time	tpLZ	Figure 4, Figure 6	—	19.0	

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	VCCA (V) VCCB (V)		Typ.	Unit
Control input capacitance	CIN	—	3.3	3.3	3	pF
Switch input/output capacitance	CI/O	SW = ON	3.3	3.3	14	
		SW = OFF	3.3	3.3	7	

DC Test Circuit

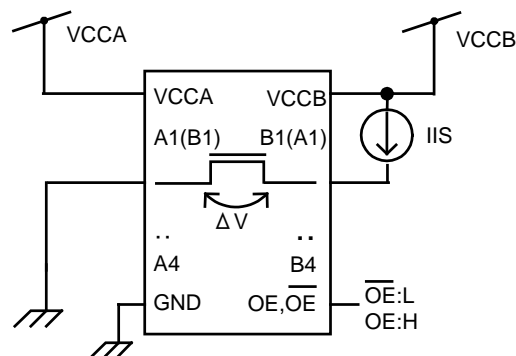


Figure 2 ON-resistance Test Circuits

AC Test Circuits

•tpLH, HL

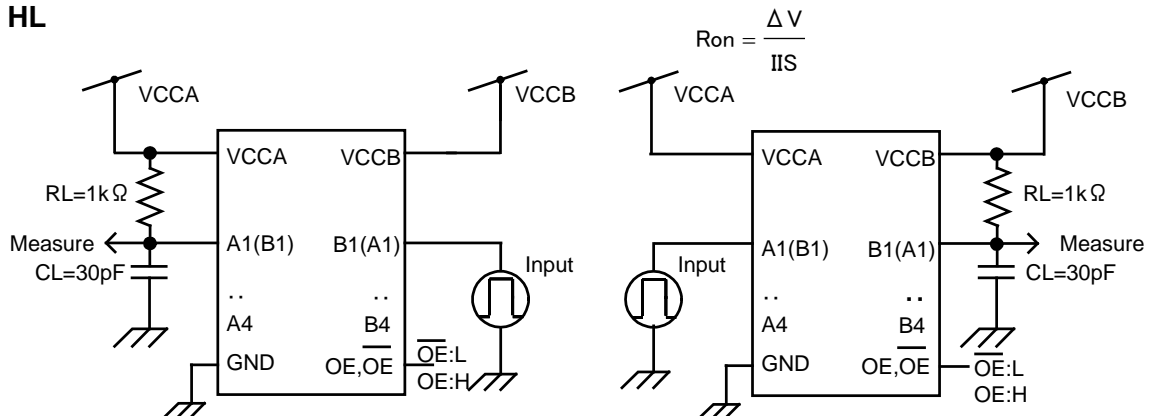


Figure 3 tpLH, tpHL Test Circuits

•tpLZ, ZL

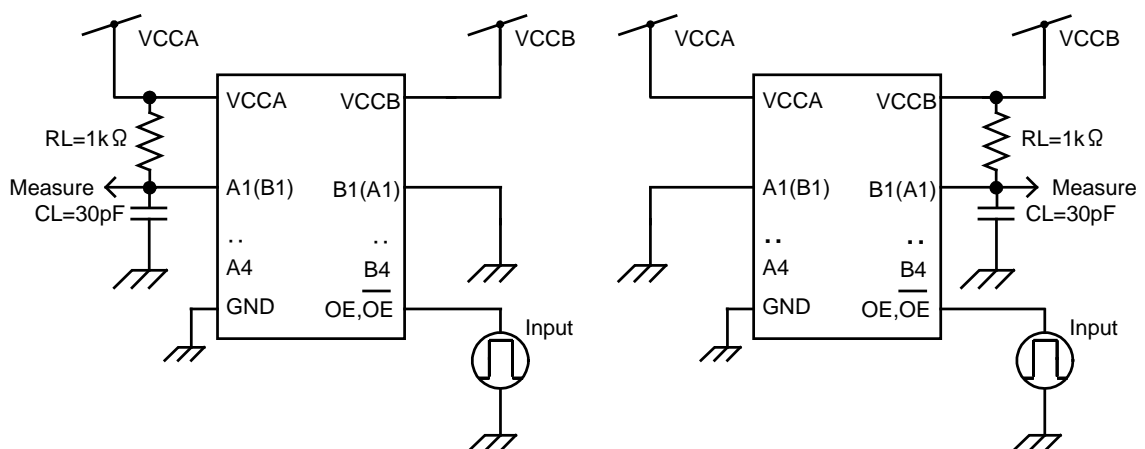


Figure 4 tpLZ, tpZL Test Circuits

AC Waveform

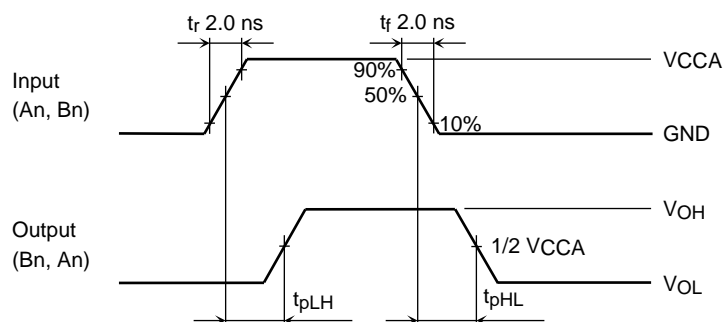


Figure 5 t_{pLH} , t_{pHL}

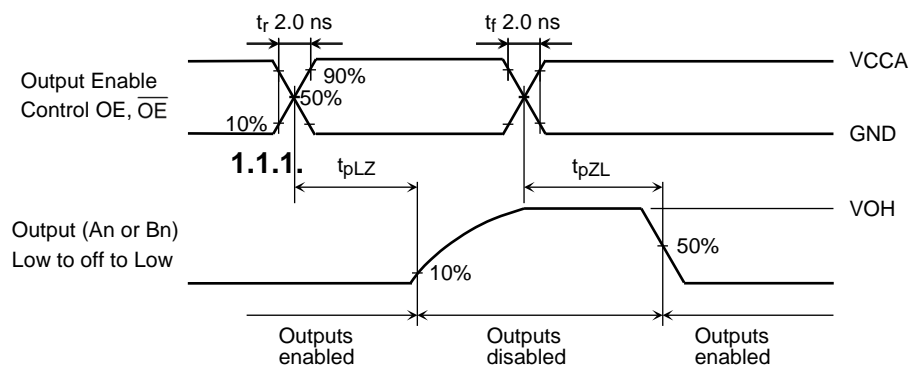


Figure 6 t_{pLZ} , t_{pZL}

Level Shift Function (Used Pull-up Resistance)

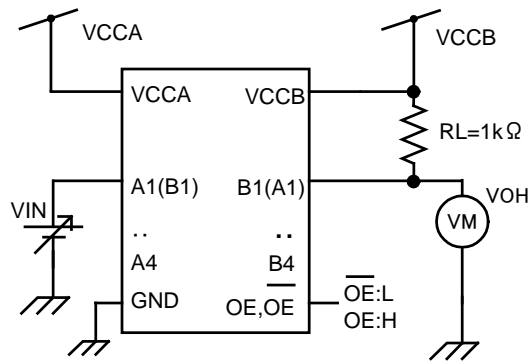


Figure 7 Test Circuit

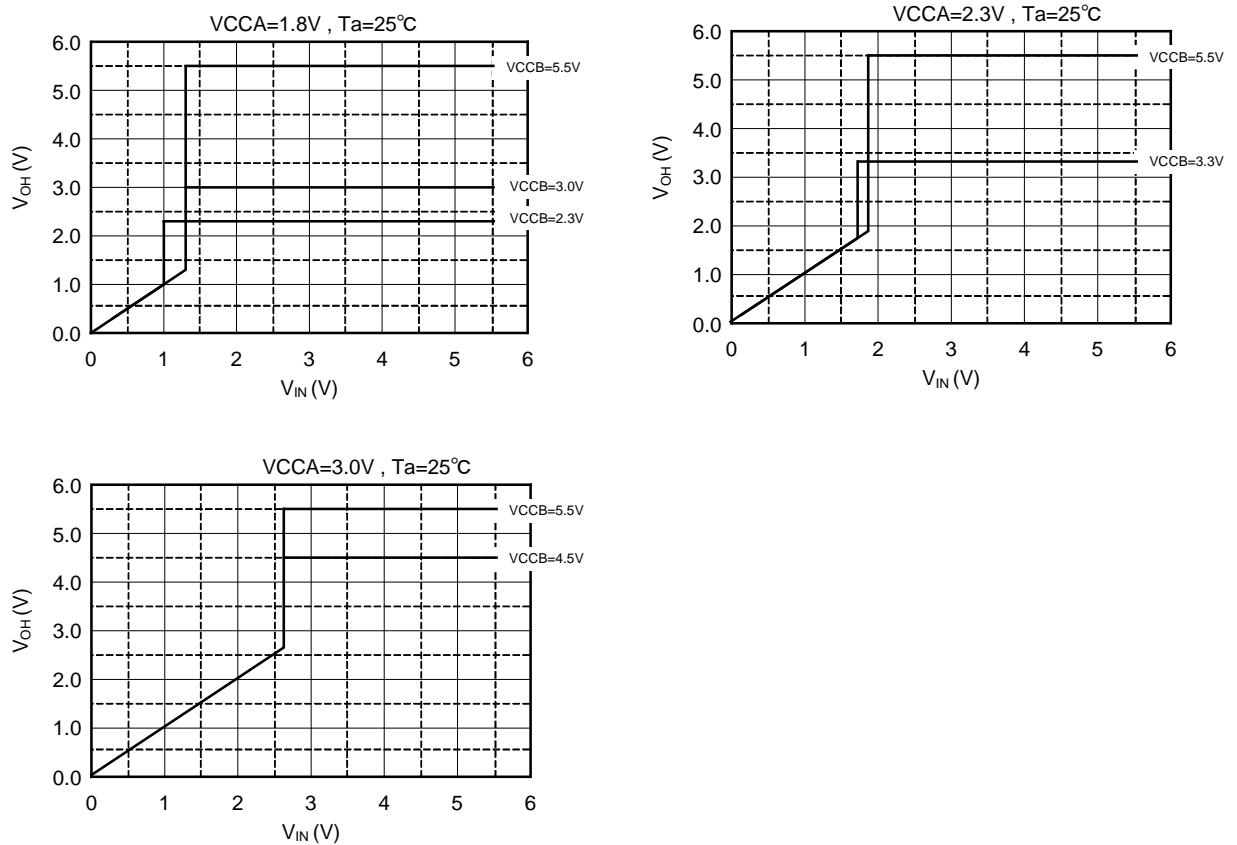


Figure 8 Input/Output Characteristics (Typ.)

Level Shift Function (Unused Pull-up Resistance)

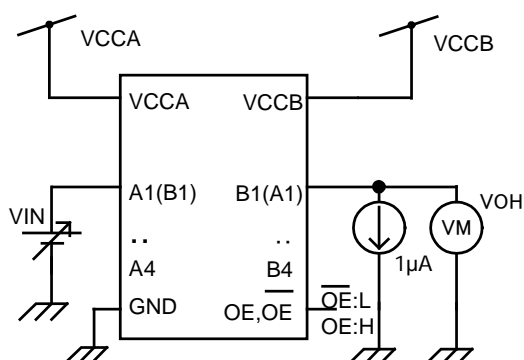


Figure 9 Test Circuit

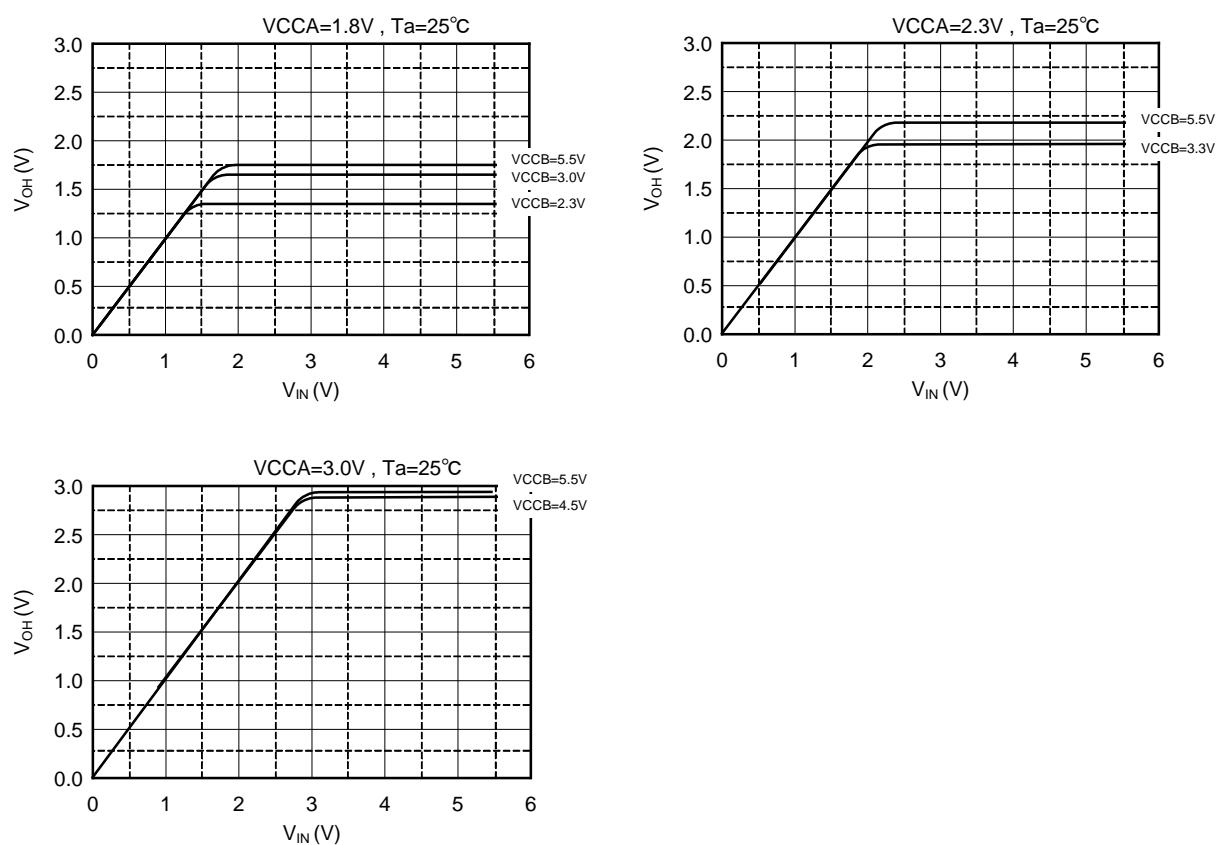
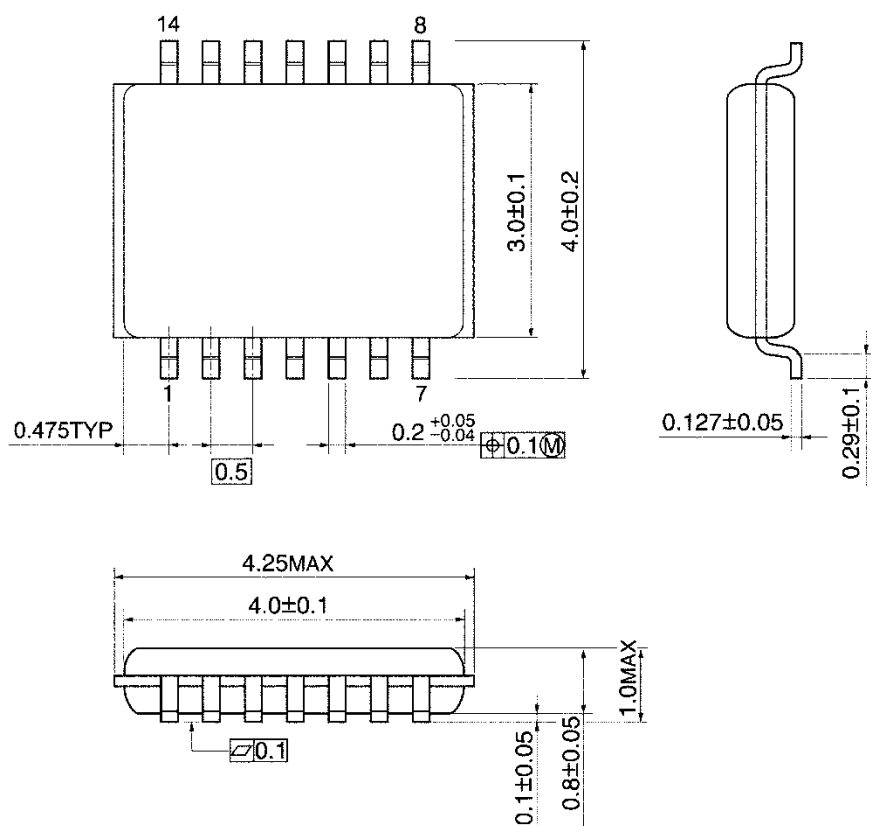


Figure 10 Input/Output Characteristics (Typ.)

Package Dimensions

VSSOP14-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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