

# TC7PCI3212MT, TC7PCI3215MT

## 1. Functional Description

- 2 Differential Channel, 2:1 multiplexer/demultiplexer switch for PCI Express Gen3

## 2. General

The TC7PCI3212MT and TC7PCI3215MT are 2 differential channel, 1-2 multiplexer/demultiplexer for PCI Express Gen3 (8Gbps), or other high-speed interface applications.

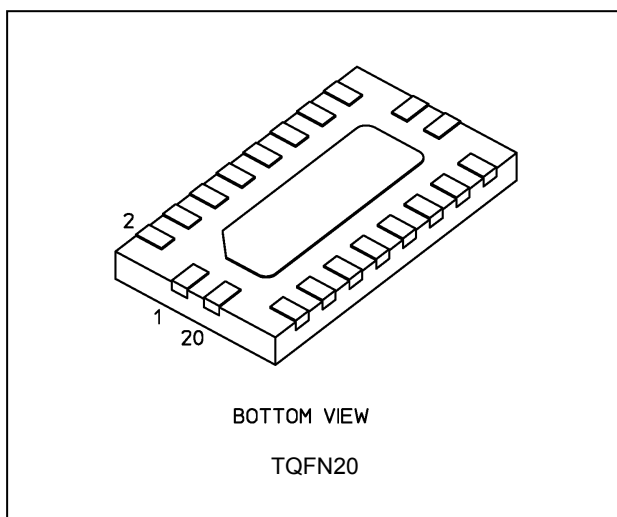
The  $A_n+/A_n-$  inputs is connected to the  $B_n+/B_n-$  or  $C_n+/C_n-$  outputs determined by the combination both the select input (SEL) and output enable ( $\overline{OE}$ ). When the output enable ( $\overline{OE}$ ) input is held high-level, the switches are open (high-impedance state) with regardless the state of select inputs and reducing consumption current.

All inputs are equipped with protection circuits against static discharge.

## 3. Features

- (1) Operating voltage:  $V_{CC} = 3.0$  to  $3.6$  V
- (2) Switch terminal ON-capacitance:  $C_{IO} = 1.5$  pF Switch On (typ.) @  $V_{CC} = 3.3$  V
- (3) ON resistance:  $R_{ON} = 7.5 \Omega$  (typ.) @  $V_{CC} = 3.0$  V,  $V_{IS} = 0$  V
- (4) -3dB Bandwidth:  $BW = 11.5$  GHz (typ.) @  $V_{CC} = 3.3$  V
- (5) Insertion Loss:  $DDIL = -1$  dB (typ.) @  $V_{CC} = 3.3$  V,  $f = 4$  GHz
- (6) Off Isolation:  $DDOIRR = -20$  dB (typ.) @  $V_{CC} = 3.3$  V,  $f = 4$  GHz
- (7) Crosstalk:  $DDNEXT = -40$  dB (typ.) @  $V_{CC} = 3.3$  V,  $f = 4$  GHz
- (8) ESD performance: Machine model  $\geq \pm 200$  V, Human body model  $\geq \pm 2000$  V
- (9) Package: TQFN20

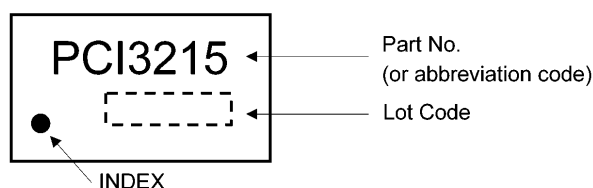
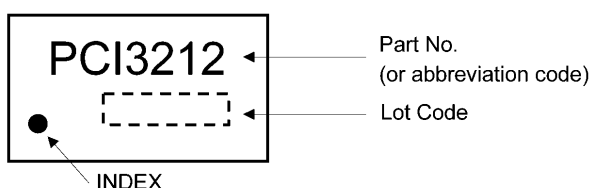
## 4. Packaging



## 5. Marking

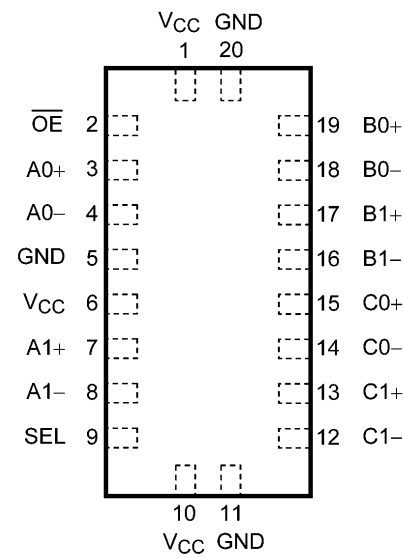
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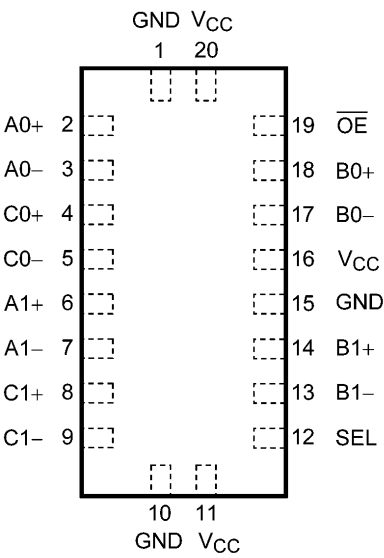


6. Pin Assignment

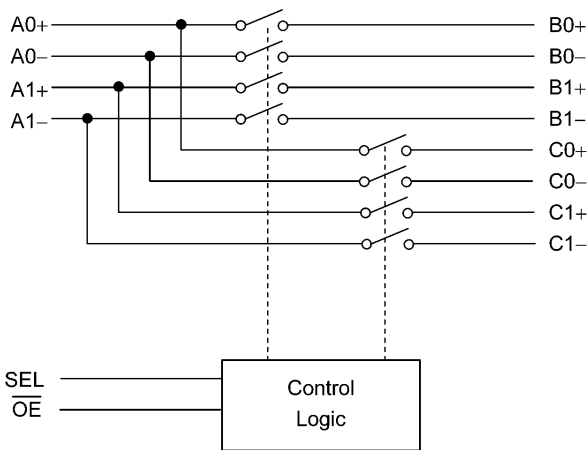
TC7PCI3212MT



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7. Block Diagram



8. Principle of Operation

8.1. Truth Table

Inputs OE	Inputs SEL	Function	Function
L	L	An+ port = Bn+ port, An- port = Bn- port	(n=0,1)
L	H	An+ port = Cn+ port, An- port = Cn- port	(n=0,1)
H	—	An, Bn, Cn port Disconnect	(n=0,1)

—: Don't care.

## 9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 4.6	V
Input voltage ( $\overline{OE}$ , SEL)	$V_{IN}$		-0.5 to 4.6	V
Switch I/O voltage	$V_S$		-0.5 to $V_{CC} + 0.5$	V
Switch I/O current	$I_S$		50	mA
Power dissipation	$P_D$		500	mW
$V_{CC}$ /ground current	$I_{CC}/I_{GND}$		$\pm 50$	mA
Storage temperature	$T_{stg}$		-55 to 125	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## 10. Operating Ranges (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		3.0 to 3.6	V
Input voltage ( $\overline{OE}$ , SEL)	$V_{IN}$		0 to 3.6	V
Switch I/O voltage	$V_S$		0 to $V_{CC}$	V
Operating temperature	$T_{opr}$		-40 to 85	°C
Input rise time	$dt/dv$		0 to 10	ns/V
Input fall time	$dt/dv$		0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused control inputs must be tied to either  $V_{CC}$  or GND.

## 11. Electrical Characteristics

### 11.1. DC Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to $85$ °C)

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit
High-level input voltage ( $\overline{OE}$ , SEL)	$V_{IH}$		—	3.0 to 3.6	$0.65 \times V_{CC}$	—	—	V
Low-level input voltage ( $\overline{OE}$ , SEL)	$V_{IL}$		—	3.0 to 3.6	—	—	$0.35 \times V_{CC}$	V
Input leakage current ( $\overline{OE}$ , SEL)	$I_{IN}$		$V_{IN} = 0$ to $3.6$ V	3.0 to 3.6	—	—	$\pm 1$	$\mu A$
Switch OFF-state leakage current	$I_{SZ}$		$V_{IS} = 0$ to $V_{CC}$ , $\overline{OE} = V_{CC}$	3.0 to 3.6	—	—	$\pm 1$	$\mu A$
ON-resistance	$R_{ON}$	(Note 1)	$V_{IS} = 0$ V, $I_{IS} = 30$ mA	3.0	—	7.5	11.5	$\Omega$
	$R_{ON}$	(Note 1)	$V_{IS} = 1.2$ V, $I_{IS} = 30$ mA	3.0	—	8.5	13.5	$\Omega$
Difference of ON-resistance between switches (bit to bit)	$\Delta R_{ON}$	(Note 1)	$V_{IS} = 0$ V, $1.2$ V, $I_{IS} = 15$ mA	3.0	—	0.1	—	$\Omega$
ON-resistance flatness	$R_{ON(Flat)}$	(Note 1)	$V_{IS} = 0$ V to $1.2$ V, $I_{IS} = 15$ mA	3.0	—	1	—	$\Omega$
Quiescent supply current	$I_{CC}$		$V_{IN} = V_{CC}$ or GND, $\overline{OE} = V_{CC}$	3.6	—	—	1	$\mu A$
Quiescent supply current	$I_{CC}$		$V_{IN} = V_{CC}$ or GND, $\overline{OE} = GND$	3.6	—	200	500	$\mu A$

Note : All typical values are at  $T_a = 25$  °C.

Note 1: ON-resistance is measured by measuring the voltage drop across the switch at the indicated current.

11.2. AC Characteristics (Note) (Unless otherwise specified,  $T_a = -40$  to  $85\text{ }^{\circ}\text{C}$ )

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit
Propagation delay time	$t_{PLH}/t_{PHL}$	(Note 1)	$C_L = 5\text{ pF}$ See Fig. 12.1	$3.3 \pm 0.3$	—	0.1	—	ns
Turn-ON time (SEL to Output)	$t_{on}$		$R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ See Fig. 12.2	$3.3 \pm 0.3$	—	10	15	ns
Turn-ON time ( $\overline{OE}$ to Output)	$t_{on}$		$R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ See Fig. 12.2	$3.3 \pm 0.3$	—	37	50	$\mu\text{s}$
Turn-OFF time (SEL to Output)	$t_{off}$		$R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ See Fig. 12.2	$3.3 \pm 0.3$	—	3.5	5	ns
Turn-OFF time ( $\overline{OE}$ to Output)	$t_{off}$		$R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ See Fig. 12.2	$3.3 \pm 0.3$	—	5	6.5	ns
Break before make	TBBM		$R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ See Fig. 12.3	$3.3 \pm 0.3$	3	—	9	ns
Output skew (bit to bit)	$t_{SK(b)}$	(Note 1)	$C_L = 5\text{ pF}$ See Fig. 12.4	$3.3 \pm 0.3$	—	5	—	ps
Output skew (channel to channel)	$t_{SK(CH)}$	(Note 1)	$C_L = 5\text{ pF}$ See Fig. 12.5	$3.3 \pm 0.3$	—	10	—	ps
Differential OFF isolation	DDOIRR	(Note 1)	$R_T = 50\text{ }\Omega$ , $f = 4\text{ GHz}$ See Fig. 12.6	$3.3 \pm 0.3$	—	-20	—	dB
Differential Near-end crosstalk	DDNEXT	(Note 1)	$R_T = 50\text{ }\Omega$ , $f = 4\text{ GHz}$ See Fig. 12.7	$3.3 \pm 0.3$	—	-40	—	dB
Differential return loss	DDRL	(Note 1)	$R_T = 50\text{ }\Omega$ , $f = 4\text{ GHz}$ See Fig. 12.8	$3.3 \pm 0.3$	—	-20	—	dB
Differential insertion loss	DDIL	(Note 1)	$R_T = 50\text{ }\Omega$ , $f = 4\text{ GHz}$ See Fig. 12.8	$3.3 \pm 0.3$	—	-1	—	dB
-3dB Bandwidth	BW	(Note 1)	$R_T = 50\text{ }\Omega$ , $C_L = 0\text{ pF}$ See Fig. 12.8	$3.3 \pm 0.3$	—	11.5	—	GHz

Note : All typical values are at  $T_a = 25\text{ }^{\circ}\text{C}$ .

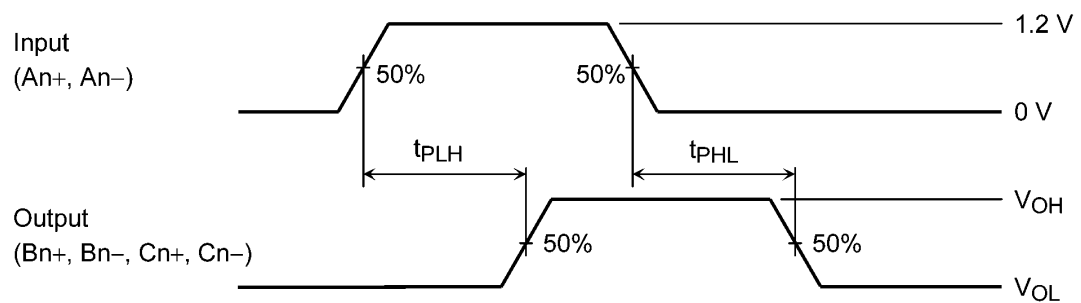
Note 1: This parameter is guaranteed by design.

11.3. Capacitive Characteristics (Note) (Unless otherwise specified,  $T_a = 25\text{ }^{\circ}\text{C}$ )

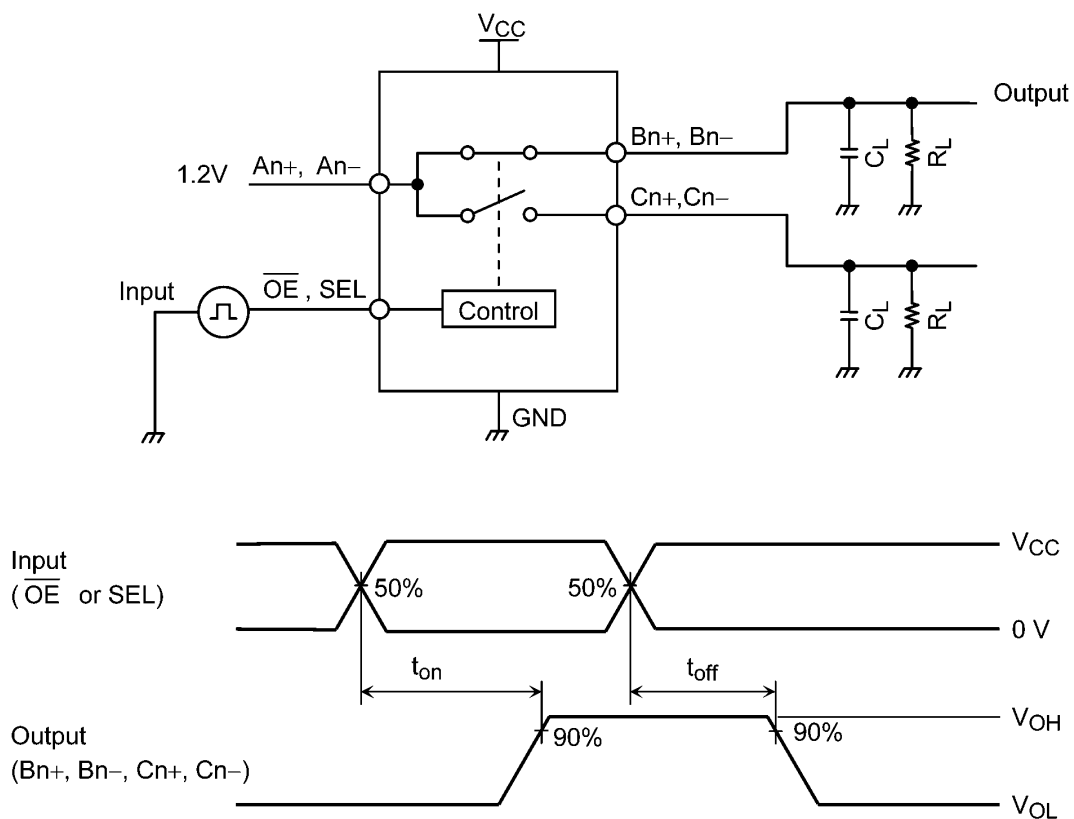
Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	Typ.	Unit
Input capacitance ( $\overline{OE}$ , SEL)	$C_{IN}$		$V_{IN} = 0\text{ V}$	3.3	3	pF
Switch terminal OFF-capacitance ( $An+$ , $An-$ )	$C_{I/O}$		$\overline{OE} = V_{CC}$ , $V_{IS} = 0\text{ V}$	3.3	0.8	pF
Switch terminal OFF-capacitance ( $Bn+$ , $Bn-$ , $Cn+$ , $Cn-$ )			$\overline{OE} = V_{CC}$ , $V_{IS} = 0\text{ V}$	3.3	0.5	pF
Switch terminal ON-capacitance	$C_{I/O}$		$\overline{OE} = \text{GND}$ , $V_{IS} = 0\text{ V}$	3.3	1.5	pF

Note: Parameter guaranteed by design.

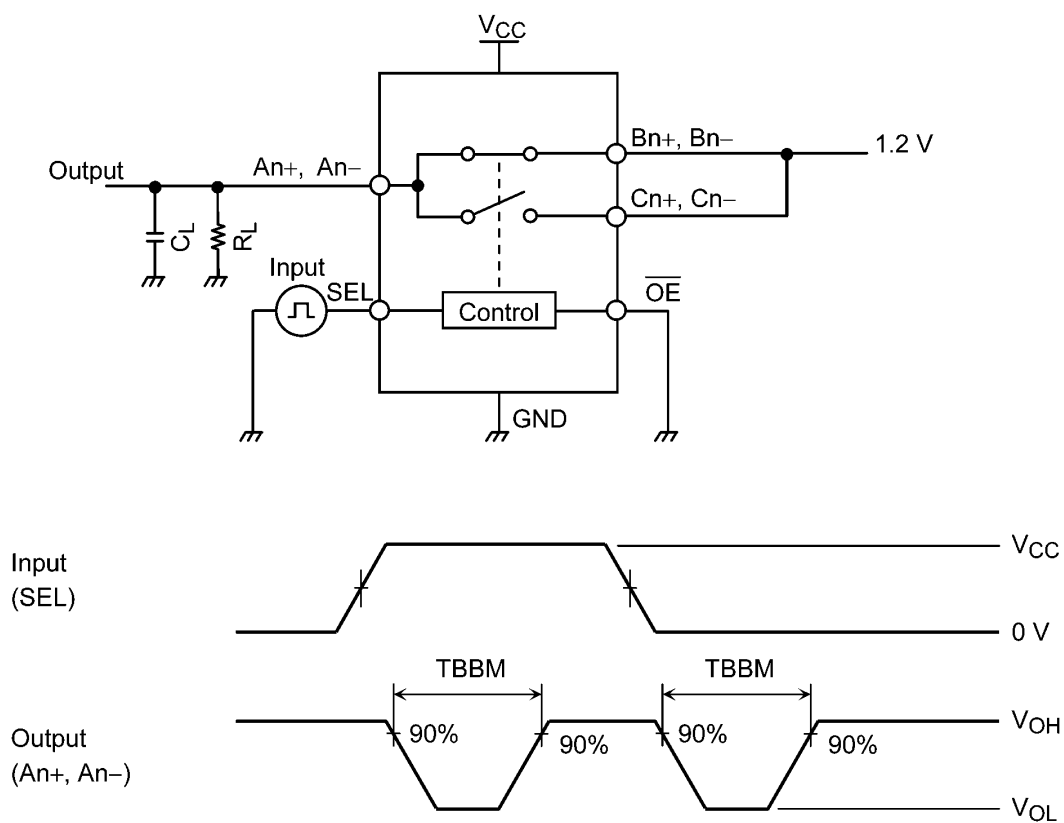
The diagram shows a 1-bit digital multiplexer. It has an **Input** terminal connected to a square-wave signal source. The input signal is connected to the **An+, An-** inputs of a 2-to-1 multiplexer core. The **SEL** (select) input is connected to the **H or L** control input of the same core. The output of the multiplexer core is connected to the **Bn+, Bn-** and **Cn+, Cn-** terminals. A **Control** block is connected to the **OE** (output enable) input of the multiplexer core. The output of the multiplexer core is connected to the **Output** terminal, which is also connected to a load capacitor  $C_L$ . The circuit is powered by  $V_{CC}$  and  $GND$ .



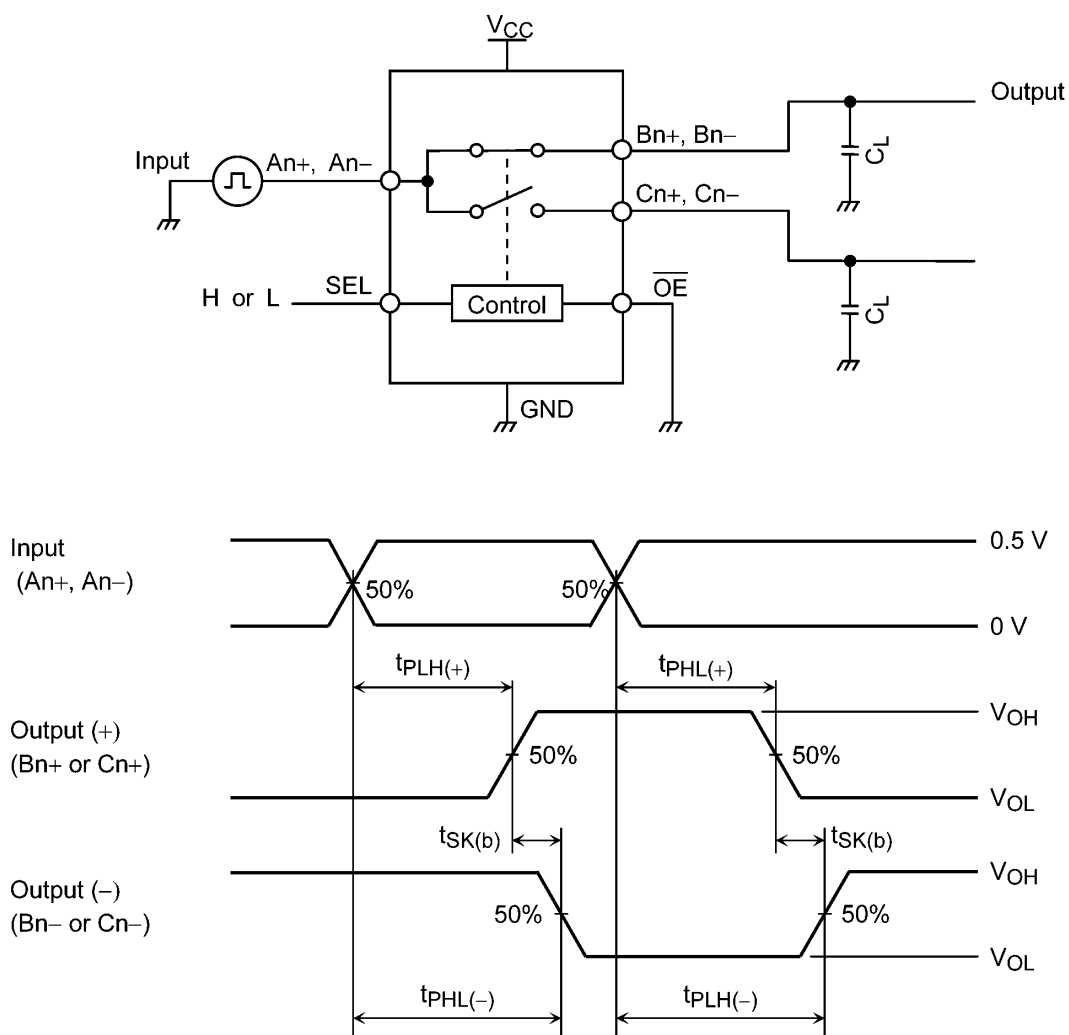
**Fig. 12.1 Propagation delay time**



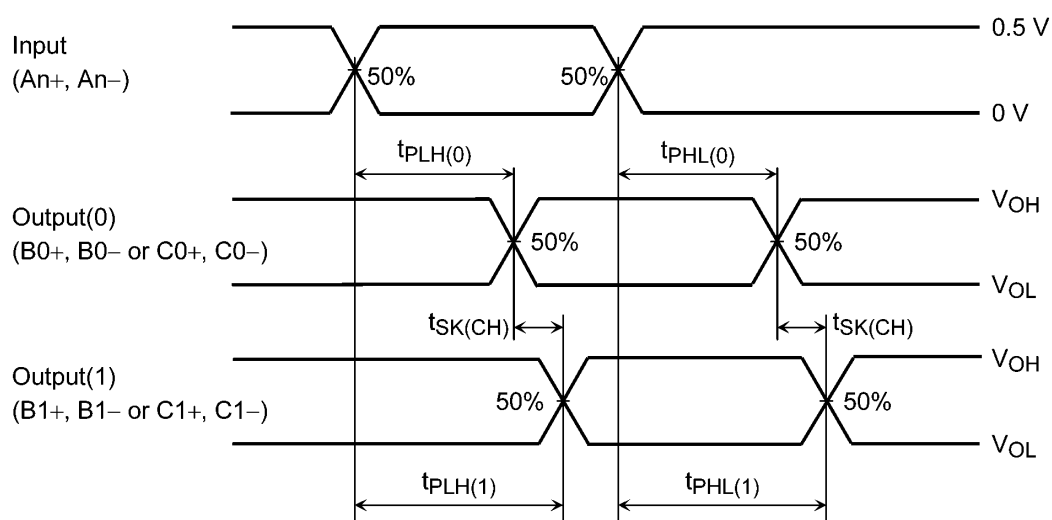
**Fig. 12.2 Turn-ON and Turn-OFF time**



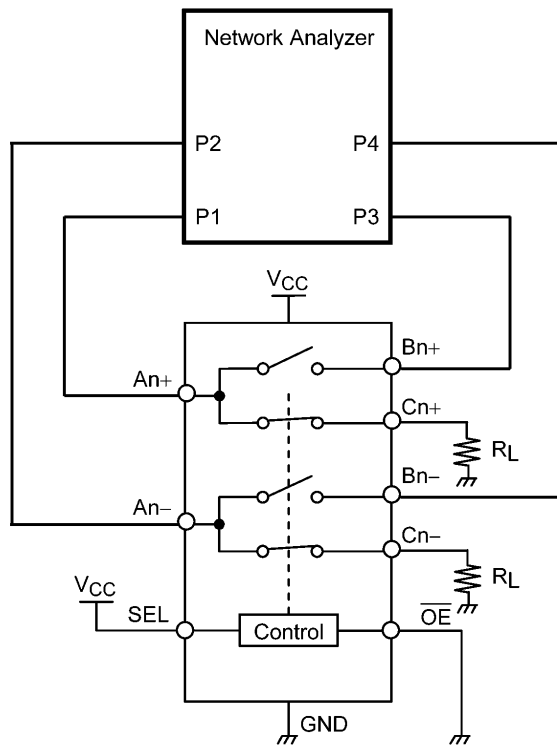
**Fig. 12.3 Break before make**



**Fig. 12.4 Output skew (bit to bit)**

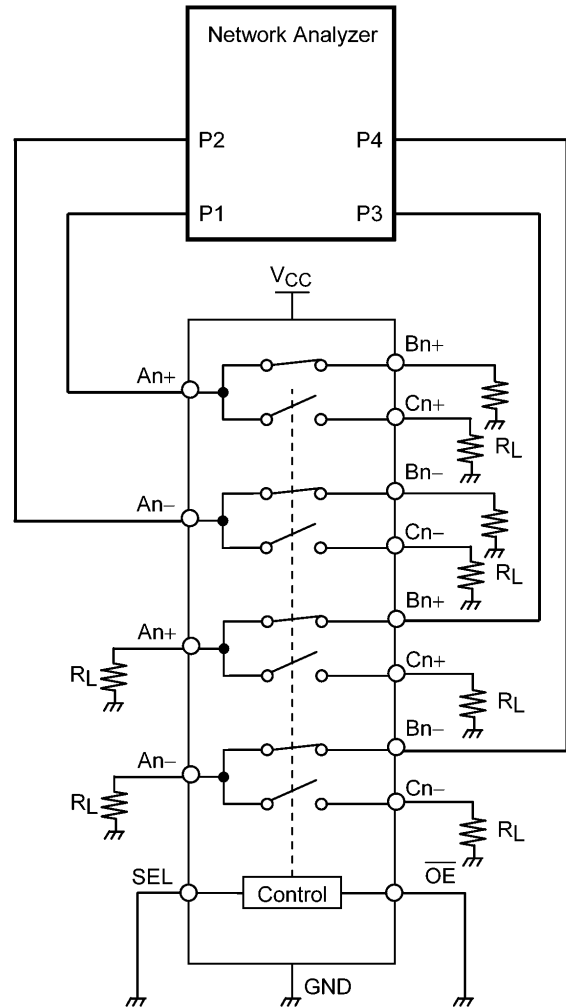


**Fig. 12.5 Output skew (channel to channel)**



$R_L = 50\ \Omega$   
All unused ports are connected to GND through  $50\ \Omega$  pull-down resistors.

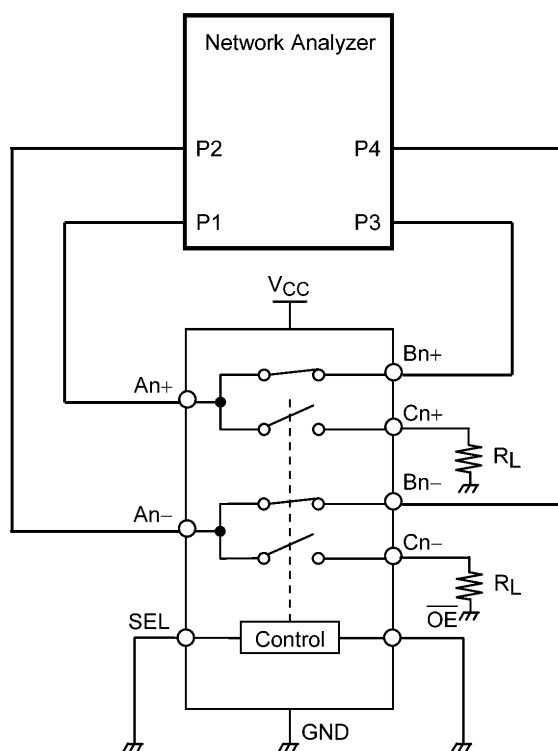
**Fig. 12.6 Differential OFF isolation**



$R_L = 50\ \Omega$   
All unused ports are connected to GND through  $50\ \Omega$  pull-down resistors.

**Fig. 12.7 Differential Near-end crosstalk**





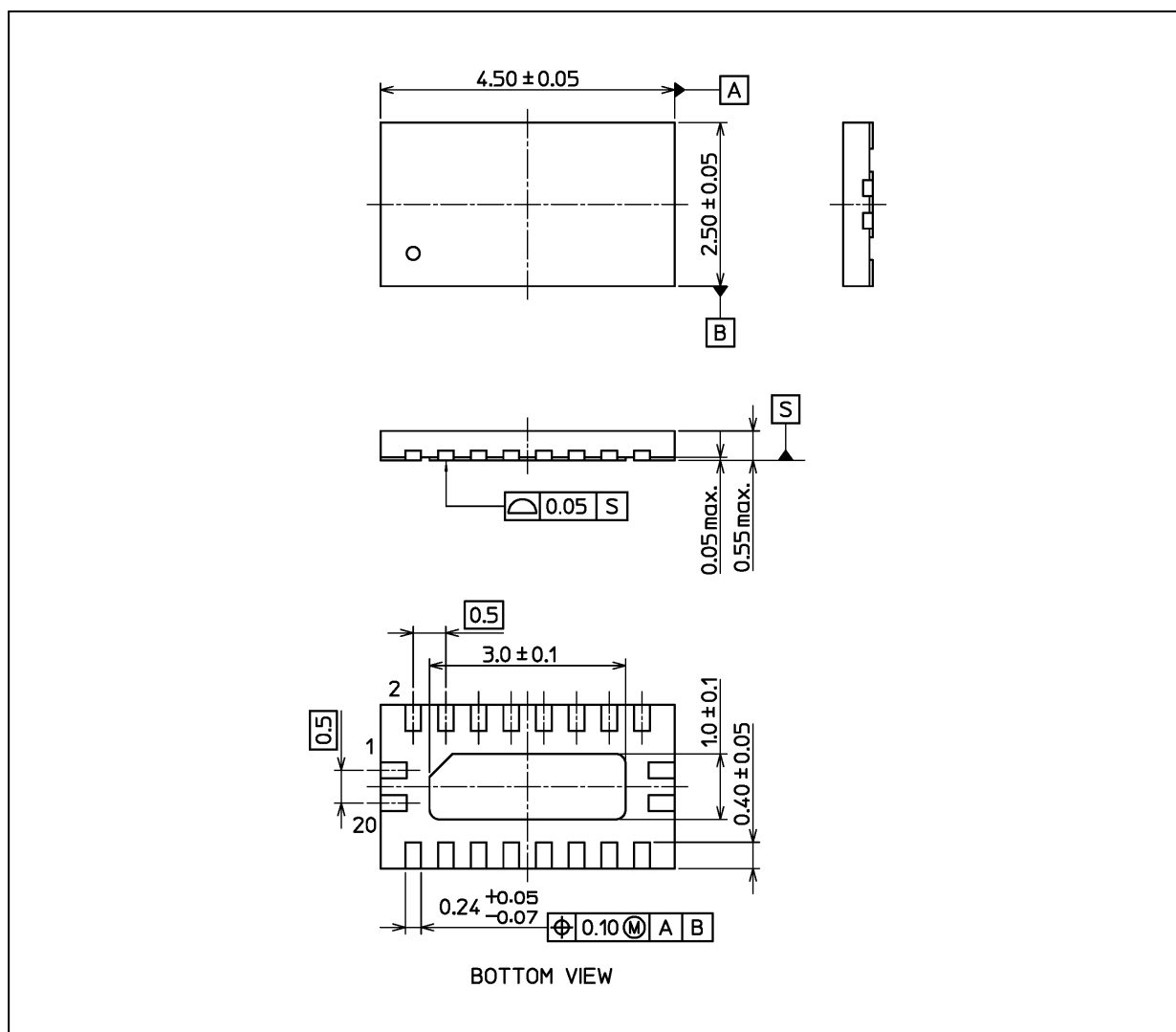
$R_L = 50\ \Omega$

All unused ports are connected to GND through  $50\ \Omega$  pull-down resistors.

**Fig. 12.8 Differential return loss, Differential insertion loss, -3dB Bandwidth**

## Package Dimensions

Unit: mm



Weight: 0.017 g (typ.)

Package Name(s)
TOSHIBA: P-UQFN20-0305-0.50-001
Nickname: TQFN20

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