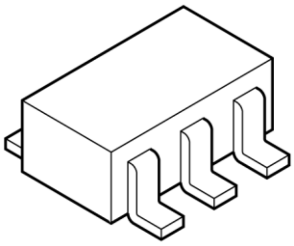
TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TC75S55F, TC75S55FU

Single Operational Amplifier

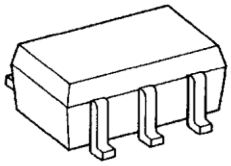
The TC75S55F/TC75S55FU is a CMOS single-operation amplifier which incorporates a phase compensation circuit. It is designed for use with a low-voltage, low-current power supply; this differentiates this device from conventional general-purpose bipolar op-amps.

TC75S55F



SSOP5-P-0.95 (SMV)

TC75S55FU



SSOP5-P-0.65A (USV)

Weight
SSOP5-P-0.95 : 0.014 g (typ.)
SSOP5-P-0.65A : 0.006 g (typ.)

Features

- Low-voltage operation : V_{DD} = ±0.9 to 3.5 V or 1.8 to 7 V
- Low-current power supply : I_{DD} (V_{DD} = 3 V) = 10 μA (typ.)
- Built-in phase-compensated op-amp, obviating the need for any external device
- Ultra-compact package

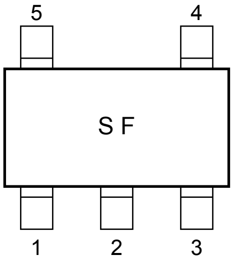
Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}, V_{SS}	7	V
Differential input voltage	DV_{IN}	±7	V
Input voltage	V_{IN}	V_{DD} to V_{SS}	V
Power dissipation	P_D	200	mW
Operating temperature	T_{opr}	−40 to 85	°C
Storage temperature	T_{stg}	−55 to 125	°C

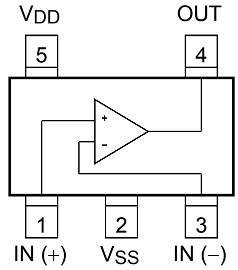
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production
1995-01

Marking (top view)



Pin Connection (top view)



Electrical Characteristics

DC Characteristics (V_{DD} = 3.0 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	R_S = 10 kΩ	—	2	10	mV
Input offset current	I_{IO}	—	—	—	1	—	pA
Input bias current	I_I	—	—	—	1	—	pA
Common mode input voltage	CMV_{IN}	2	—	0.0	—	2.1	V
Voltage gain (open loop)	G_V	—	—	60	70	—	dB
Maximum output voltage	V_{OH}	3	R_L ≥ 1 MΩ	2.9	—	—	V
	V_{OL}	4	R_L ≥ 1 MΩ	—	—	0.1	
Common mode input signal Rejection Ratio	CMRR	2	V_{IN} = 0.0 to 2.1 V	60	70	—	dB
Supply voltage rejection ratio	SVRR	1	V_{DD} = 1.8 to 7.0 V	60	70	—	dB
Supply current	I_{DD}	5	—	—	10	20	μA
Source current	I_{source}	6	—	10	20	—	μA
Sink current	I_{sink}	7	—	100	450	—	μA

DC Characteristics (V_{DD} = 1.8 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	R_S = 100 kΩ	—	2	10	mV
Input offset current	I_{IO}	—	—	—	1	—	pA
Input bias current	I_I	—	—	—	1	—	pA
Common mode input voltage	CMV_{IN}	2	—	0.0	—	0.9	V
Voltage gain (open loop)	G_V	—	—	60	70	—	dB
Maximum output voltage	V_{OH}	3	R_L ≥ 1 MΩ	1.7	—	—	V
	V_{OL}	4	R_L ≥ 1 MΩ	—	—	0.1	
Supply current	I_{DD}	5	—	—	8	16	μA
Source current	I_{source}	6	—	8	16	—	μA
Sink current	I_{sink}	7	—	100	400	—	μA

AC Characteristics (V_{DD} = 3.0 V, V_{SS} = GND, Ta = 25°C)

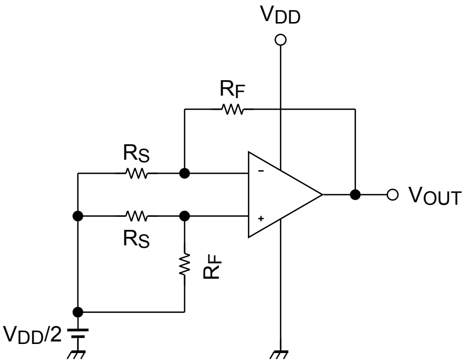
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	—	—	0.08	—	V/μs
Unity gain cross frequency	f_T	—	—	—	160	—	kHz

AC Characteristics (V_{DD} = 1.8 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	—	—	0.06	—	V/μs
Unity gain cross frequency	f_T	—	—	—	140	—	kHz

Test Circuit

1. SVRR, V_{IO}



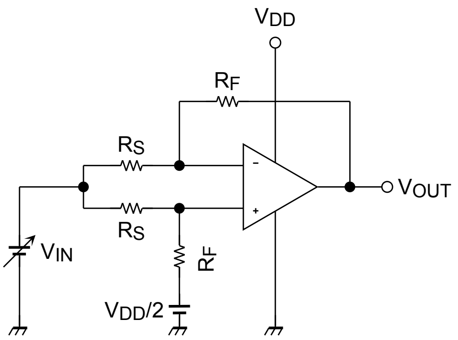
- SVRR
  For each of the two V_{DD} values, measure the V_{OUT} value, as indicated below, and calculate the value of SVRR using the equation shown.
  When V_{DD} = 1.8 V, V_{DD} = $V_{DD}1$ and V_{OUT} = $V_{OUT}1$
  When V_{DD} = 7.0 V, V_{DD} = $V_{DD}2$ and V_{OUT} = $V_{OUT}2$

$$SVRR = 20\log\left(\left|\frac{V_{OUT}1 - V_{OUT}2}{V_{DD}1 - V_{DD}2}\right| \times \frac{R_S}{R_F + R_S}\right)$$

- V_{IO}
  Measure the value of V_{OUT} and calculate the value of V_{IO} using the following equation.

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

2. CMRR, CMV_{IN}

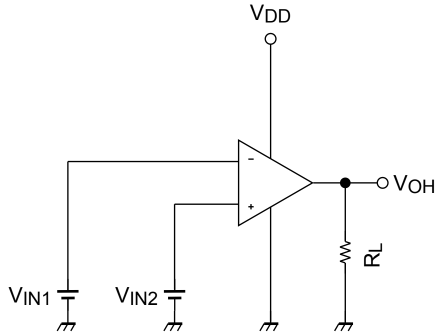


- CMRR
  Measure the V_{OUT} value, as indicated below, and calculate the value of the CMRR using the equation shown.
  When V_{IN} = 0.0 V, V_{IN} = $V_{IN}1$ and V_{OUT} = $V_{OUT}1$
  When V_{IN} = 2.1 V, V_{IN} = $V_{IN}2$ and V_{OUT} = $V_{OUT}2$

$$CMRR = 20\log\left(\left|\frac{V_{OUT}1 - V_{OUT}2}{V_{IN}1 - V_{IN}2}\right| \times \frac{R_S}{R_F + R_S}\right)$$

- CMV_{IN}
  Input range within which the CMRR specification guarantees V_{OUT} value (as varied by the V_{IN} value).

3. V_{OH}

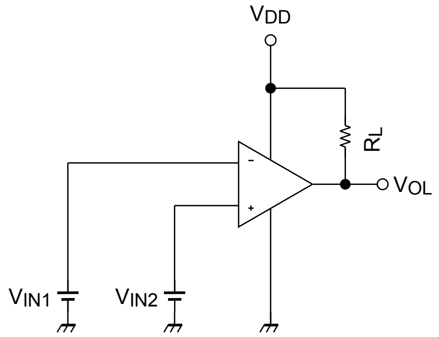


- V_{OH}

$$V_{IN1} = \frac{V_{DD}}{2} - 0.05\ \text{V}$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.05\ \text{V}$$

4. V_{OL}

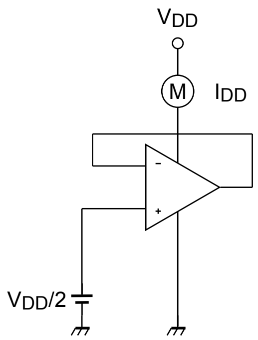


- V_{OL}

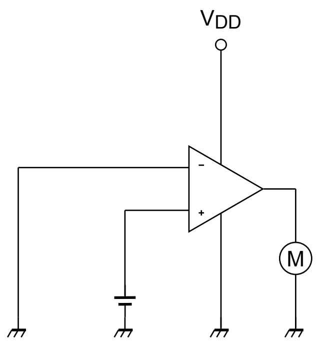
$$V_{IN1} = \frac{V_{DD}}{2} + 0.05\ \text{V}$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.05\ \text{V}$$

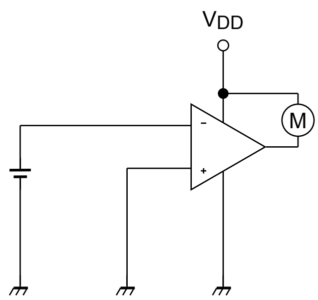
5. I_{DD}



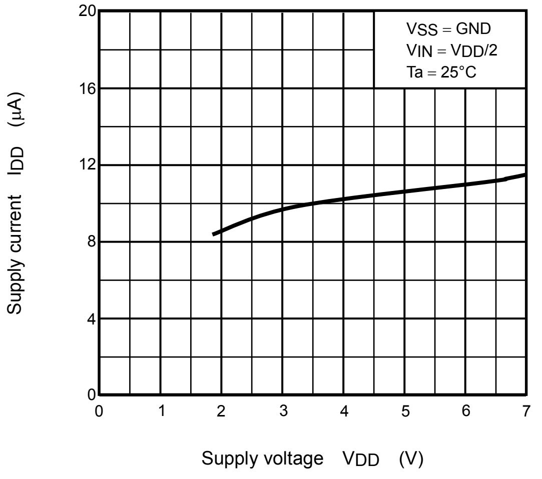
6. I_{source}



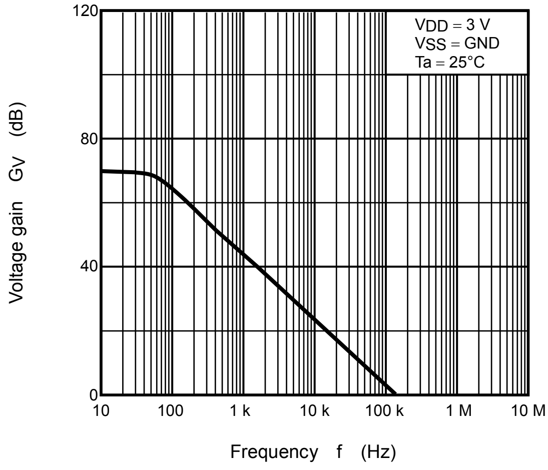
7. I_{sink}



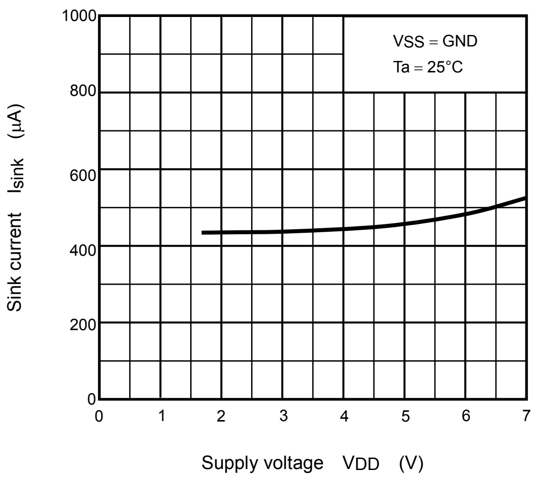
$I_{DD} - V_{DD}$



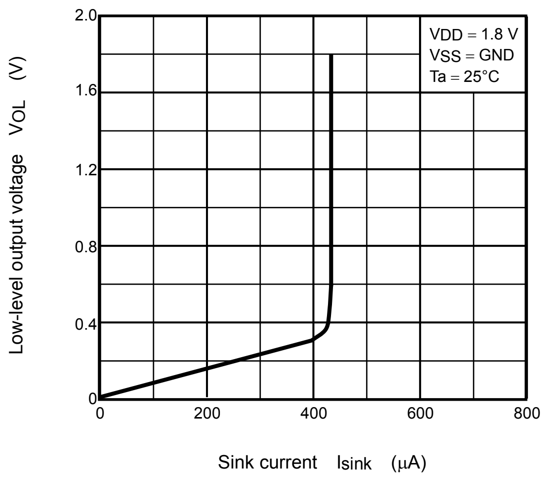
$G_V - f$



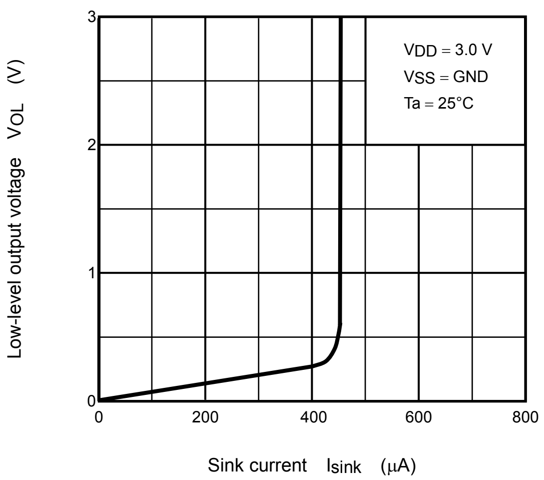
$I_{sink} - V_{DD}$



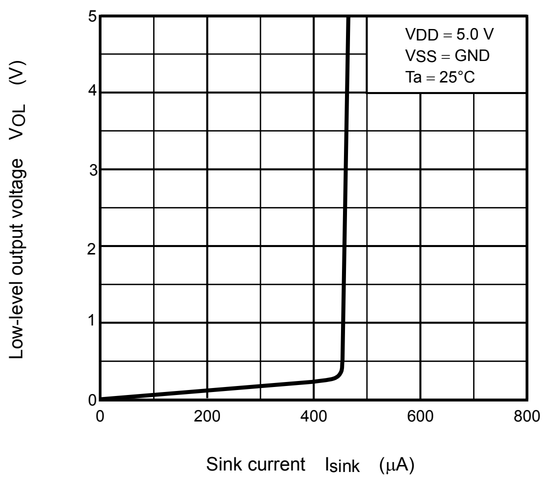
$V_{OL} - I_{sink}$



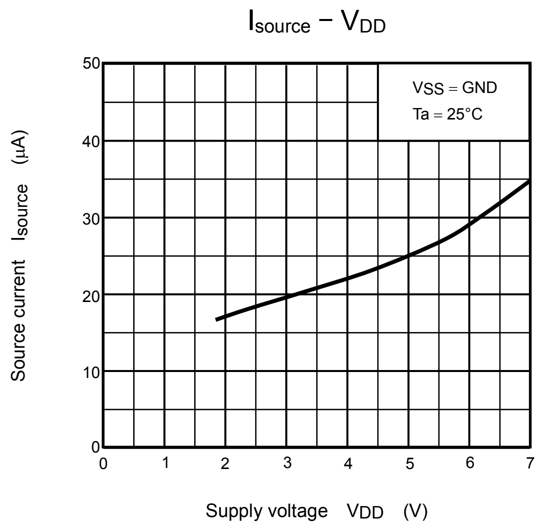
$V_{OL} - I_{sink}$

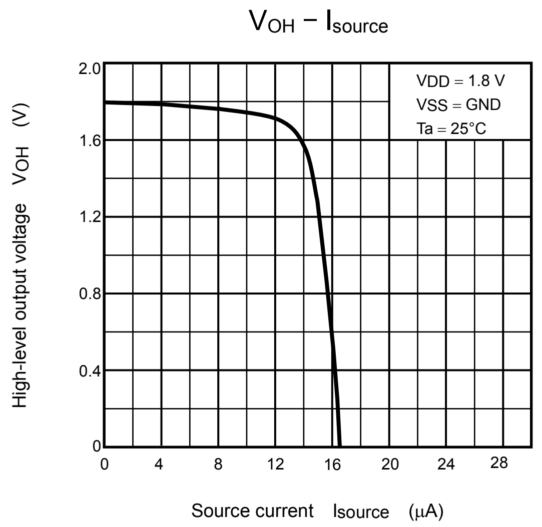


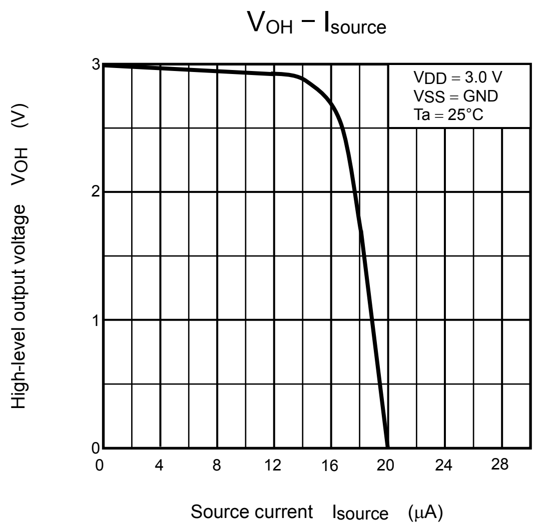
$V_{OL} - I_{sink}$

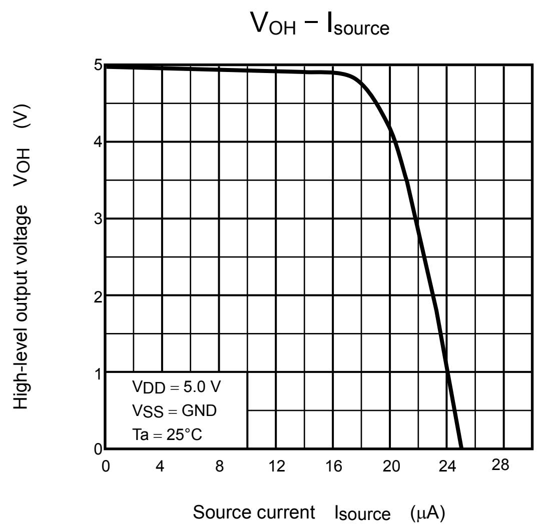


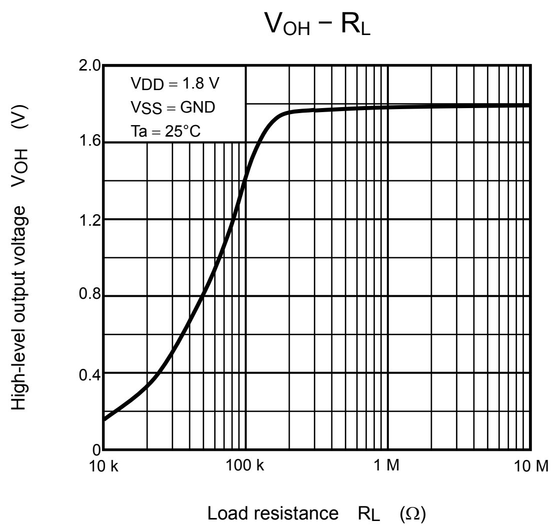
The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

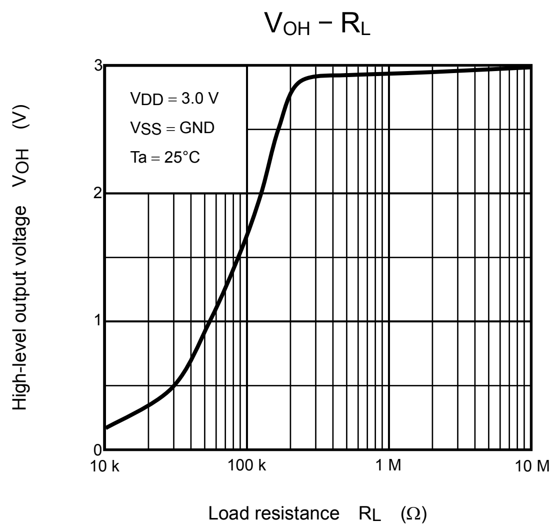












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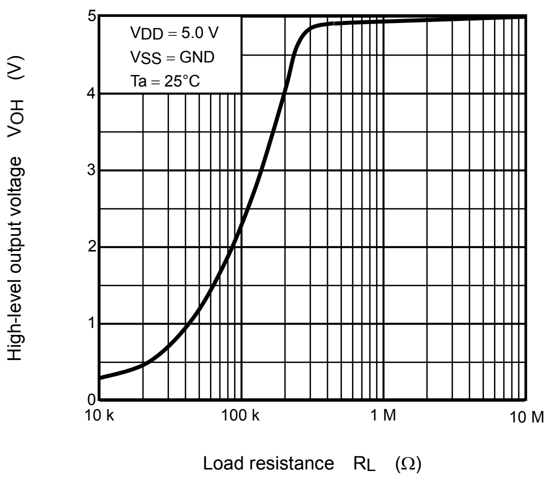
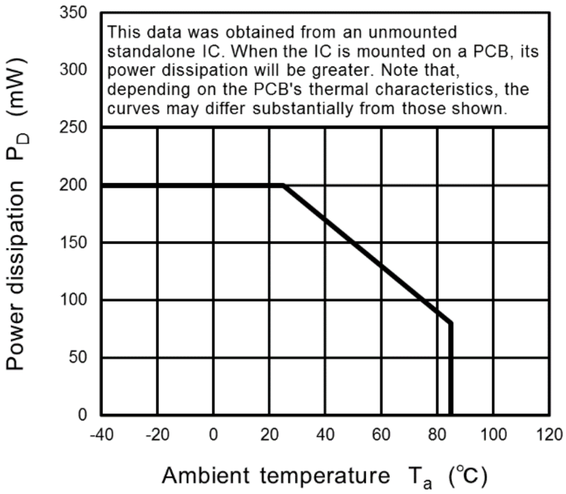
V_{OH} – R_L



P_D – Ta

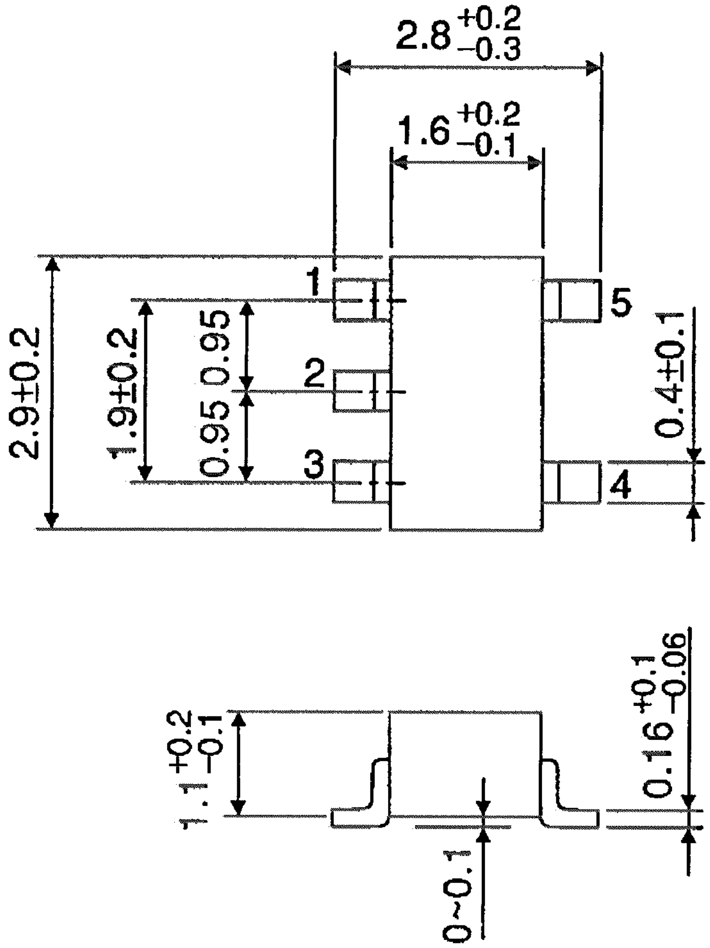


The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

SSOP5-P-0.95

Unit : mm

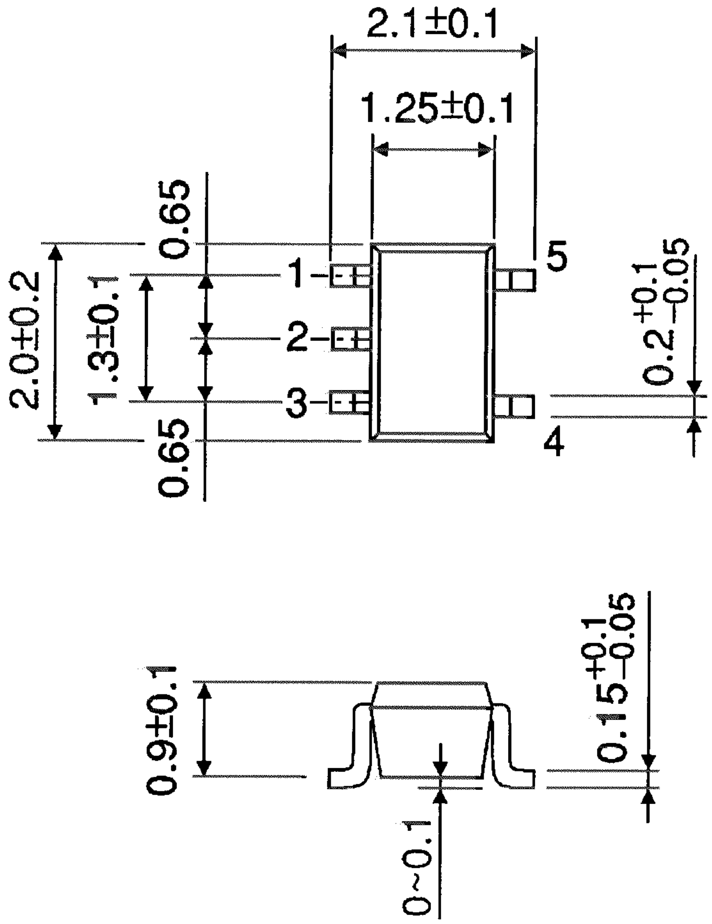


Weight: 0.014 g (typ.)

Package Dimensions

SSOP5-P-0.65A

Unit : mm



Weight: 0.006 g (typ.)

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