TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC7292AP, TC74HC7292AF

Programmable Divider/Timer

The TC74HC7292A is a high speed CMOS PROGRAMMABLE DIVIDER/TIMER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC7292A can divide from 2^2 to 2^{31}.

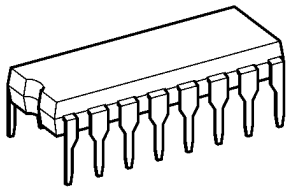
CK1 and CK2 are clock inputs, either one may be used for clock gating.

It features an active-low clear input to initialize the state of all flip-flops.

To facilitate incoming inspection, test points are provided. (TP1, TP2 and TP3)

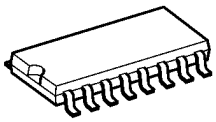
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74HC7292AP



DIP16-P-300-2.54A

TC74HC7292AF



SOP16-P-300-1.27A

Weight

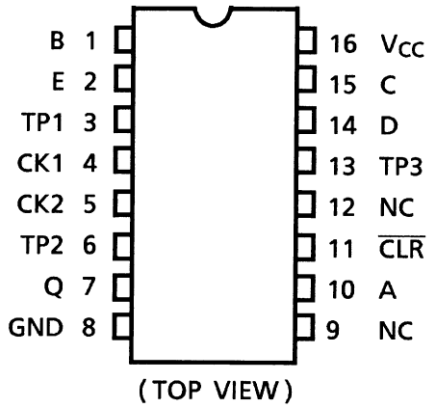
DIP16-P-300-2.54A : 1.00 g (typ.)

SOP16-P-300-1.27A : 0.18 g (typ.)

Features

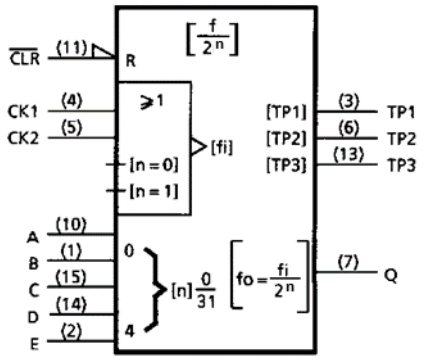
- High speed: f_{max} = 70 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with 74LS292

Pin Assignment



Start of commercial production
1988-11

IEC Logic Symbol

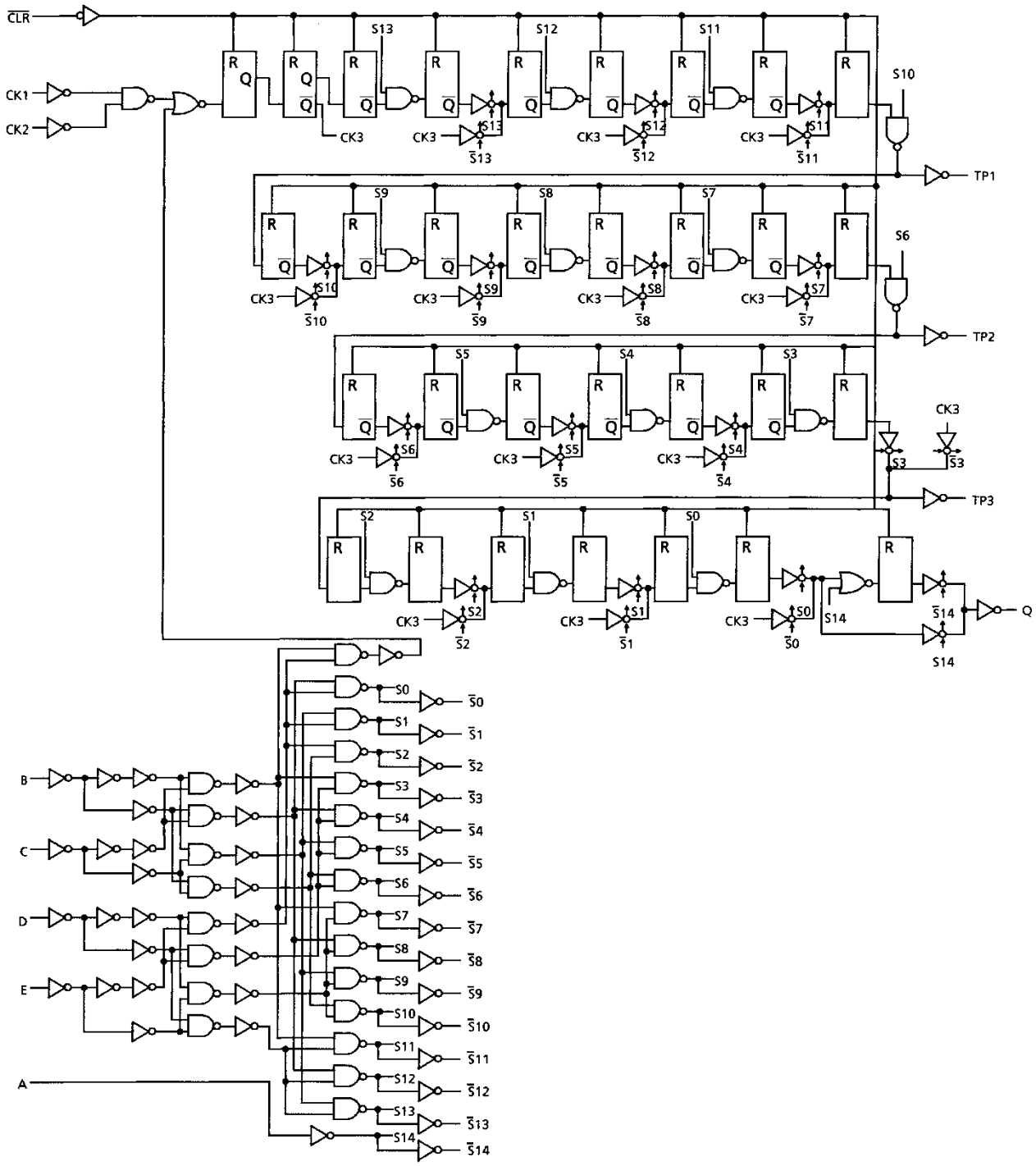


Truth Table

$\overline{CLR}$	CK1	CK2	Q Output Mode
L	X	X	Cleared to L
H	↑	L	Up Count
H	L	↑	
H	H	X	No Change
H	X	H	

Programming Inputs					Frequency Division							
					Q		TP1		TP2		TP3	
E	D	C	B	A	Binary	Decimal	Binary	Decimal	Binary	Decimal	Binary	Decimal
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2^{2}	4	2^{9}	512	2^{17}	131,072	2^{24}	16,777,216
L	L	L	H	H	2^{3}	8	2^{9}	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	L	2^{4}	16	2^{9}	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	H	2^{5}	32	2^{9}	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	L	2^{6}	64	2^{9}	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	H	2^{7}	128	2^{9}	512	2^{17}	131,072	2^{24}	16,777,216
L	H	L	L	L	2^{8}	256	2^{9}	512	2^{17}	131,072	2^{2}	4
L	H	L	L	H	2^{9}	512	2^{9}	512	2^{17}	131,072	2^{2}	4
L	H	L	H	L	2^{10}	1,024	2^{9}	512	2^{17}	131,072	2^{4}	16
L	H	L	H	H	2^{11}	2,048	2^{9}	512	2^{17}	131,072	2^{4}	16
L	H	H	L	L	2^{12}	4,096	2^{9}	512	2^{17}	131,072	2^{6}	64
L	H	H	L	H	2^{13}	8,192	2^{9}	512	2^{17}	131,072	2^{6}	64
L	H	H	H	L	2^{14}	16,384	2^{9}	512	Disabled Low		2^{8}	256
L	H	H	H	H	2^{15}	32,768	2^{9}	512	Disabled Low		2^{8}	256
H	L	L	L	L	2^{16}	65,536	2^{9}	512	2^{3}	8	2^{10}	1,024
H	L	L	L	H	2^{17}	131,072	2^{9}	512	2^{3}	8	2^{10}	1,024
H	L	L	H	L	2^{18}	262,144	2^{9}	512	2^{5}	32	2^{12}	4,096
H	L	L	H	H	2^{19}	524,288	2^{9}	512	2^{5}	32	2^{12}	4,096
H	L	H	L	L	2^{20}	1,048,576	2^{9}	512	2^{7}	128	2^{14}	16,384
H	L	H	L	H	2^{21}	2,097,152	2^{9}	512	2^{7}	128	2^{14}	16,384
H	L	H	H	L	2^{22}	4,194,304	Disabled Low		2^{9}	512	2^{16}	65,536
H	L	H	H	H	2^{23}	8,388,608	Disabled Low		2^{9}	512	2^{16}	65,536
H	H	L	L	L	2^{24}	16,777,216	2^{3}	8	2^{11}	2,048	2^{18}	262,144
H	H	L	L	H	2^{25}	33,554,432	2^{3}	8	2^{11}	2,048	2^{18}	262,144
H	H	L	H	L	2^{26}	67,108,864	2^{5}	32	2^{13}	8,192	2^{20}	1,048,576
H	H	L	H	H	2^{27}	134,217,728	2^{5}	32	2^{13}	8,192	2^{20}	1,048,576
H	H	H	L	L	2^{28}	268,435,456	2^{7}	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	L	H	2^{29}	536,870,912	2^{7}	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	H	L	2^{30}	1,073,741,824	2^{9}	512	2^{17}	131,072	2^{24}	16,777,216
H	H	H	H	H	2^{31}	2,147,483,648	2^{9}	512	2^{17}	131,072	2^{24}	16,777,216

System Diagram



Absolute Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7	V
DC input voltage	V_{IN}	-0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	-0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	500 (DIP) (Note 1)/180 (SOP)	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 500 mW in the range of Ta = -40 to 65°C. From Ta = 65 to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

Operating Ranges

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V) 0 to 500 (V_{CC} = 4.5 V) 0 to 400 (V_{CC} = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = -40 to 85°C Min	Ta = -40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage (Q)	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I_{OH} = -4 mA	4.5	4.18	4.31	—	4.13	—	
			I_{OH} = -5.2 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage (Q)	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Typ.	Ta = 25°C Limit	Ta = -40 to 85°C Limit	Unit
Minimum pulse width (CK)	$t_{W\ (L)}$ $t_{W\ (H)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($\overline{CLR}$)	$t_{W\ (L)}$	—	2.0	—	175	220	ns
			4.5	—	35	44	
			6.0	—	30	37	
Minimum removal time	t_{rem}	—	2.0	—	5	5	ns
			4.5	—	5	5	
			6.0	—	5	5	
Clock frequency	f	—	2.0	—	5	4	MHz
			4.5	—	27	22	
			6.0	—	32	26	

AC Characteristics (C_L = 15 pF, V_{CC} = 5 V, Ta = 25°C, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time (Q)	t_{TLH} t_{THL}	—	—	4	8	ns
Output transition time (TP)	t_{TLH} t_{THL}	—	—	25	44	ns
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	—	—	42	75	ns
Propagation delay time ($\overline{CLR}$ -Q)	t_{pHL}	—	—	36	62	ns
Maximum clock frequency	f_{max}	—	30	70	—	MHz

AC Characteristics (C_L = 50 pF, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = -40 to 85°C Min	Ta = -40 to 85°C Max	Unit
Output transition time (Q)	t_{TLH} t_{THL}	—	2.0	—	27	75	—	95	ns
			4.5	—	9	15	—	19	
			6.0	—	8	13	—	16	
Output transition time (TP)	t_{TLH} t_{THL}	—	2.0	—	90	250	—	315	ns
			4.5	—	30	50	—	63	
			6.0	—	25	43	—	54	
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	—	2.0	—	150	425	—	530	ns
			4.5	—	48	85	—	106	
			6.0	—	41	72	—	90	
Propagation delay time ($\overline{CLR}$ -Q)	t_{pHL}	—	2.0	—	130	350	—	440	ns
			4.5	—	42	70	—	88	
			6.0	—	36	60	—	75	
Maximum clock frequency	f_{max}	—	2.0	5	20	—	4	—	MHz
			4.5	27	64	—	22	—	
			6.0	32	75	—	26	—	
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD}	(Note)		—	22	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

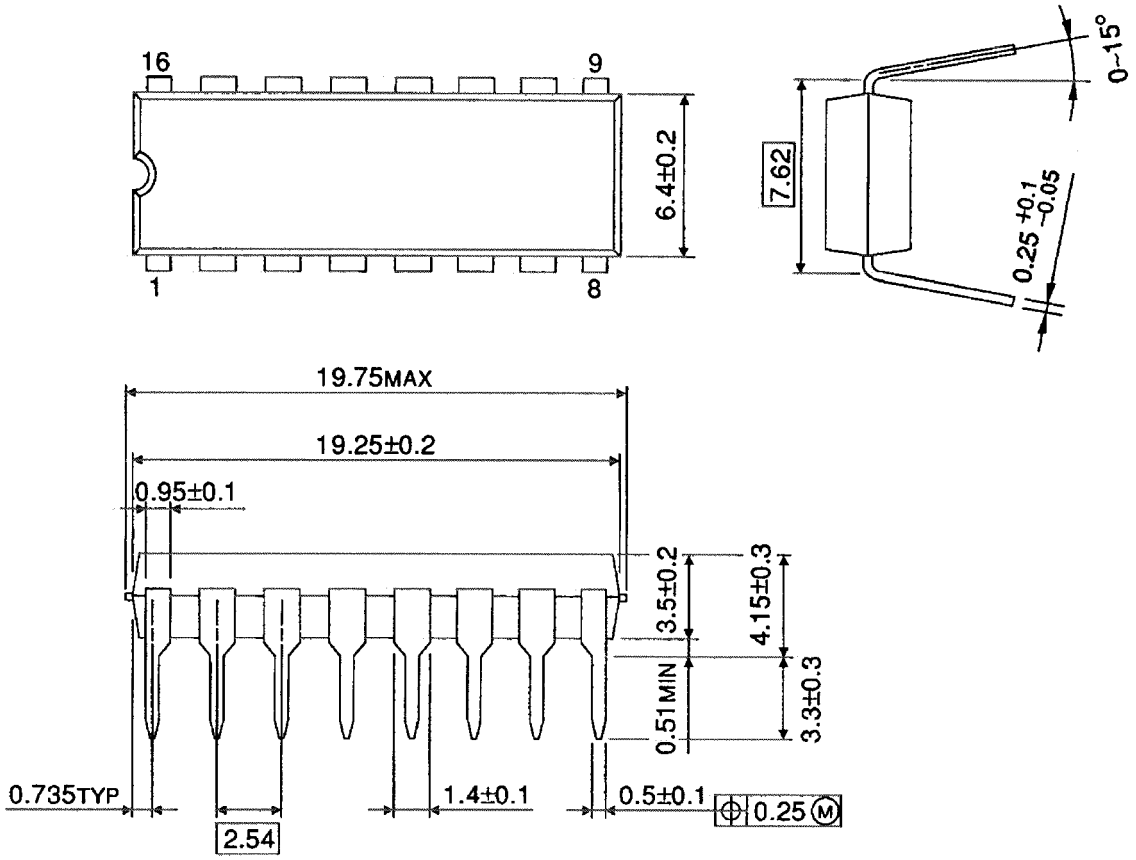
Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

DIP16-P-300-2.54A

Unit : mm

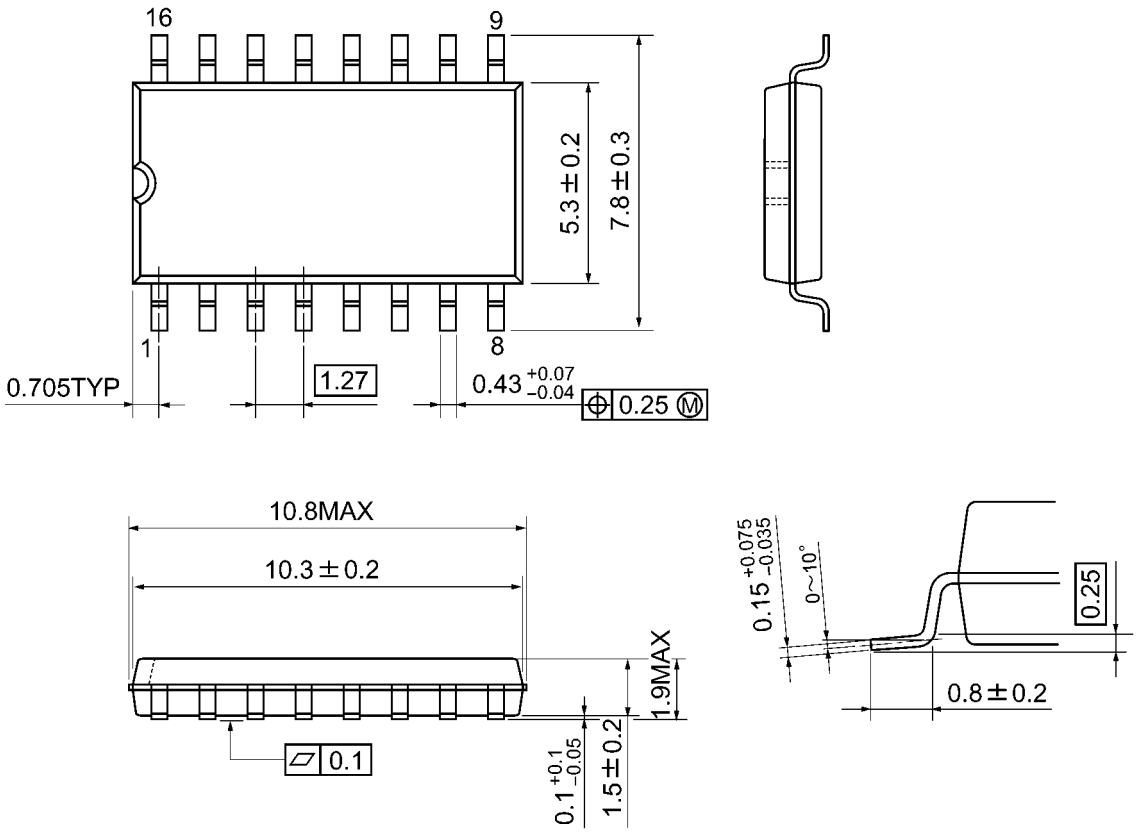


Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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