CMOS Digital Integrated Circuits Silicon Monolithic

TC74HC4049AP,TC74HC4050AP

1. Functional Description

・ Hex Buffer

TC74HC4049AP: HEX BUFFER/CONVERTER (INVERTING)
TC74HC4050AP: HEX BUFFER/CONVERTER

2. General

The TC74HC4049AP and TC74HC4050AP are high speed CMOS HEX BUFFERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC4049AP is an inverting buffer, while the TC74HC4050AP is a non-inverting buffer. The internal circuits are composed of 3-stages (TC74HC4049AP) or 2-stages (TC74HC4050AP) of inverter, which provided high noise immunity and stable output.

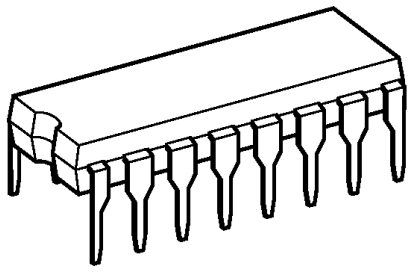
Input protection circuits are different from those of other high speed CMOS IC's. They eliminate the diodes on the V_{CC} side thus providing of logic-level conversion from high-level voltages up to 15 V to low-level voltages.

They are useful for battery back up circuits, because input voltage can be applied on IC's which are not biased by V_{CC}.

3. Features

(1) High speed: t_{pd} = 9 ns (typ.) at V_{CC} = 5.0 V
(2) Low power dissipation: I_{CC} = 1.0 μA (max) at T_a = 25 °C
(3) High noise immunity: $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (min)
(4) Symmetrical Output impedance: $|I_{OH}| = I_{OL}$ = 6 mA (min)
(5) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
(6) Wide operating voltage range: $V_{CC(opr)}$ = 2.0 V to 6.0 V
(7) Power-down protection is provided on all inputs.

4. Packaging

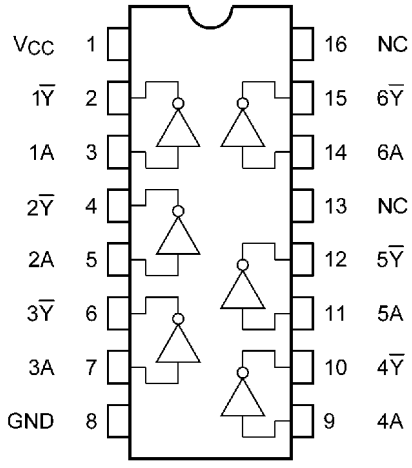


DIP16

Start of commercial production
1986-05

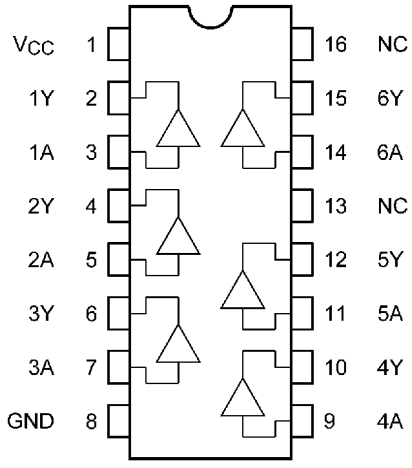
5. Pin Assignment

TC74HC4049AP



(top view)

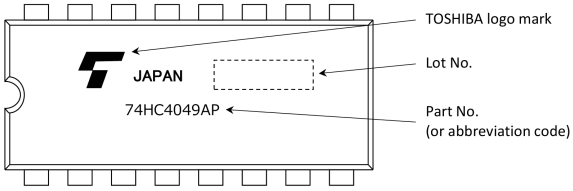
TC74HC4050AP



(top view)

6. Marking

TC74HC4049AP



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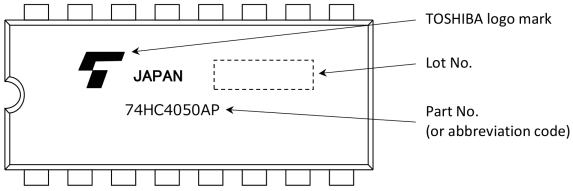
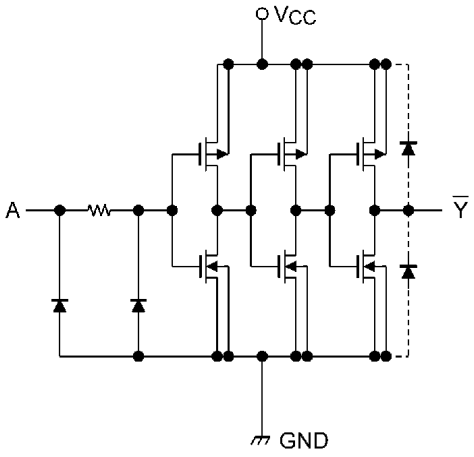


7. IEC Logic Symbol

TC74HC4049AP



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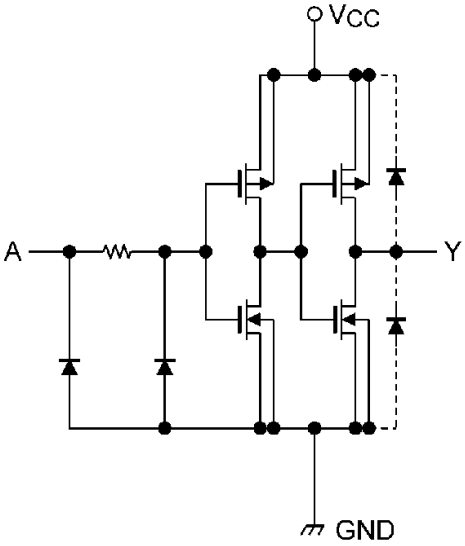
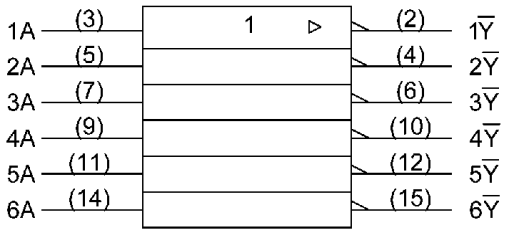


8. Truth Table

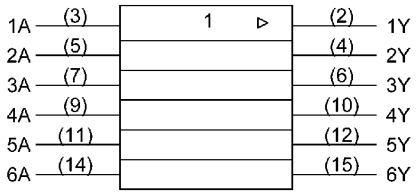
Input A	Output $\overline{Y}$ (TC74HC4049AP)	Output Y (TC74HC4050AP)
L	H	L
H	L	H

9. Internal Equivalent Circuit

TC74HC4049AP



TC74HC4050AP



10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}	(Note 1)	-0.5 to 18.0	V
Output voltage	V_{OUT}		-0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}		-20	mA
Output diode current	I_{OK}		±20	mA
Output current	I_{OUT}		±35	mA
V_{CC}/ground current	I_{CC}		±75	mA
Power dissipation	P_D	(Note 2)	500	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: DC input voltage (V_{IN}) specified is measured to GND and is not related to V_{CC}.
The operating range is 0 V to 15 V and it is possible to convert logic-levels from 15 V to 5 V or 5 V to 2 V.

Note 2: 500 mW in the range of T_a = -40 to 65 °C. From T_a = 65 to 85 °C a derating factor of -10 mW/°C shall be applied until 300 mW.

11. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CC}			2.0 to 6.0	V
Input voltage	V_{IN}			0 to 15.0	V
Output voltage	V_{OUT}			0 to V_{CC}	V
Operating temperature	T_{opr}			-40 to 85	°C
Input rise and fall times	t_r,t_f		V_{CC} = 2.0 V	0 to 1000	ns
			V_{CC} = 4.5 V	0 to 500	
			V_{CC} = 6.0 V	0 to 400	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

12. Electrical Characteristics

12.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				4.5	3.15	—	—	
				6.0	4.20	—	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	V
				4.5	—	—	1.35	
				6.0	—	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	2.0	—	V
				4.5	4.4	4.5	—	
				6.0	5.9	6.0	—	
			I_{OH} = -6 mA	4.5	4.18	4.31	—	
			I_{OH} = -7.8 mA	6.0	5.68	5.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	V
				4.5	—	0.0	0.1	
				6.0	—	0.0	0.1	
			I_{OL} = 6 mA	4.5	—	0.17	0.26	
			I_{OL} = 7.8 mA	6.0	—	0.18	0.26	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	μA
		V_{IN} = 15 V		6.0	—	—	±0.5	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	1.0	μA

12.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	—	V
				4.5	4.4	—	
				6.0	5.9	—	
			I_{OH} = -6 mA	4.5	4.13	—	
			I_{OH} = -7.8 mA	6.0	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
			I_{OL} = 6 mA	4.5	—	0.33	
			I_{OL} = 7.8 mA	6.0	—	0.33	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	±1.0	μA
		V_{IN} = 15 V		6.0	—	±5.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	10.0	μA

12.3. AC Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Note	Test Condition	C_L (pF)	V_{CC} (V)	Min	Typ.	Max	Unit
Output transition time	t_{TLH},t_{THL}		—	50	2.0	—	25	60	ns
					4.5	—	6	12	
					6.0	—	5	10	
Propagation delay time	t_{PLH},t_{PHL}		—	50	2.0	—	30	75	ns
					4.5	—	9	15	
					6.0	—	8	13	
				150	2.0	—	45	100	
					4.5	—	14	20	
					6.0	—	12	17	
Input capacitance	C_{IN}		—			—	5	10	pF
Power dissipation capacitance	C_{PD}	(Note 1)	—			—	26	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

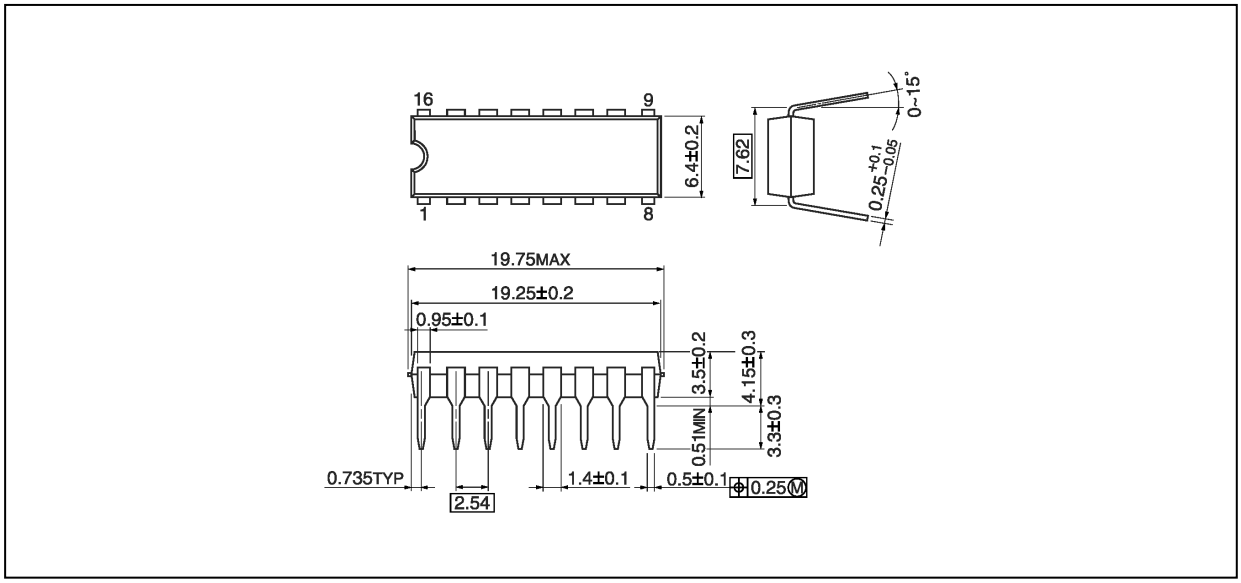
$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/6$ (per gate)

12.4. AC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	C_L (pF)	V_{CC} (V)	Min	Max	Unit
Output transition time	t_{TLH},t_{THL}	—	50	2.0	—	75	ns
				4.5	—	15	
				6.0	—	13	
Propagation delay time	t_{PLH},t_{PHL}	—	50	2.0	—	95	ns
				4.5	—	19	
				6.0	—	16	
			150	2.0	—	145	
				4.5	—	29	
				6.0	—	25	
Input capacitance	C_{IN}	—			—	10	pF

Package Dimensions

Unit: mm



Weight: 1.00 g (typ.)

Package Name(s)
Nickname: DIP16

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