# TC3567DFSG-002 Bluetooth<sup>®</sup> low energy IC

# **Rev 1.2**



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### 1. General Description

#### 1.1. Product Concept

TC3567DFSG (Later omitted TC3567D.) are compliant with 2.4-GHz wireless communication, Bluetooth<sup>®</sup> Ver4.2 low energy. RF analog parts and baseband digital parts are built in them, and TC3567D provides Bluetooth<sup>®</sup> HCI (Host Control Interface) functions and Bluetooth<sup>®</sup> low energy GATT profile functions defined by Bluetooth<sup>®</sup> core specifications. TC3567D works as a standalone application using Bluetooth<sup>®</sup> low energy communication system by connecting EEPROM (written a program for standalone use) by I<sup>2</sup>C connection. The TC3567D can be connected to an external host CPU by the UART and controlled with the HCI or the GATT/SM layer control command.

#### 1.2. Features

- > Compliant with Bluetooth<sup>®</sup> Ver4.2 low energy
  - ♦ Built-in Bluetooth<sup>®</sup> Baseband Circuit
  - ♦ Built-in Bluetooth<sup>®</sup> RF analog Circuit
    - Transmission electric power: 0 dBm
    - Receiver sensitivity: -93.5 dBm
    - RSSI accuracy: ±1 dB (-90 to -10 dBm@input)
    - Internal matching circuit
  - ♦ Built-in ARM® Cortex®-M0 (13 MHz or 26 MHz operation frequency is able to select to run)
  - ♦ Built-in masking ROM
    - Boot program
    - HCI/ extension HCI command
    - GATT/SM layer control API (TCU command; <u>T</u>oshiba <u>Command Unit</u>)
    - API for hardware control
  - ♦ Retention SRAM (128 KB with 51 KB available for the user area)
  - ♦ Support up to 4 patch program loader functions and auto patch function
- General Purpose IO (17 ports)
- > General Purpose Serial Interfaces
  - ♦ SPI interface (1 ch assigned to a General Purpose IO)
  - ♦ I<sup>2</sup>C interface (1 ch assigned to a General Purpose IO)
- Host CPU Interface
  - ♦ UART interface (9600 bps to 921.6 kbps, 1ch shared with GPIOs)
  - ♦ SPI interface
- > Emulator debug control interface
  - SWD (Serial Wire Debug) 2-wire (1 ch, There are two types of products, enabled or disabled for SWD function.)
  - Wake-up Interface (2 ch assigned to a General Purpose IO)
    - ♦ Wake-up input function from sleep and deep sleep
- > PWM Interface (4 ch assigned to General Purpose IOs)
- Reference Clock Input (26 MHz)
  - ♦ Built-in oscillator for crystal oscillator connection
- Sleep Clock Input (32.768 kHz)
  - ♦ Built-in oscillator for crystal oscillator connection
- Works as Standalone (In User-App mode, operating by standalone is possible)
- > Sleep and Deep Sleep Functions
- Built-in DCDC converter and LDO
  - Wide range of input power supply voltages supported (Booting power supply voltage : 1.8 to 3.6 V, low battery voltage detection)

- > Built-in general purpose ADC
  - ♦ External analog inputs assigned to GPIOs (5 ch)
  - Internal VDD monitoring (1 ch connected inside)
- RNG function
  - ♦ Random number generator by DRBG and ESG (up to 256 bit)
  - ♦ Support random number test for NIST SP800-22 and BSI
- > RTC
  - ♦ RTC function which has a frequency accuracy of Sleep clock
  - Clock/calendar function: YY/MM/DD, hh:mm:ss (24-hour clock system), and day of the week
  - Alarm function: hh:mm, set the alarm by day or day of the week, and alarm-triggered interrupt
  - ♦ Leap year function (Not supported for exception handling in every 100th year)
  - ♦ Available during Sleep and Backup modes
- Package:
  - ♦ TC3567DFSG: QFN Package [40 pin, 5 x5 mm, 0.4 mm pitch, 0.9 mm thickness]

### 2. Pin Function

2.1. TC3567DFSG Pin Assignment (Top View)



Figure 2-1 Pin Assignment (Top View)

### 2.2. Pin Function Descriptions

Table 2-1 shows attributes, input/output states for operating modes and descriptions for pin functions. Table 2-4 shows descriptions about power supply pins.

Pin name	Pin No.	Attribute	Condition	Functional description
		VDD category	Default	
		Direction	(during reset)	
		Туре		
			Reset interface	
RESETX	3	VDDIO	—	Hardware reset input pin.
		IN		Setting this pin to Low level put the system at reset
		Schmitt trigger		state.
			Clock interface	
XOIN	11	VDDCORE	IN	Reference clock input pin. Please use oscillator with
		IN		26 MHz and < 50 ppm accuracy.
		OSC		A feedback resistor is built in between XOIN pin and
				XOOUT pin and a capacity array which can set
				parameters in the crystal oscillation circuit is built-in,
				so that external feedback resistances and
				capacities are unnecessary.
XOOUT	12	VDDCORE	OUT	Oscillator output for Baseband and RF reference
		OUT		clock (26 MHz) pin.
		OSC		A feedback resistor is built in between XOIN pin and
				XOOUT pin and a capacity array which can set
				parameters in the crystal oscillation circuit is built-in,
				so that external feedback resistances and
				capacities are unnecessary.
SLPXOIN	21	VDDIO	IN	Sleep clock input pin from oscillator. Please use an
		IN		oscillator with 32.768 kHz and < 500 ppm accuracy.
		OSC		A feedback resistor is built in between SLPXOIN pin
				and SLPXOOUT pin and a capacity array which
				can set parameters in the crystal oscillation circuit is
				built-in, so that external feedback resistances and
				capacities are unnecessary.
SLPXOOUT	22	VDDIO	OUT	Oscillator output (feedback) pin for the oscillation of
		IN/OUT		32.768 kHz.
		OSC		

#### Table 2-1 Pin Functions

### TC3567DFSG-002

Pin name	Pin No.	Attribute	Condition	Functional description
		VDD category	Default	7
		Direction	(during reset)	
		Туре		
			RF interface	
RFIO	7	VDDCORE		RF I/O pins.
		IN/OUT		This product incorporates the 50 $\Omega$ matching circuit,
		Analog		so that external matching circuit is unnecessary.
				The RF output pattern should wire with the 50 $\Omega$
				transmission line.
				For details, refer to the hardware application note of
				this product.
			General purpose I/O por	t
GPIO0	31	VDDIO	Refer to Table 2-2	General purpose I/O pin.
GPIO15	33	IN/OUT		During reset, the input will be disable state with
		Pull-up		disconnecting the Pull-up/Pull-down resistor.
		Pull-down		After the pin configuration by software processing, it
		Schmitt trigger		works as a GPIO pin of the input and output or
				Table 2-2 function.
				Please refer to Table 2-2.
GPIO1	40	VDDIO	Refer to Table 2-2	General purpose I/O pin.
GPIO2	16	IN/OUT		During reset, the input will be disable state with
GPIO5	36	Pull-up		connecting the Pull-up resistor.
GPIO6	37	Pull-down		After the pin configuration by software processing, it
GPIO7	38	Schmitt trigger		works as a GPIO pin of the input and output or
GPIO8	39			Table 2-2 function.
GPIO11	35			Please refer to Table 2-2.
GPIO12	34			In addition, GPIO1 pin is used in the case of
GPIO25	2			switching operation modes.
				GPIO11 and GPIO12 are used as the ports for
				connecting to EEPROM written an user application
				program, to download a software written in
				EEPROM during booting.
GPIO3	30	VDDIO	Refer to Table 2-2	ADC input and general purpose I/O pin.
GPIO4	29	IN/OUT		During reset, the input will be disable state with
GPIO9	28	Pull-up		disconnecting the Pull-up/Pull-down resistor.
GPIO10	26	Pull-down		After the pin configuration by software processing, it
GPIO14	24	Schmitt trigger		works as a GPIO pin of the input and output or
				Table 2-2 function.
				Please refer to Table 2-2.
GPIO13	25	VDDIO	Refer to Table 2-2	General purpose IO pin.
		IN/OUT		During reset, the input will be disable state with
		Pull-up		connecting the Pull-up resistor.
		Pull-down		After the pin configuration by software processing, it
		Schmitt trigger		works as a GPIO pin of the input and output or
				Table 2-2 function.
				Please refer to Table 2-2.

### TC3567DFSG-002

Pin name	Pin No.	Attribute	Condition	Functional description
		VDD category	Default	
		Direction	(during reset)	
		Туре		
SWDCLK	32	VDDIO	Pull-down	Serial Wire debugger clock pin.
		IN		During the reset, it remains in the input state with
		Pull-up		connecting the Pull-down resistor. After the reset is
		Pull-down		released, it will be the input of the Serial Wire
		Schmitt trigger		Debugger clock.
				When not used, this pin should be open.
SWDIO	17	VDDIO	Pull-up	Serial Wire Debugger data pin and operation
		IN/OUT		switching pin.
		Pull-up		During the reset, it remains in the input state with
		Pull-down		connecting the Pull-up resistor. After the reset is
		Schmitt trigger		released, it will be the input and output of the Serial
				Wire Debugger data.
				When not used, this pin should be open.
			IC test interface	
TMODE	4	VDDIO	—	Test mode setting pin.
		IN		This pin is used for IC manufacturing test and need
		Schmitt trigger		to be connected to GND when assembled on a
				board.
TRTEST1	9	VDD12A	_	Analog test pins.
TRTEST2	10	IN/OUT		These pins are used for IC manufacturing test and
		Analog		need to be connected to GND when assembled on
				a board.

### 2.3. GPIO function list

GPIO pins can be assigned to UART I/Fs, serial memory I/Fs and etc. by TC3567D firmware or command from external Hosts. Table 2-2 shows available functions, during reset status and software controlling after reset release for each GPIO pin, and Table 2-3 shows examples of GPIO function settings. About what function name shown in Table 2-2 is assigned to a plurality of pins in the same, please note that it cannot be assigned to select a plurality of pins at the same time.

Pin	During reset status	After reset release	Function 1	Function 2	Function 3	Function 4	Analog input	Pin state at unused
GPIO0	Disable/ Hi-Z	Disable/ Disconnection: Pull-up, Pull-down	WakeUp0 Input	_	_	_	_	Open
GPIO1	Disable/ Pull-up	Input/ Pull-up (Note2)	PWM0 Output	_	_	_	_	Open (Note1)
GPIO2	Disable/ Pull-up	Input/ Pull-up (Note2)	PWM1 Output	—	—	—	_	Open (Note1)
GPIO3	Disable/ Hi-Z	Disable/ Disconnection: Pull-up, Pull-down	PWM2 Output	SPI-DOUT Output	—	—	ADC1 Input	Open
GPIO4	Disable/ Hi-Z	Disable/ Disconnection: Pull-up, Pull-down	PWM3 Output	SPI-DIN Input	_	_	ADC2 Input	Open
GPIO5	Disable/ Pull-up	Input/ Pull-up (Note3)	UART1-TX Output	SPI-DOUT Output	_	_	_	Open
GPIO6	Disable/ Pull-up	Input/ Pull-up (Note3)	UART1-RX Input	SPI-DIN Input	_	_	_	Open
GPI07	Disable/ Pull-up	Input/ Pull-up	I2C-SCL Output	_	SPI-SCS Output	UART1-RTSX Output	_	Open
GPIO8	Disable/ Pull-up	Input/ Pull-up	I2C-SDA I/O	_	SPI-SCLK Output	UART1-CTSX Input	_	Open
GPIO9	Disable/ Hi-Z	Disable/ Disconnection: Pull-up, Pull-down	_	_	_	_	ADC3 Input	Open
GPIO10	Disable/ Hi-Z	Disable/ Disconnection: Pull-up, Pull-down	_	_	_	_	ADC4 Input	Open
GPIO11	Disable/ Pull-up	Input/ Pull-up	I2C-SCL Output (Note4)	SPI-DOUT Output	_	_	_	Open
GPIO12	Disable/ Pull-up	Input/ Pull-up	I2C-SDA I/O (Note4)	SPI-DIN Input	_	_	_	Open
GPIO13	Disable/ Pull-up	Input/ Pull-up	UART1-RTSX Output	_	_	_	_	Open
GPIO14	Disable/ Hi-Z	Disable/ Disconnection: Pull-up, Pull-down	UART1-CTSX Input	_	_	_	ADC5 Input	Open
GPIO15	Disable/ Hi-Z	Disable/ Disconnection: Pull-up, Pull-down	WakeUp1 Input	_	_	_	_	Open
GPIO25	Disable/ Pull-up	Input/ Pull-up	_	_	_	_	_	Open

Table 2-2 Available functions for GPIO

Note1: Handle with care because of using operation mode switching.

Note2: Except in User-App mode, it becomes Pull-down.

Note3: In the HCI mode, the pull-up / pull-down resistor is disconnected.

Note4: GPIO11 and GPIO12 are used as the ports for connecting to EEPROM written an user application program, to download a software written in EEPROM during booting.

Note: About the GPIO pin state, the state in case of using in the user application mode is shown. When it is turned on in HCI mode, a part of the state becomes different. Therefore, for detail states of each pin, refer to the software application note.

Pin name	Example of basic setting	Example of function setting 1	Example of function setting 2	Example of function setting 3	ADC
GPIO0	WakeUp0	_	_	_	_
GPIO1	PWM0	PWM0	_	—	_
GPIO2	PWM1	PWM1	—	—	—
GPIO3	SPI-DOUT	PWM2	SPI-DOUT	—	ADC1
GPIO4	SPI-DIN	PWM3	SPI-DIN	—	ADC2
GPIO5	UART1-TX	UART1-TX	SPI-DOUT	—	—
GPIO6	UART1-RX	UART1-RX	SPI-DIN	—	—
GPIO7	SPI-SCS	I2C-SCL	-	SPI-SCS	—
GPIO8	SPI-SCLK	I2C-SDA	—	SPI-SCLK	—
GPIO9	ADC3	—	—	—	ADC3
GPIO10	ADC4	—	—	—	ADC4
GPIO11	I2C-SCL	I2C-SCL (Note1)	SPI-DOUT	—	—
GPIO12	I2C-SDA	I2C-SDA (Note1)	SPI-DIN	—	—
GPIO13	UART1-RTSX	UART1-RTSX	32kHz output	—	—
GPIO14	UART1-CTSX	UART1-CTSX	32kHz output	—	ADC5
GPIO15	WakeUp1				—
GPIO25	GPIO25	_	—	—	—

#### Table 2-3 Example of GPIO function setting

Note1: GPIO11 and GPIO12 are used as the ports for connecting to EEPROM written an user application program, to download a software written in EEPROM during booting.

Note: For details, refer to the firmware specifications since other settings of those shown in this table may be possible.

### 2.4. Power Supply Pins

Table 2-4 shows the attributes and descriptions of power supply pins for normal operations.

#### Table 2-4 Power supply pins

Pin name	Pin number	Attribute	Description
		Type VDD/GND	
			VDD/GND
VPGM	5	TEST	Test pin
		—	Please connect VPGM to GND.
VBAT	18	VBAT	Power supply pin for DCDC and sleep circuit.
		VDD	Connect the external power source for DCDC and LDO built into the IC.
LX	19	VBAT	DCDC output pin.
		VDD	Please connect to external inductor for DCDC.
VDDCORE1	14	-	DCDC for feedback input, analog circuit power supply pin.
		VDD	Please connect to external inductor for DCDC.
VDDCORE2	15	-	DCDC for feedback input, digital circuit power supply pin.
		VDD	Please connect to external inductor for DCDC.
VDDIO1	1	VDDIO	IO power supply
VDDIO2	23	VDD	Power supply pin for GPIO.
VSSA	8	Analog	GND pin for analog, this pin needs to be connected to GND
VOOR		GND	
VSSRFIO	6	Analog	GND pin for RFIO, this pin needs to be connected to GND.
		GND	
VSSX	13	Analog	GND pin for OSC, this pin needs to be connected to GND.
		GND	
VSSDC	20	Digital	GND pin for DCDC, this pin needs to be connected to GND.
		GND	
VSSD1	27	Analog,	GND pin for analog, digital common, this pin needs to be connected to GND.
VSSD2	FIN	Digital	Connect the exposed Die Pad to GND because this pad is digital ground as
		GND	well.

### 3. System Configuration

### 3.1. Block Diagram

Figure 3-1 shows block diagram of TC3567D. TC3567D is powered by single voltage between 1.8 V and 3.6 V. The chip has built-in DCDC and LDO requiring external capacitors. It uses 26 MHz reference clock and 32.768 kHz sleep clock. External memory Interface is SPI or I<sup>2</sup>C, and host CPU interface is UART.



Figure 3-1 Example of TC3567D system configuration

### 3.2. Boot Sequence

The boot sequence of TC3567D is as shown below.

Depending on the pin state of GPIO1 at the time of reset release, it can be used to switch between User-App mode and HCI mode.





### 4. Functional Specifications

### 4.1. Bluetooth<sup>®</sup> Function

The Bluetooth<sup>®</sup> function is realized by using the hardware which is configured with RF analog and baseband, and the software on a mask ROM. Only connecting a crystal oscillator and some discrete parts externally, the Bluetooth<sup>®</sup> wireless communication can work.

### 4.1.1. Supported Function

This function is compliant with Bluetooth® V4.2 low energy standard. Main supported functions are shown below.

ltems	Description	Notes
Bluetooth Core	4.2	LE is supported.
v4.0 features	Central	Supported
	Peripheral	Supported
	Multi Profile/point	Supported
	Connection Update	Supported
	Random Address	Supported
	WhiteList	Supported
	Security Property (Just Works)	Supported
	Security Property (PassKey Entry)	Supported
	Security Property (OOB)	Supported
	Security Property (Numeric Comparison)	Supported
	GATT-Client	Supported
	GATT-Server	Supported
	Broadcaster	Supported
	Observer	Supported
v4.1 features	Low Duty Cycle Directed Advertising	Supported
	32-bit UUID support in LE	Supported
	LE L2CAP Connection Oriented Channel Support	Not supported
	LE Privacy v1.1	Supported
	Connection Parameter Request Procedure	Supported
	Extended Reject Indication	Supported
	Slave-initiated Features Exchange	Supported
	LE Ping	Supported
	Act as LE Master and LE Slave at the same time	Supported
	Act as LE Slave to more than one LE Master at the same time	Supported
v4.2 features	LE Data Packet Length Extension	Supported (Note)
	LE Secure Connections	Supported
	Link Layer Privacy	Not supported
	Link Laver Extended Scanner Filter Policies	Supported

#### Table 4-1 List of supported functions

Note: LE Data Packet Length Extension is supported but maximum Tx octets is limited by maximum MTU size; 158 octets.

### 4.1.2. Support Protocol Layer

Following figure shows the Bluetooth Protocol and Profile Layer supported. It has RF control, Link layer, internal HCI, L2CAP, ATT, SMP and GATT.



Figure 4-1 Protocol Layer

### 4.1.3. RF

Since the RF analog part of TC3567D builds in not only transmission and reception circuits but also the RF switch and the matching circuit, the RFIO pin which is a single I/O does not need an external matching circuit. The wireless device which suits for RF-PHY specifications of Bluetooth<sup>®</sup> low energy can be realized easily by connecting to 50  $\Omega$  wiring.

The transmission power can be selected from intended power between 0 and -20 dBm (4 dB steps). Not only default transmission power but also transmission power to the specified destination can be set. The RSSI of reception block has an accuracy of  $\pm 2$  dB (typ.) to the input signal between -90 and -10 dBm.

### 4.1.4. Auto Advertise Function

Using an auto advertise function enables repeating transmissions of advertise packets with very small power. The auto advertise function is a function which transmits intended advertise packets without waking CPU up in Backup mode. Then, a scan request and a connection request can be also received. The response to the remote device can be preset in case of receiving a scan request, and when one connection request is received, this function wakes CPU up and leaves a subsequent process to the user software.

### 4.2. Reset Interface (Power up sequence)

### 4.2.1. Features

Reset interface has the following features.

- 1.8 to 3.6 V operation
- > Level sensitive asynchronous reset (Low level: reset)

The external reset signal connected to TC3567D should be at reset status (RESETX = Low) when the power is turned on. When the power supply has become over 1.8 V, to be disable the external reset signal (RESETX = High). Then, the crystal oscillation starts, and an internal timer releases the internal reset after the crystal oscillation has become stable.

### 4.2.2. Connection Example

Reset signal can be input by an RC time constant circuit or an asynchronous level sensitive reset IC. Figure 4-2 shows a connection example where TC3567D is power-supplied by an RC time constant circuit. Reset signal can be given by RC time constant circuit. Figure 4-3 shows the timings to reset and reset-release for the power supply.



#### Figure 4-2 Reset signal connection example



#### Figure 4-3 Power-on reset release sequence

### 4.3. UART Interface

### 4.3.1. Features

TC3567D UART interface has the following features.

- > 1.8 to 3.6 V operation
- > Full-duplex start-stop synchronization data transfer (RX, TX, CTSX, RTSX)
- Two-wire start-stop synchronization data transfer (RX, TX) or four-wire start-stop synchronization data transfer (RX, TX, CTSX, RTSX) are available depending on the settings.
- Start bit field (1 bit), data bit field (8 bit, LSB first), stop bit field (1 bit), no parity bit
- > In HCI mode, UART TX/RX pins can be switched by commands.
- > Programmable baud rate: 9600 bps to 921.6 kbps.
- > More than 3 characters are inserted between TX messages. Interval can be changed on the command.
- > Error detection (receiver timeout error, receiver over run error, receiver frame error)
- Host wake up function

TC3567D communicates commands, status, and data with a host CPU through UART interfaces. The UART interfaces are shared with GPIO pins, and during boot process after a reset, TC3567D firmware assigns UART functions to the GPIOs. The UART interfaces can operate at 1.8 to 3.6 V depending on the VDDIO power supply voltage. Sharing the power supply pin with other hardware interfaces, they cannot operate at a different voltage from the one other hardware interfaces operate at.

### 4.3.2. Connection Example

TC3567D UART can be connected with an UART interface on a host CPU. Figure 4-4 shows an example of two-wire start-stop synchronization data transfer connection with an external host CPU. Figure 4-5 shows the timing when UART is assigned to GPIO and activated.



#### Figure 4-4 UART connection example



#### Figure 4-5 Timing for UART function assignment

### 4.3.3. Frame Format

TC3567D supports the following format:

- Number of data bits: 8 bits (LSB first)
- Parity bit: no parity
- Stop bit: 1 stop bit
- Flow control: RTSX/CTSX

Figure 4-6 shows UART data frame.



#### Figure 4-6 UART data frame

### 4.3.4. Flow Control Function

Hardware flow control is available when TC3567D UART interface is assigned to GPIO5 to GPIO8 (GPIO5, 6, 13, 14) as four-wire start-stop synchronization data transfer. Transmit flow control (CTSX) and receive flow control (RTSX). Figure 4-7 shows signals input and output direction.



#### Figure 4-7 UART connection example

CTSX (Clear to Send) input signal is used for UART transmitting. Low input indicates the peer device (for example, the host in the Figure 4-7) is ready to receive data, and TC3567D sends data if it has data to transmit. On the other hand, TC3567D stops transmitting on the basis of UART unit frame when CTSX input is high.

RTSX (Request to Send) output signal is used for UART receiving. Low output indicates TC3567D is ready to receive data and requests data to the peer device. TC3567D outputs RTSX low when ready to receive data. When the UART becomes busy and cannot receive data, TC3567D outputs RTSX high, and stops UART communication on the basis of UART unit frame.

Response time of UART transmitting and receiving to flow control signals is between 1 frame to 4 frames depending on the baud rate and internal process status of frame.

### 4.3.5. Baud rate

UART baud rate of TC3567D is generated from 26 MHz clock. It is calculated from the number of oversampling and the division ratio as follows; The oversampling number can be set between 12 and 17. The division ratio can be set between 1 and 65535.

 $UART \text{ baud rate} = \frac{Baud \text{ rate generation clock frequency}}{Number \text{ of oversampling } \times Division \text{ ratio}}$ 

Table 4-2 shows the actual baud rate values that can be set for the TC3567D. The TC3567D can receive data with an error of up to  $\pm 2\%$  of the actual baud rate. Set the baud rate of the host CPU within this range.

ldeal baud rate [bps]	Actual baud rate [bps]	Oversampling number	Division ratio
9600	9587.021	12	226
14400	14396.46	14	129
19200	19174.04	12	113
28800	28856.83	17	53
38400	38461.54	13	52
57600	57777.78	15	30
76800	76923.08	13	26
115200	115555.6	15	15
153600	153846.15	13	13
230400	232142.9	16	7
307200	305882.4	17	5
460800	464285.7	14	4
921600	928571.4	14	2

#### Table 4-2 Typical UART baud rate configuration

### 4.3.6. TX message spacing function

TC3567D spaces more than 12 time frames between different TX messages making less than 12 time frames between TX frames in a TX message when several TX frames belong to one TX message. Host CPU is able to know the boundaries between TX messages by measuring time frames between TX frames.



Figure 4-8 TX frames and TX messages

### 4.3.7. Error Detecting Functions

TC3567D UART interface has 3 kinds of error detecting functions.

- Receiver timeout error
- Receiver over run error
- Receiver frame error

Receiver timeout error detection judges an error if an UART RX message made from several RX frames has an RX frame interval longer than a certain value. The interval is counted by internal timer. Keep the interval between RX frames less than 12 time frames that belong to an RX message. For UART1, keep intervals between different RX messages more than 12 time frames. For example, 115200 bps has 0.087 ms for 1 frame, the interval between RX messages should be longer than 0.087 ms × 12 = 1.04 ms. RX messages that has intervals less than 12 time frames gives an error because TC3567D sees them as one UART RX message. Interval of the received frame is the default in the 12 time frame, but it can be changed by the command.



#### Figure 4-9 RX frames and RX messages

Receiver over run error judges if UART receive frame buffer internal TC3567D is overflowed. Normally, this overflow does not happen when the flow control mentioned in 4.2.4 is activated for data communication.

Receiver frame error judges if failing recognize the unit frame. A frame formation is judged as failure when its start bit is detected and the corresponding stop bit is detected as "0".

### 4.3.8. Host Wake up Function

TC3567D can wakes up its host before sending UART data to the host. This function is disabled by default, but can be assigned to GPIO by command. Host wake up time can be changed by command (10 ms by default).



#### Figure 4-10 Host wake up

### 4.3.9. HCI mode

When TC3567D is used in the HCI mode, UART is the host interface to receive HCI commands. The Bluetooth<sup>®</sup> wireless performance can be tested in HCI mode by the measurement equipment which connects the UART directly.

### 4.3.9.1. HCI Reset

Sends a HCI reset command from the host, at least 150  $\mu$ s from the command complete event can be processed the following command successfully.

### 4.4. SPI Interface

### 4.4.1. Features

TC3567D has the following main features for a serial memory interface

≻	Operation voltage:		1.8 to 3.6 V
$\triangleright$	SPI i	nterface	
	۶	Chip select:	1 ch
	۶	Chip select polarity:	Selectable: High-active and Low-active
	۶	Serial clock master operation:	Polarity and phase are adjustable (4 combinations are selectable)
	۶	Serial clock frequency:	25 Hz to 6.5 MHz
	۶	Serial data transfer mode:	MSB-first, LSB-first

SPI interface can operate at 1.8 to 3.6 V depending on VDDIO, however, cannot operate at different voltage from ones other interfaces are operate at.

### 4.4.2. Connection Example

TC3567D SPI interface can be connected to serial EEPROMs and serial Flash-ROMs and has 1 chip select port. Figure 4-11 shows a connection example, where a serial Flash-ROM is connected to TC3567D SPI interface.



Figure 4-11 Connection example for serial Flash-ROM using SPI interface

### 4.4.3. Frame Format

When the SPI interface is connected to external ICs, the first 8 bit (X7 to X0) specifies the address and read or write mode. The command recognition code type and the address bit width should be determined by the external IC in use. For more information in detail, please refer to the technical documents for the external IC.

Figure 4-12 shows an example where 8-bit address is written and then 8-bit data is read. Figure 4-13 shows an example where 8-bit address is written and then 8-bit data is written.



Figure 4-12 SPI format (single byte read)



Figure 4-13 SPI format (single byte write)

### 4.5. I<sup>2</sup>C Interface

### 4.5.1. Features

I<sup>2</sup>C has the following main features for a serial interface.

- Operation voltage: 1.8 to 3.6 V
- I<sup>2</sup>C Interface

 $\triangleright$ 

- Operation mode: I<sup>2</sup>C bus master
- > Serial clock frequency: Standard mode (Max 100 kHz), Fast mode (Min 100 kHz to Max 400 kHz)
  - Output mode: Open-drain output, CMOS output
- > Device address format: 7-bit address (10-bit address is not supported)

 $I^2C$  interface can operate at 1.8 to 3.6 V depending on VDDIO, however, cannot operate at different voltage from ones other interfaces are operate at.

### 4.5.2. Connection Example

Figure 4-14 shows a connection example of a serial EEPROM using I<sup>2</sup>C bus interface of the open-drain mode. External pull-up resistors (Rext) are necessary for both serial clock line and serial data line.

Figure 4-15 shows another connection example where  $I^2C$  bus is in the CMOS output mode. Only the serial data line needs Rext because this line can be driven by neither TC3567D nor a serial EEPROM.



Figure 4-14 Connection example for serial EEPROM with I<sup>2</sup>C-bus interface (Open-drain output)



Figure 4-15 Connection example for serial EEPROM with I<sup>2</sup>C-bus interface (CMOS output)

### 4.5.3. Selection of External Pull-up Resistor Value

An external pull-up resistor value needs to be selected by the following equations in case of  $I^2C$  bus interface. Its maximum value is defined by equation (1), in which  $t_r$  is rise time of serial clock and data and  $C_b$  is  $I^2C$  bus capacity. Its minimum value is defined by equation (2), in which VDDIO is a supply voltage for TC3567D,  $V_{ol_max}$  is the maximum value of low level output voltage, and  $I_{ol}$  is the low level output current. Please set the pull-up resistor value between these lower and upper limits.

$$R_{\text{ext}_{max}} = \frac{t_r}{0.8473 \times C_b} \tag{1}$$

$$R_{\text{ext}\_\min} = \frac{VDDIO - V_{ol}\_\max}{I_{ol}}$$
(2)

TC3567D supports  $I^2C$  bus standard mode (Max 100 kHz) and  $I^2C$  bus fast mode (Min 100 kHz to Max 400 kHz). The rise time tr is 1000 ns for the standard mode and it is 300 ns for the fast mode. C<sub>b</sub> can vary depending on the IC board and how it is implemented. Table 4-3 and Table 4-4 show examples when  $I^2C$  bus capacity is 20 pF.

I <sup>2</sup> C bus frequency	Max 100 kHz								
tr [ns]	1000								
Cb [pF]				20					
VDDIO [V]	1.8			3.0			3.6		
Vol_max [V]	0.3		0.4			0.4			
lol [mA]	1	1 2 4		1	2	4	1	2	4
Rext_min [k $\Omega$ ]	1.50	1.50 0.75 0.38		2.60	1.30	0.65	3.20	1.60	0.80
Rext_max [k $\Omega$ ]	59.01								

#### Table 4-3 External pull-up resistor value for $l^2C$ standard mode (Cb = 20 pF)

Table 4-4 External pull-up resistor value for I <sup>2</sup> C fast mode (Cb = 20 pF)	$^{-}$ I <sup>2</sup> C fast mode (Cb = 20 pF)
---	--

I <sup>2</sup> C bus frequency		Min 100 to Max 400 kHz							
tr [ns]		300							
Cb [pF]		20							
VDDIO [V]		1.8		3.0			3.6		
Vol_max [V]		0.3		0.4			0.4		
lol [mA]	1	2	4	1	2	4	1	2	4
Rext_min [ $k\Omega$ ]	1.50	0.75	0.38	2.60	1.30	0.65	3.20	1.60	0.80
Rext_max [k $\Omega$ ]	17.70								

### 4.5.4. Frame Format

For I<sup>2</sup>C format, TC3567D first generates start condition. Then, it sends device recognition address (7 bit: [A6:A0]) and the first byte address ([B7:B0]) for the access target. Next, it goes for read or write sequence. For I<sup>2</sup>C, every data is sent as MSB first. How to specify the value and byte address of the device identification address, and it has been determined in accordance with the device to be connected. In order to be connected, it must match the device to be connected. For read operation, TC3567D returns to the serial memory either receive acknowledge bit (ACK) or receive not acknowledge bit (NACK) every time it receives one byte. For write operation, TC3567D receives either ACK or NACK from the serial memory every time it sends one byte. It can handle not only one byte but also several bytes in a row. TC3567D generates stop condition when it has finished all the read or write of data.

Figure 4-16 shows an example where TC3567D reads two-byte data. Figure 4-17 shows an example where TC3567D writes two-byte data. In these examples, gray texts and lines indicate signals that are given by the serial memory. For read operation, after having read the final byte data, TC3567D returns NACK with which the serial memory gets to know the completion of the read operation.



Figure 4-16 I<sup>2</sup>C format (Serial memory, read)



Figure 4-17 I<sup>2</sup>C format (Serial memory, write)

### 4.6. PWM Interface

TC3567D has a PWM interface that can be used for LED, buzzer control, etc.

The PWM interface has the following features.

- > Arbitrary pulse generation function
- > It can select the source clock from 13 MHz and 32.768 kHz
- > It has 12-bit clock division setting up to 1/4096: 8 Hz to 16.384 kHz (32.768 kHz), 3.17 kHz to 6.5 MHz (13 MHz)
- > The pulse output can be masked by the regular pattern whose period is one second with 50 ms unit width (Rhythm function).
- > It can generate an interrupt which is synchronized to the rhythm pattern period 1 s.
- It can switch the pulse output to Low / High active
- > It can adjust the duty cycle of the pulse output.

### 4.6.1. Pulse Generation Function

Figure 4-18 shows a brief explanation of the pulse generation. TC3567D can adjust output pulse frequency by changing its cycle. Also it can adjust on/off ratio by changing its duty.

The cycle (frequency) can be set from 8 Hz to 16.384 kHz for 32.768 kHz clock, and from 3.17 kHz to 6.5 MHz for 13 MHz clock. The duty can be set from 0% to 100%



Figure 4-18 PWM pulse generation function

### 4.6.2. Rhythm Function (Output Masking)

Figure 4-19 shows the brief explanation of PWM rhythm function. In addition to the one for pulse generation, TC3567D has another timer that has 50 ms  $\times$  20 = 1 s (rhythm counter). That timer has 20-bit register (pattern register), each bit corresponds to the rhythm counter that counts down in every 50 ms. When the pattern register is zero, the PWM output is masked to zero or one. Using this function, LED or buzzer can be on with 1 s periodical pattern



Figure 4-19 PWM Rhythm Function

### 4.7. ADC

### 4.7.1. Features

TC3567D has 6 ch of 10-bit ADCs for battery monitoring, analog inputs from external sensors, for example. The ADC has the following features.

- > 5 ch for analog inputs Note: Analog inputs are shared with GPIO pins.
- > 1 ch for VBAT voltage monitor
  - Note: The reference input is internally connected to VBAT, and the analog input is to built-in VDDCORE2 output. Please refer to 4.7.2 for how to calculate voltage value.
- Maximum conversion rate: 1 MS/s

### 4.7.2. Descriptions

The ADC has 10 bits conversion accuracy and can work for input voltages from 0 V to 3.6 V (VBAT). It has 6 ch of analog inputs, and the ch0 is connected to VDDCORE2 output, and the ch1 to ch5 are shared with GPIO pins.

When a battery is used as power source, the reference voltage can slide over time because the battery is connected as reference voltage. In that case, the VDDCORE2 output voltage connected to ch0 can be used as a reference voltage. The input voltage to ch1 to ch5 is converted by the reference voltage of ch0 and the converted value is used to calculate a correct digital value by the CPU. The following shows the conversion method of the input voltage.

Voltage A at time T can be calculated as follows

- (1) VDDCORE2 output voltage (VDDCORE2) on Ch0 should be converted by the ADC. The converted digital value is X.
- (2) The analog signal on Ch1 is converted and the converted digital value is Y.
- (3) When the absolute value of the analog signal on Ch1 is defined as A (V), VDDCORE2 (V) / A (V) = X / Y. So,

 $A(V) = VDDCORE2(V) \times Y / X$ 

Calculation example:

Suppose ch0 (for ex. VDDCORE2 output is 1.2 V) is converted to 0x0134, and ch1 (measurement target) is converted to 0x0188, the absolute voltage at ch1 A (V) is given by  $1.2 \times 0x0188 / 0x0134 = 1.2 \times 392 / 308 = 1.527$  (V).

Figure 4-20 shows conceptual of voltage conversion.



#### Figure 4-20 Voltage conversion concept

The ADC converts inputs from ch selected by register settings. When a conversion has finished, the CPU detects it by the interrupt or register polling, and then returns the results. The maximum sampling rate depends on software load on the CPU.

Note: The numerical values are expressed as follows. Hexadecimal number: 0xABC

### 4.8. IC Reference Clock Interface

### 4.8.1. Features

TC3567D has the following features for IC reference clock interface.

Clock frequency: 26 MHz (please adjust the accuracy to < 50 ppm at the temperature in use)

TC3567D doesn't require external feedback resistors and load capacitor because it has an internal feedback resistor and capacitor array. Please adjust capacitor array, based on the specification of the used oscillator and PCB layout and assembly.

### 4.8.2. Connection Example



Figure 4-21 Crystal oscillator connection example

### 4.9. Sleep Clock Interface

TC3567D has the following features for sleep clock interface.

- > Crystal oscillator can be connected.
- Clock frequency: 32.768 kHz (please adjust the frequency accuracy to less than or equal to ±500 ppm at the temperature in use.)

Crystal oscillator is connected between SLPXOIN pin and SLPXOOUT pin. TC3567D doesn't require external feedback resistors and load capacitor because it has an internal feedback resistor and capacitor array between SLPXOIN pin and SLPXOOUT pin. Please adjust capacitor array based on PCB layout and assembly if necessary within the range of the crystal's specification.

### 4.9.1. Sleep Clock Connection Example



Figure 4-22 Crystal oscillator connection example

### 5. Electric Characteristics

### 5.1. Absolute Maximum Ratings

Absolute maximum ratings must not be exceeded even for a moment. Voltages, currents, and temperatures that exceed the absolute maximum ratings can cause break-downs, degradations, and damages not only for ICs but also for other components and boards. Please make sure application designs not to exceed the absolute maximum ratings in any situation.

Itomo	Symbols	Rati	ngs	Linite
ilems	Symbols	Min	Max	UTIIIS
Power supply	VBAT	0.3	+3.0	V
	VDDIO (Note1)	-0.3	т <u>э</u> .э	
Input voltage	VIN	-0.3	VDDIO + 0.3 (Note2)	V
Output voltage	VOUT	-0.3	VDDIO + 0.3 (Note2)	V
I/O pin Input current	IIN	-10	+10	mA
Input power	RFIO	_	+6	dBm
Storage temperature	Tstg	-40	+125	°C

Note1: Do not connect VBAT to GND while VDDIO is powered. Current from VDDIO to VBAT through IC may cause damages, break-downs, and degradations.

Note2: Please use VDDIO + 0.3 V not to exceed 3.9 V.

### 5.2. Operating Conditions

TC3567D can operate normally with proven quality under the operating ranges. Any diversion from the operating ranges may cause false operation. Thus, please make sure application design to comply these operating ranges.

	Itomo	Sumbolo.			Linito	
	liems	Symbols	Min	Тур.	Max	Units
	VBAT Operating Voltage1	VBATopr1	1.80	3.00	3.60	V
Power supply	VDDIO Operating Voltage (Note)	VDDIOopr	1.80	3.00	3.60	V
	VDDCORE Voltage (Note)	VDDCORE1/ VDDCORE2	_	1.2	_	V
RF	frequency	Fc	2400		2483.5	MHz
Clock	fraguanaiaa	Reference clock Fck	25.99870	26.00000	26.00130	MHz
Clock frequencies		Sleep clock fslclk	32.751616	32.768000	32.784384	kHz
Aml	bient temp.	Та	-40	+25	+85	°C

#### Table 5-2 Operating conditions (VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Note: Please refer to other documents (application note) for our connection examples.

### 5.3. DC electric characteristics

### 5.3.1. Current Consumption (Design value)

This section shows current consumption. When the operating temperature (Ta) is 25°C, and the operation of each power supply pin is in the recommendation connection state of our company, the current consumption is an average value.

#### Table 5-3 Current consumption (VBAT = VDDIO1 = VDDIO2 = 3.0 V, VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Itomo	Symbols	Conditions	Pins		Ratings		Unit
liems	Symbols	Conditions	(Note)	Min	Тур.	Max	
Digital operation	IDD <sub>DIG</sub>				0.0		
Digital operation	(Active1)			_	0.0		
RX	IDD <sub>RX</sub>				2.2		m۸
	(Active2)		VDAI	_	3.3		ШA
ту	IDD <sub>TX</sub>	Output Power=			3.3		
	(Active3)	0 dBm		_			
Low power mode	IDDS1	26 MHz crystal oscillator disabled			25		
With Connection	(Sleep)	32 kHz crystal oscillator enabled		_	2.5	—	
Low power mode	IDDS2	26 MHz crystal oscillator disabled			24		
Without Connection	(Backup)	32 kHz crystal oscillator enabled	VDAI	_	2.4	_	μA
Low power mode	IDDS	26 MHz crystal oscillator disabled			0.05		
Without Connection	(Deep Sleep)	32 kHz crystal oscillator disabled			0.05	_	

Note: Power consumption for IO depends on its settings.

Table 5-4 shows DC electric characteristics for each pin under 25°C ambient temperature.

#### Table 5-4 DC Electric Characteristics (VBAT = VDDIO1 = VDDIO2 = 3.0 V, VSSD = VSSA = VSSRFIO = VSSDC = VSSX = 0 V)

		Con	dition	Magguring Din		Rating		
Items	Symbols	I/F Voltage	Other Condition	(Note 1)	Min	Тур.	Max	Unit
High Level Input Voltage	VIH	3.0 V	LVCMOS	VDDIO	0.8×VDDIO	_	—	V
Low Level Input Voltage	VIL	3.0 V	LVCMOS VDDIO		I	_	0.2×VDDIO	v
High Level			Pull-down Off	VDDIO	-10	_	10	
Input Current	IIH	VDDIO =	Pull-down On		10	_	200	
Low Level		of each pin	Pull-up Off		VDDIO	-10	_	10
Current	IIL		Pull-up On		-200	_	-10	
High Level Output Voltage	VOH	3.0 V	IOH = 1 mA	VDDIO	VDDIO-0.6	_	_	V
Low Level Output Voltage	VOL	3.0 V	IOL = 1 mA	VDDIO	_		0.4	V

Note 1: Please refer to Table 2-4 for power supply line for each pin.

### 5.4. Built-in Regulator Characteristics

Table 5-5 Built-in regulator characteristics (VBAT = 1.8 to 3.6 V, VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Items	Cumbolo.			Ratings				
	Symbols	Pin hames and conditions	Min	Тур.	Max	Units		
Output voltages	Vout	VDDCORE1/		10		V		
	VOULT	VDDCORE2	_	1.2	_	v		

### 5.5. ADC Characteristics

Table 5-6 ADC characteristics (VBAT = 1.8 to 3.6 V, VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Items	Symbols	Symbols Condition		Ratings			
	Symbols	Condition	Min	Тур.	Max	Offic	
Analog reference voltage	VREFH	—	1.8	3.0	3.6	V	
Analog input voltage	VAIN	—	VSSD	_	VREFH	V	

### 5.6. RF Characteristics (Design value)

The following conditions are applicable unless otherwise specified.

- ➤ Ta = 25°C
- ➤ VBAT = 3.0 V
- > fx'tal = 26 MHz (Frequency accuracy is adjusted to  $\pm 2$  ppm at normal temperature)
- > PAOUT= 0 dBm

Table 5-7, Table 5-8 shows RF receiving characteristics and RF transmitting characteristics based on Bluetooth<sup>®</sup> Core Spec. V4.2 low energy.

About some the characteristics data here are design values.

Test Item	Deal/at	bit	ch	Co	dition		Spec.		Linit
Testilem	Packel	DIL	CI.	CO		Min	Тур.	Max	Unit
	255		0.12	n	eak	_	_	Pavg+	
Output Power	octets	PRBS9	10,12,	2	car			3 dB	dBm
	001013		10,00	ave	erage		0	_	
In-band Emissions				-5	MHz		-60	-30	
				-4	MHz		-55	-30	
				-3	MHz		-53	-30	
	255	DDDCO	0,12,	-2	MHz		-48	-20	dPm
	octets	FRDO9	19,39	2	MHz	-	-50	-20	UDITI
				3	MHz	_	-53	-30	
				4	MHz		-56	-30	
				5	MHz		-60	-30	
		11110000		∆f1avg (	11110000)	225	249.3	275	kHz
Modulation	255	10101010	0,12, 10.20	Δf2max	(99.9 %)	99.9	100	_	%
Characteristics	001013	_	19,09	∆f2avç	g /∆f1avg	0.8	0.90	_	Ratio
Carrier frequency	255	10101010		ave	erage		4.4	_	
offset (CFO)	octets	10101010		w	rorst	-150	_	150	KITZ
Carrier frequency	255	10101010	0,12,	Abaaluta	Absolute maximum		4.0	50	
drift	octets		19,39	AUSUILLE			4.9	50	NTIZ
Carrier frequency	255	10101010		Absoluto	maximum		10	20	kHz/50 up
drift Rate	octets			AUSUILLE			4.9	20	κπ2/30 μS

#### Table 5-7 RF Characteristic

#### Table 5-8 RF Characteristics

Test Item	Sub Item	Packet	bit	ch.	Condition	Min	Тур.	Max	Unit																								
Rx Sensitivity	_	37 octets	_	0,12, 19,3	PER=30.8 % at 1500 packets with dirty	_	-93.5	_	dBm																								
					<=7 MHz	_	-38 or less	_																									
					-6 MHz	_	-32	—																									
									-5 MHz	_	-26	_																					
					-4 MHz	_	-30	_																									
					-3 MHz	_	-32	_																									
	PER=30.8 %		D wave:		-2 MHz	_	-35	_																									
C/I and Receiver Selectivity	at 1500	055	PRBS9	0,2,12,	-1 MHz	_	-2	_	JD																								
Selectivity	packets with dirty	255 OCTETS	O wave:	19,37, 30	0 MHz	_	8	_	aв																								
T chomance			PRBS15	55	1 MHz	_	-2	_																									
					2 MHz	_	-30	_																									
					3 MHz	_	-38	_																									
																													4 MHz	_	-40		
						5 MHz	_	-44	_																								
					=>6 MHz	_	-38 or less	—																									
					30-2000 MHz	-30		_																									
Blocking			D wave:	1.5	2003-2399 MHz	-35		_																									
Performance	—	255 octets	PRBS9	12	2484-2997 MHz	-35	_	_	dBm																								
			U wave. Cvv		3000 M-12.75 GHz	-30	_																										
			f1=-50 dBm with		-4 MHz																												
Intermodulation Performance	1500 packets	255 octets	un-modulati on f2=-50 dBm with PBBS15	0,12, 19,39	+4 MHz	30.8	0	_	%																								
Maximum input signal level	PER	255 octets	PRBS9	0,12, 19,39	-10 dBm	30.8	0	_	%																								
PER Report Integrity	PER	255 octets	PRBS9	0,12, 19,39	-30 dBm	50	50	65.4	%																								

Note: C/I characteristic and blocking characteristic has the relief specs of the logo attestation test of Bluetooth<sup>®</sup> maybe applied. The blocking characteristic measures D wave as 12 ch.

### 5.7. AC Interface Characteristics (Design value)

5.7.1. UART Interface

#### Table 5-9 UART Interface AC characteristics

Symbols	ltems	Min	Тур.	Max	Unit
tCLDTDLY	Transmit Data ON from CTSX Low level	192	_	—	ns
tCHDTDLY	Transmit Data OFF from CTSX High level	—		2	byte
tRLDTDLY	Received Data ON from RTSX Low level	0		—	ns
tRHDTDLY	Received Data OFF from RTSX High level	—		8	byte



Figure 5-1 UART Interface Timing Diagram

### 5.7.2. I<sup>2</sup>C Interface

### 5.7.2.1. Normal Mode

Symbols	Items	Min	Тур.	Max	Unit
tDATS	Data set-up time	250	_	_	ns
tDATH	Data hold time	300	_	_	ns
tDATVD	Data validity period	—	_	3450	ns
tACKVD	ACK validity period	—	_	3450	ns
tSTAS	Restart condition set-up time	4700	_	_	ns
tSTAH	Restart condition hold time	4000	_	_	ns
tSTOS	Stop condition set-up time	4000	_	_	ns
tBUF	Bus open period from stop condition to start condition	4700	_	_	ns
tr	Rise up time	_	_	1000	ns
ť	Fall down time	—	_	300	ns
tHIGH	Serial clock period of High	4000	_	_	ns
tLOW	Serial clock period of Low	4700	_	_	ns
Cb	Bus load capacitance	—	_	400	pF



Figure 5-2 I<sup>2</sup>C Interface Normal mode Timing diagram

### 5.7.2.2. Fast mode

Symbols	ltems	Min	Тур.	Max	Unit
tDATS	Data set-up time	100	_	_	ns
tDATH	Data hold time	300	_	_	ns
tDATVD	Datavalidity period	_	_	900	ns
tACKVD	ACKvalidity period	_	_	900	ns
tSTAS	Restart condition set-up time	600	_	_	ns
tSTAH	Restart condition hold time	600	_	_	ns
tSTOS	Stop condition set-up time	600	_	_	ns
tBUF	Bus open period from stop condition to start condition	1300	_	_	ns
tr	Rise up time	20 + 0.1Cb	_	300	ns
ť	Fall down time	20 + 0.1Cb	_	300	ns
tSP	Spike pulse width that can be removed	0	_	50	ns
tHIGH	Serial clock period of High	_	1423	_	ns
tLOW	Serial clock period of Low	_	1423	_	ns
Cb	Bus load capacitance	—	_	400	pF

#### Table 5-11 I<sup>2</sup>C Interface Fast mode AC Characteristics



Figure 5-3 I<sup>2</sup>C Interface Fast mode Timing diagram

### 5.7.3. SPI Interface

#### Table 5-12 SPI Interface

Symbols	Items	Min	Тур.	Max	Unit
tSPICLKCYC	SPI clock cycle	154		_	ns
tSPICLKHPW	SPI clock high pulse width	77	—	—	ns
tSPICLKLPW	SPI clock low pulse width	77	—	—	ns
tSPICSS	SPI chip select setup time	38	—	—	ns
tSPICSH	SPI chip select hold time	77	—	—	ns
tSPIIW	SPI transfer idle pulse width	54		—	ns
tSPIAS	SPI address setup time	38		_	ns
tSPIAH	SPI address hold time	77		_	ns
tSPIDS	SPI data setup time	38		_	ns
tSPIDH	SPI data hold time	77		_	ns

Note: SPI Interface operates on the basis of 1/n frequency of half the frequency of ARM® Cortex®-M0 core clock (6.5 MHz for 13 MHz core clock)



Figure 5-4 SPI Interface timing diagram

### 6. System Configuration Example

An example of system configuration is shown in the following figures.

### 6.1. In HCI mode

- Host interface=UART and 26 MHz Reference Clock= XOSC Connection.
- XOSC (32.768 kHz) of the dotted line enclosure is unnecessary when the external input (HOST common use) is chosen.
- GPIO and SWD of connection is the connection example of when not in use.



Figure 6-1 Example of TC3567DFSG system configuration (HCI mode)

### 6.2. In User-App mode

- XOSC (32.768 kHz) of the dotted line enclosure is unnecessary when the external input (HOST common use) is chosen.
- GPIO and SWD of connection is the connection example of when not in use.



Figure 6-2 Example of TC3567DFSG system configuration (User-App mode)

### 7. Package outline

7.1. Outline dimensional drawing TC3567DFSG (P-VQFN40-0505-0.40-005/F01)



Figure 7-1 Package outline (P-VQFN40-0505-0.40-005/F01)

### 8. Part Numbering Nomenclature



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