

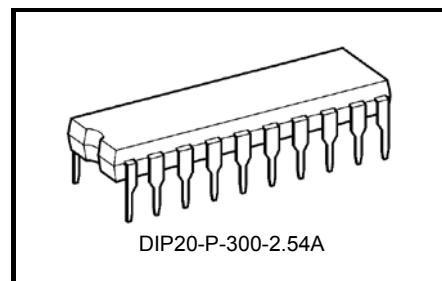
TBD62789APG

8-ch source type DMOS transistor array including D type flip-flop

TBD62789APG is a DMOS transistor array with 8 circuits including D type flip flop logic circuits. Please be careful about thermal conditions during use.

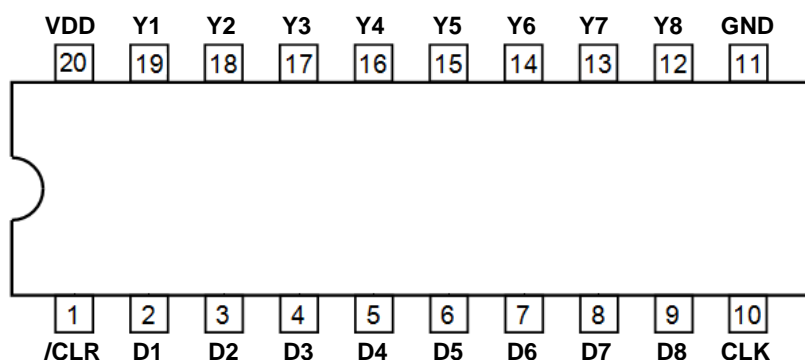
Features

- Built-in 8 circuits
- High output voltage : $V_{OUT} = 50\text{ V (max)}$
- High output current : $I_{OUT} = 500\text{ mA/ch (max)}$
- Package : DIP20-P-300-2.54A



Weight: 1.4 g (typ.)

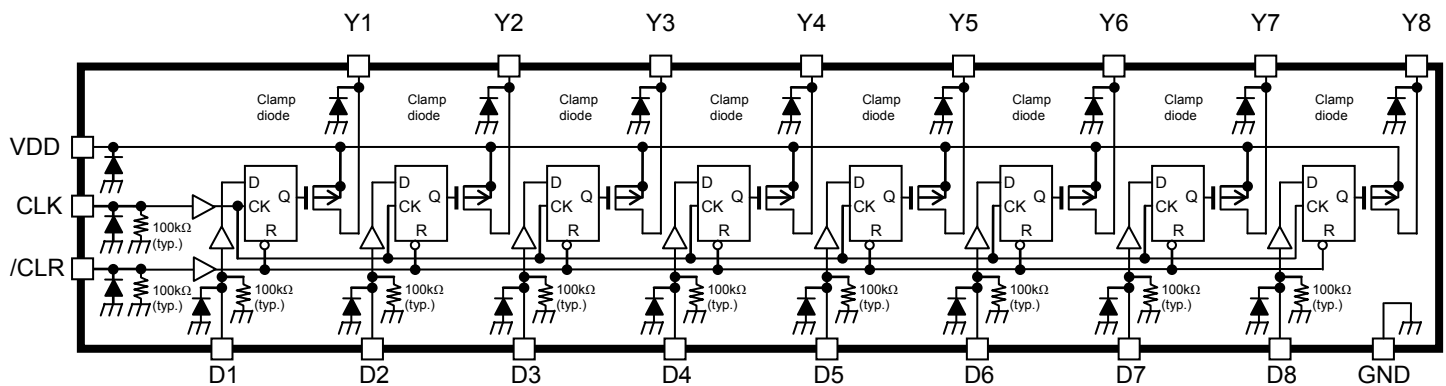
Pin Assignment (top view)



Pin Description

| Pin No. | Pin name | Function |
|---------|----------|----------------------------|
| 1 | /CLR | Input pin of clear signals |
| 2 | D1 | Input pin of data signals |
| 3 | D2 | Input pin of data signals |
| 4 | D3 | Input pin of data signals |
| 5 | D4 | Input pin of data signals |
| 6 | D5 | Input pin of data signals |
| 7 | D6 | Input pin of data signals |
| 8 | D7 | Input pin of data signals |
| 9 | D8 | Input pin of data signals |
| 10 | CLK | Input pin of clock signals |
| 11 | GND | Ground pin |
| 12 | Y8 | Output pin |
| 13 | Y7 | Output pin |
| 14 | Y6 | Output pin |
| 15 | Y5 | Output pin |
| 16 | Y4 | Output pin |
| 17 | Y3 | Output pin |
| 18 | Y2 | Output pin |
| 19 | Y1 | Output pin |
| 20 | VDD | Power supply pin |

Block Diagram



Basic circuit may be omitted partially or simplified for explanatory purpose.

Function Table

| INPUT | | | OUTPUT: Y |
|-------|-----|---|-----------|
| /CLR | CLK | D | |
| L | X | X | Z (OFF) |
| H | ↑ | L | Z (OFF) |
| H | ↑ | H | H (ON) |
| H | L | X | Y0 |
| H | ↓ | X | Y0 |

↑: Change from "L" to "H"

↓: Change from "H" to "L"

H: High level

Z: High impedance (OFF)

X: Don't care

Y0: Y level immediately before determining the input condition shown in the table

Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | Symbol | Rating | Unit |
|-------------------------------|------------------------|--------------|------|
| Power supply voltage | V _{DD} | 50 | V |
| Output current (per ch) | I _{OUT} | -500 | mA |
| Input voltage | V _{IN} | -0.5 to 6 | V |
| Clamp diode withstand voltage | V _R | 50 | V |
| Clamp diode forward current | I _F | 500 | mA |
| Power dissipation | P _D (Note1) | 1.76 (Note2) | W |
| Operating temperature | T _{opr} | -40 to 85 | °C |
| Storage temperature | T _{stg} | -55 to 150 | °C |

Note1: On PCB (size: 50 mm × 50 mm × 1.6 mm, Cu area: 40 %, single-side glass epoxy)

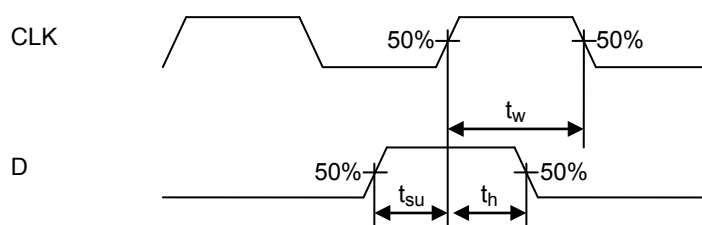
Note2: When Ta exceeds 25 °C, it is necessary to do the derating with 14.1 mW/°C.

Operating Ranges (Ta = -40 to 85°C, unless otherwise specified)

| Characteristics | Symbol | Test conditions | Min | Typ. | Max | Unit |
|-----------------------------------|-----------------------|--|-----|------|------|------|
| Power supply voltage | V _{DD} | — | 4.5 | — | 50 | V |
| Output current (per ch) (Note) | I _{OUT} | 1 circuit ON, Ta = 25 °C | 0 | — | -400 | mA |
| | | t _{pw} = 25 ms 8 circuits ON Ta = 85 °C T _j = 120 °C Duty = 10 % | 0 | — | -400 | |
| | | Duty = 50 % | 0 | — | -195 | |
| Clamp diode forward current | I _F | — | — | — | 400 | mA |
| Input voltage (Output on) | V _{IN (ON)} | CLK pin, /CLR pin, and D1 to D8 pin | 2.0 | — | 5.5 | V |
| Input voltage (Output off) | V _{IN (OFF)} | CLK pin, /CLR pin, and D1 to D8 pin | 0 | — | 0.8 | V |
| Setup time | t _{su} | D setup time to CLK input | 15 | — | — | ns |
| Hold time | t _h | D hold time to CLK input | 15 | — | — | ns |
| Pulse width of CLK and /CLR | t _w | CLK pin and /CLR pin | 100 | — | — | ns |
| Clock frequency | f _{CLK} | CLK pin | — | — | 5 | MHz |

Note: Stand alone

Timing chart

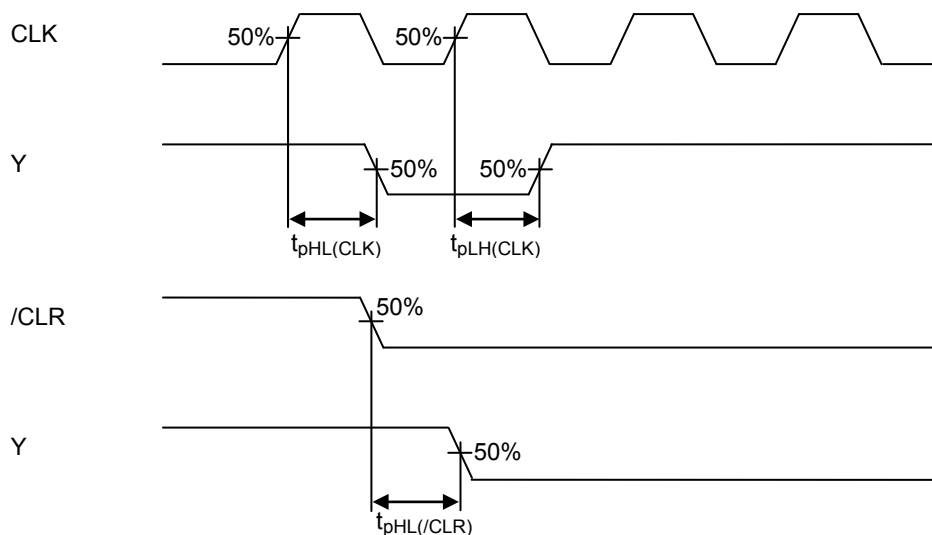


Timing charts may be omitted partially or simplified for explanatory purposes.

Electrical Characteristics (Ta = 25°C, unless otherwise specified)

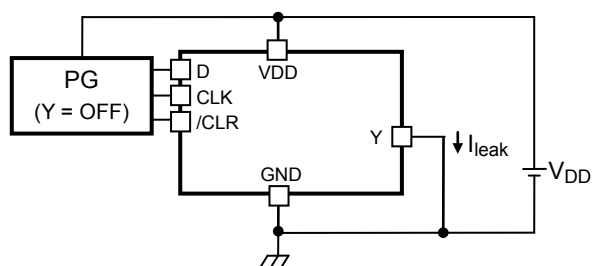
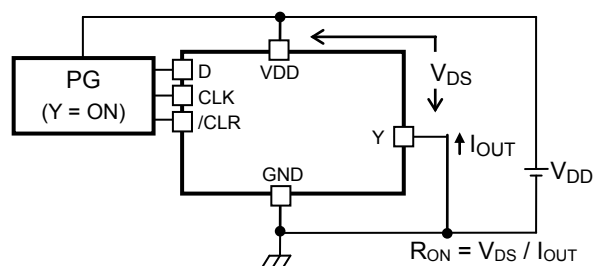
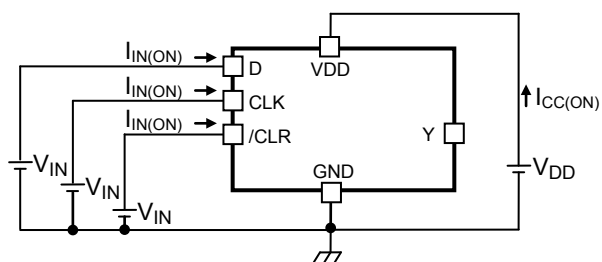
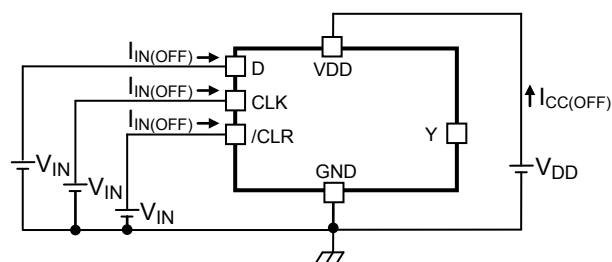
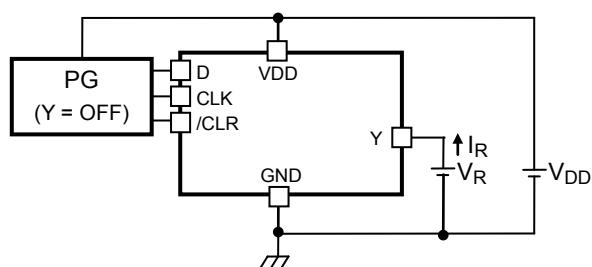
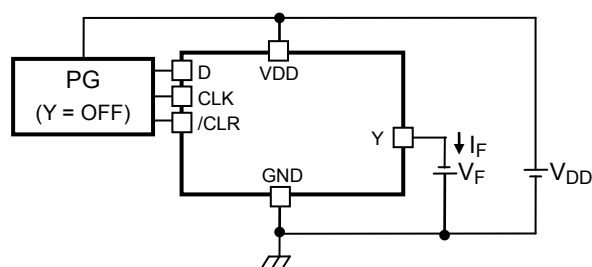
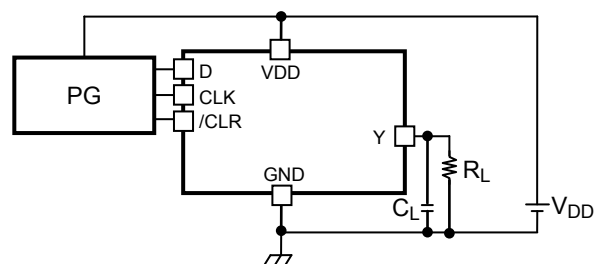
| Characteristics | Symbol | Test Circuit | Test conditions | Min | Typ. | Max | Unit |
|--|--------------------------|--------------|--|-----|---------------|-----------------|-------------------|
| Output leakage current | I_{leak} | 1 | $V_{DD} = 50\text{ V}$, $T_a = 85^\circ\text{C}$ At output OFF | — | — | 1.0 | μA |
| Output voltage (Output ON-resistance) | V_{DS} (R_{ON}) | 2 | $I_{OUT} = -350\text{ mA}$ $V_{DD} = 10\text{ V}$ | — | 0.49 (1.4) | 1.14 (3.25) | V (Ω) |
| | | | $I_{OUT} = -200\text{ mA}$ $V_{DD} = 10\text{ V}$ | — | 0.28 (1.4) | 0.65 (3.25) | |
| | | | $I_{OUT} = -100\text{ mA}$ $V_{DD} = 10\text{ V}$ | — | 0.14 (1.4) | 0.325 (3.25) | |
| Input current (Output ON) | $I_{IN(ON)}$ | 3 | $V_{IN} = 5.5\text{ V}$, $V_{DD} = 50\text{ V}$ | — | — | 100 | μA |
| Input current (Output OFF) | $I_{IN(OFF)}$ | 4 | $V_{IN} = 0\text{ V}$, $V_{DD} = 50\text{ V}$ | — | — | 1 | μA |
| Power supply current | $I_{CC(ON)}$ | 3 | $V_{DD}=50\text{ V}$, Output ON | — | 24 | 40 | mA |
| | $I_{CC(OFF)}$ | 4 | $V_{DD}=50\text{ V}$, Output OFF | — | 24 | 40 | mA |
| Clamp diode leakage current | I_R | 5 | $V_R = 50\text{ V}$, $T_a = 85^\circ\text{C}$ | — | — | 1.0 | μA |
| Clamp diode forward voltage | V_F | 6 | $I_F = 350\text{ mA}$ | — | — | 2.0 | V |
| Propagation delay time | t_{pHL} (CLK) | 7 | CLK (50%) to Y (50%) Y changes from H to L. $C_L=15\text{ pF}$, $R_L=25\Omega$ $V_{DD} = 10\text{ V}$ | — | 120 | 200 | ns |
| | t_{pLH} (CLK) | 7 | CLK (50%) to Y (50%) Y changes from L to H. $C_L=15\text{ pF}$, $R_L=25\Omega$ $V_{DD} = 10\text{ V}$ | — | 120 | 200 | ns |
| | t_{pHL} (/CLR) | 7 | /CLR (50%) to Y (50%) Y changes from H to L. $C_L=15\text{ pF}$, $R_L=25\Omega$ $V_{DD} = 10\text{ V}$ | — | 120 | 200 | ns |

Timing chart



Timing charts may be omitted partially or simplified for explanatory purposes.

Test Circuit

1. I_{leak} 2. $V_{DS} (R_{ON})$ 3. $I_{IN} (ON)$ and $I_{CC} (ON)$ 4. $I_{IN} (OFF)$ and $I_{CC} (OFF)$ 5. I_R 6. V_F 7. $t_{pHL} (CLK)$, $t_{pLH} (CLK)$, $t_{pHL} (/CLR)$ 

Test circuits may be omitted partially or simplified for explanatory purpose.

Precautions for Using

This IC does not incorporate protection circuits for over current and over voltage.

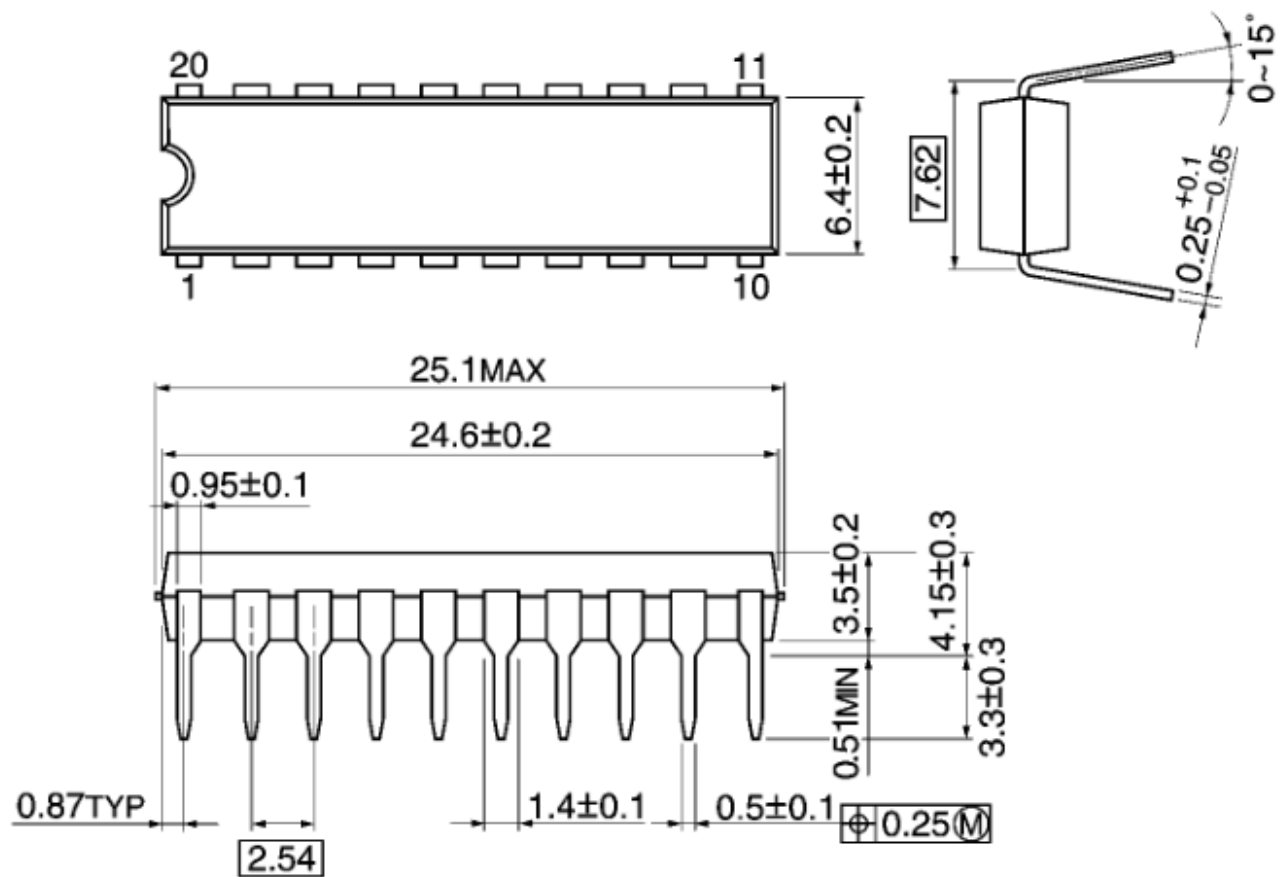
Therefore, if the short-circuit between adjacent pins or between outputs, the short-to-power or ground fault has occurred, the current or voltage beyond the absolute maximum rating is impressed, and IC may be destroyed. When designing, please consider enough in power supply line, output line, and GND line.

In addition, so as not to continue to flow a current that exceeds the absolute maximum rating of the IC, please insert the appropriate fuse in the power supply line.

Package Dimensions

DIP20-P-300-2.54A

Unit: mm



Weight: 1.4 g (typ.)

Notes on Contents

1. Block diagram

Block diagram may be simplified for explanatory purpose.

2. Test Circuit

Test circuit may be simplified for explanatory purpose.

3. Timing Chart

Timing charts may be simplified for explanatory purposes.

IC Usage Considerations

Notes on handling of ICs

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
- (2) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. In addition, do not use any device inserted in the wrong orientation or incorrectly to which current is applied even just once.
- (3) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of overcurrent and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (4) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator. If there is a large amount of leakage current such as from input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure may cause smoke or ignition. (The overcurrent may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

Heat Radiation Design

When using an IC with large current flow such as power amp, regulator or driver, design the device so that heat is appropriately radiated, in order not to exceed the specified junction temperature (T_j) at any time or under any condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, when designing the device, take into consideration the effect of IC heat radiation with peripheral components.

Back-EMF

When a motor rotates in the reverse direction, stops or slows abruptly, current flows back to the motor's power supply owing to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond the absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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