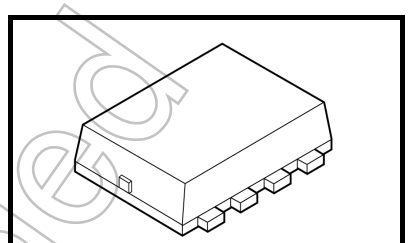
TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB7107FN

Buck DC-DC Converter IC

The TB7107FN is a single-chip buck DC-DC converter IC utilizing a chopper circuit. The TB7107FN adopts bootstrap system and contains high-speed and low-on-resistance N-channel MOSFETs for the high side main switch to achieve high efficiency.



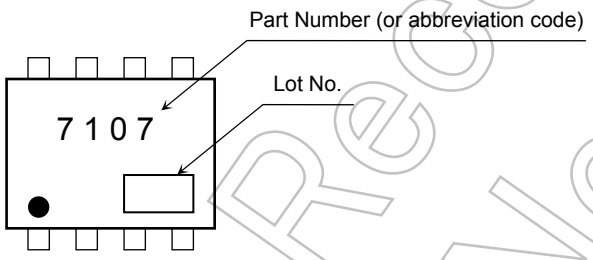
SON8-P-0303-0.65A

Weight: 0.017 g (typ.)

Features

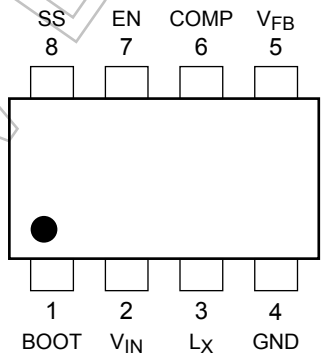
- Enables up to 2 A of load current (I_{OUT}) with a minimum of external components.
- High efficiency: η = 87% (typ.) (@V_{IN} = 12 V, V_{OUT} = 3.3 V and I_{OUT} = 0.7A)
- Operating voltage range: V_{IN} = 4.5 V to 20 V
- Low ON-resistance: $R_{DS\ (ON)}$ = 0.2 Ω (high-side) typical (@V_{IN} = 12 V, Tj = 25°C)
- Oscillation frequency: f_{OSC} = 380 kHz (typ.)
- Reference voltage: V_{FB} = 0.8 V ±2.25%(@ T_j = 25 ℃)
- Because of an external phase compensation element, the optimal phase compensation according to the output filter capacitor can be realized.
- Allows the use of a small surface-mount ceramic capacitor as an output filter capacitor.
- Housed in a small surface-mount package (PS-8) with low thermal resistance.
- Soft-start time adjustable by an external capacitor

Part Marking

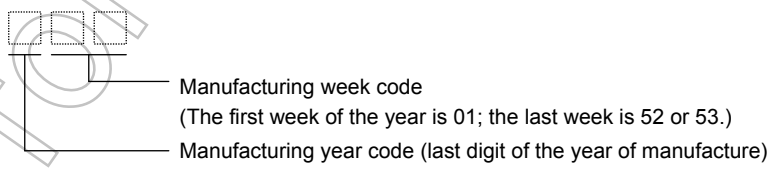


The dot (•) on the top surface indicates pin 1.

Pin Assignment



*: The lot number consists of three digits. The first digit represents the last digit of the year of manufacture, and the following two digits indicates the week of manufacture between 01 and either 52 or 53.



This product has a MOS structure and is sensitive to electrostatic discharge. Handle with care.

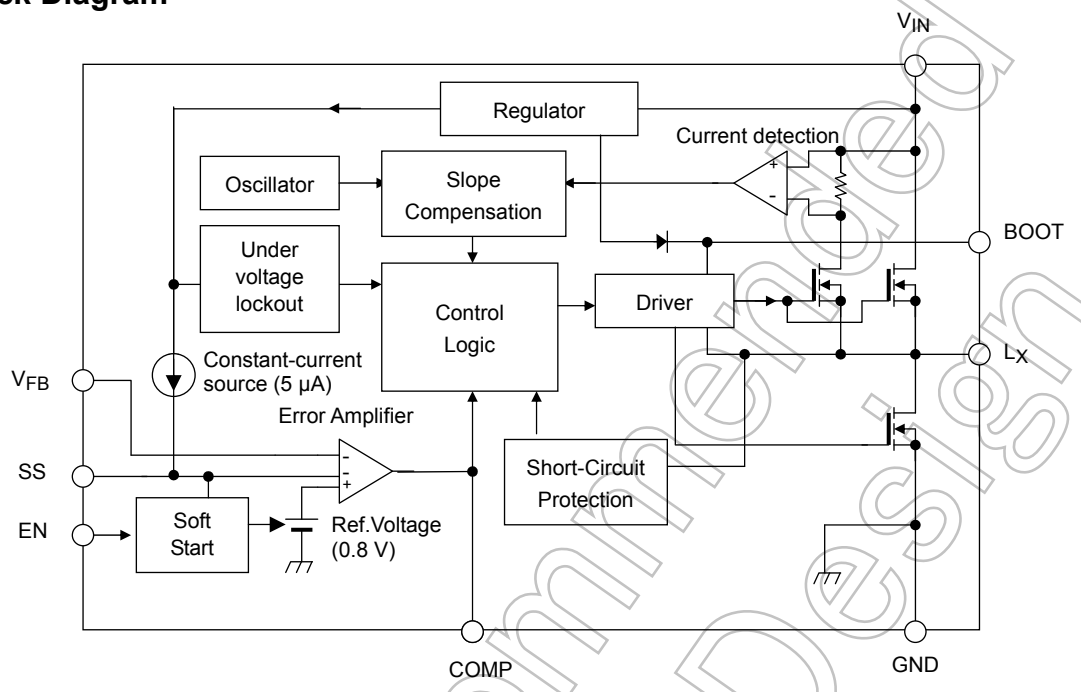
The product(s) in this document ("Product") contain functions intended to protect the Product from temporary small overloads such as minor short-term overcurrent, or overheating. The protective functions do not necessarily protect Product under all circumstances. When incorporating Product into your system, please design the system to avoid such overloads upon the Product, and to shut down or otherwise relieve the Product of such overload conditions immediately upon occurrence. For details, please refer to the notes appearing below in this document and other documents referenced in this document.

Start of commercial production
2009-10

Ordering Information

Part Number	Shipping
TB7107FN (TE85L, F)	Embossed tape (3000 units per reel)

Block Diagram



Pin Description

Pin No.	Symbol	Description
1	BOOT	Bootstrap pin This pin is connected to Bootstrap capacitor. A 0.1 μF bootstrap capacitor is required between BOOT pin and L_X pin.
2	V_{IN}	Input pin This pin is placed in the standby state if EN = low. Standby current is 60 μA (@V_{IN}=12V) or less.
3	L_X	Switch pin This pin is connected to high-side N-channel MOSFET.
4	GND	Ground pin
5	V_{FB}	Feedback pin This input is fed into an internal error amplifier with a reference voltage of 0.8 V (typ.).
6	COMP	Phase compensation pin Pin for connecting an error amplifier phase compensation resistor and capacitor.
7	EN	Enable pin When $V_{EN} \geq 1.8$ V (@ V_{IN} = 12 V), the internal circuitry is allowed to operate and thus enable the switching operation of the output section. When $V_{EN} \leq 0.5$ V (@ V_{IN} =12 V), the internal circuitry is disabled, putting the TB7107FN in Standby mode. This pin has an internal pull-up current of 15 μA(typ.).
8	SS	Soft-start pin The soft-start time can be adjusted with an external capacitor. The external capacitor is charged from a 5 μA (typ.) constant-current source, and the reference voltage of the error amplifier is regulated between 0 V and 0.8 V. The external capacitor is discharged when EN = low and in case of undervoltage lockout or thermal shutdown.

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Input pin voltage	V_{IN}	-0.3 to 25	V
Bootstrap pin voltage	V_{BOOT}	-0.3 to 28	V
Bootstrap pin - Switch pin voltage	V_{BOOT} -V_{LX}	-0.3 to 6	V
Switch pin voltage (Note 1)	V_{LX}	-0.3 to 25	V
Feedback pin voltage	V_{FB}	-0.3 to 6	V
Enable pin voltage	V_{EN}	-0.3 to 25	V
Soft-start pin voltage	V_{SS}	-0.3 to 6	V
Phase compensation pin voltage	V_{COMP}	-0.3 to 6	V
Switch pin current	I_{LX}	-2.3	A
Power dissipation (Note 2)	P_D	0.9	W
Operating junction temperature	T_{jopr}	-40 to 125	°C
Junction temperature (Note 3)	T_j	150	°C
Storage temperature	T_{stg}	-55 to 150	°C

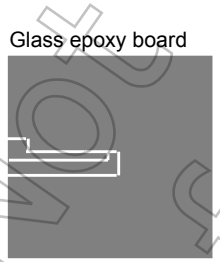
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc)

Note 1: The switch pin voltage (V_{LX}) doesn’t include the peak voltage generated by TB7107FN’s switching.

Thermal Resistance Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, junction to ambient	$R_{th\ (j\text{-}a)}$	110.2 (Note 2)	°C/W

Note 2:



Note 3: The TB7107FN may go into thermal shutdown at the rated maximum junction temperature. Thermal design is required to ensure that the rated maximum operating junction temperature, T_{jopr}, will not be exceeded.

Electrical Characteristics (Tj = 25°C, V_{IN} = 4.5 to 20 V, unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Operating input voltage		$V_{IN(OPR)}$	—	4.5	—	20	V
Operating current		I_{IN}	V_{IN} = 12V ,V_{EN} = 5V ,V_{FB} = 2 V	—	1.8	2.5	mA
Output voltage range		$V_{OUT(OPR)}$	V_{EN} = V_{IN}	0.8	—	V_{IN} -2	V
Standby current		$I_{IN(STBY)}$	V_{IN} = 12 V , V_{EN} = 0 V V_{FB} = 0.8 V	—	—	60	μA
High-side switch leakage current		$I_{LEAK(H)}$	V_{IN} = 12 V, V_{EN} = 0 V V_{FB} = 0.8 V , V_{LX} = 0 V	—	—	10	μA
EN threshold voltage		$V_{IH(EN)}$	V_{IN} = 12 V	1.8	—	—	V
		$V_{IL(EN)}$	V_{IN} = 12V	—	—	0.5	
EN input current		$I_{IH(EN)}$	V_{IN} = 12V, V_{EN} = 5 V	-5	—	5	μA
		$I_{IL(EN)}$	V_{IN} = 12V, V_{EN} = 0 V	—	-15	—	
V_{FB} input voltage		V_{FB}	V_{IN} = 12 V , V_{EN} = 5 V	0.782	0.8	0.818	V
V_{FB} input current		I_{FB}	V_{IN} = 12 V , V_{EN} = 5 V V_{FB} = 2V	-1	—	1	μA
Phase compensation input current		$I_{COMP(H)}$	V_{IN} = 12 V , V_{EN} = 5 V V_{FB} = 0.7V , V_{COMP} = 0.5 V	—	-40	—	μA
		$I_{COMP(L)}$	V_{IN} = 12 V , V_{EN} = 5 V V_{FB} = 0.9V , V_{COMP} = 0.5 V	—	40	—	
High-side switch on-state resistance		$R_{DS(ON)(H)}$	V_{IN} = 12V , V_{EN} = 5V I_{LX} = - 1A	—	0.2	—	Ω
Low-side switch on-state resistance		$R_{DS(ON)(L)}$	V_{IN} = 12 V , V_{EN} =5 V I_{LX} = 100 mA	—	1.5	—	Ω
Oscillation frequency		f_{OSC}	V_{IN} = 12V , V_{EN}= 5V	300	380	460	kHz
Internal soft-start time		t_{SS}	V_{IN} = 12 V , V_{EN}= 5V , I_{OUT} = 0A Measured between 0% and 90%points at V_{OUT}	0.5	1	2	ms
External soft-start charge current		I_{SS}	V_{IN} = 12 V , V_{EN} = 5 V	-3	-5	-8	μA
High-side switch duty cycle		Dmax	V_{IN} = 12 V , V_{EN} = 5 V	—	88	—	%
Thermal shutdown (TSD)	Detection temperature	T_{SD}	V_{IN} = 12 V , V_{EN} = 5 V	—	160	—	°C
	Hysteresis	ΔT_{SD}	V_{IN} = 12 V , V_{EN} = 5 V	—	15	—	
Undervoltage lockout (UVLO)	Detection voltage	V_{UV}	V_{EN} = V_{IN}	2.9	3.2	3.5	V
	Recovery voltage	V_{UVR}	V_{EN} = V_{IN}	3.2	3.5	3.8	
	Hysteresis	ΔV_{UV}	V_{EN} = V_{IN}	—	0.3	—	
L_X current limit		I_{LIM}	V_{IN} = 4.5V to 20 V , V_{EN}= 5V V_{OUT} = 2 V	2.9	3.5	—	A

Note on Electrical Characteristics

The test condition T_j = 25°C means a state where any drifts in electrical characteristics incurred by an increase in the chip's junction temperature can be ignored during pulse testing.

Application Circuit Example

Figure 1 shows a typical application circuit using a low-ESR electrolytic or ceramic capacitor for C_{OUT}.

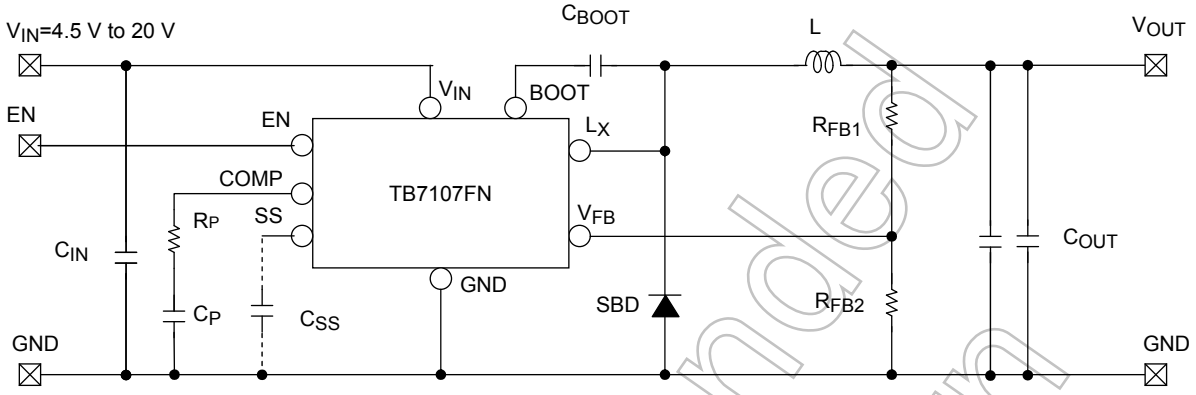


Figure 1 TB7107FN Application Circuit Example

Component values (reference value@ V_{IN} = 12 V, V_{OUT} = 3.3 V, Ta = 25°C)

C_{IN}: Input filter capacitor = 10 μF
(ceramic capacitor: GRM31CR71E106K manufactured by Murata Manufacturing Co., Ltd.)

C_{OUT}: Output filter capacitor = 10 μF
(ceramic capacitor: GRM31CR71E106K manufactured by Murata Manufacturing Co., Ltd.)

R_{FB1}: Output voltage setting resistor = 7.5 kΩ

R_{FB2}: Output voltage setting resistor = 2.4 kΩ

C_P: Phase compensation capacitance

R_P: Phase compensation resistance

L: Inductor = 10 μH (SLF10165T-100M3R83PF or SLF7055T-100M2R5-3PF manufactured by TDK-EPC Corporation)

SBD: Schottky barrier diode CRS30I30A (manufactured by Toshiba Corporation)

C_{BOOT}: Bootstrap capacitor = 0.1 μF (GRM188R71H104J manufactured by Murata Manufacturing Co., Ltd.)

C_{SS} is a capacitor for adjusting the soft-start time.

Examples of Component Values (For Reference Only)

Output Voltage Setting V_{OUT}	Inductance L	Input Capacitance C_{IN}	Output Capacitance C_{OUT}	Feedback Resistor R_{FB1}	Feedback Resistor R_{FB2}	Phase Compensation Capacitance C_P	Phase Compensation Resistance R_P
1.2 V	10 μH	10 μF	20 μF	7.5 kΩ	15 kΩ	4700 pF	10 kΩ
1.51 V	10 μH	10 μF	20 μF	16 kΩ	18 kΩ	4700 pF	10 kΩ
1.8 V	10 μH	10 μF	20 μF	15 kΩ	12 kΩ	2200 pF	15 kΩ
2.5 V	10 μH	10 μF	20 μF	5.1 kΩ	2.4 kΩ	2200 pF	22 kΩ
3.3 V	10 μH	10 μF	20 μF	7.5 kΩ	2.4 kΩ	2200 pF	22 kΩ
5.0V	10 μH	10 μF	20 μF	27 kΩ	5.1 kΩ	2200 pF	33 kΩ

Component values need to be adjusted, depending on the TB7107FN's I/O conditions and the board layout.

Application Notes

Inductor Selection

The inductance required for inductor L can be calculated as follows:

$$L = \frac{V_{IN} - V_{OUT}}{f_{OSC} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}} \quad \cdots\cdots\cdots\cdots(1)$$

V_{IN}: Input voltage (V)
V_{OUT}: Output voltage (V)
f_{OSC}: Oscillation frequency = 380 kHz (typ.)
ΔI_L: Inductor ripple current (A)

*: Generally, ΔI_L should be set to approximately 30% of the maximum output current. Since the maximum output current of the TB7107FN is 2.0 A, ΔI_L should be 0.6 A or so. The inductor should have a current rating greater than the peak output current of 2.3 A. If the inductor current rating is exceeded, the inductor becomes saturated, leading to an unstable DC-DC converter operation.

When V_{IN} = 12 V and V_{OUT} = 3.3 V, the required inductance can be calculated as follows. Be sure to select an appropriate inductor, taking the input voltage range into account.

$$L = \frac{V_{IN} - V_{OUT}}{f_{OSC} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$
$$= \frac{12\ V - 3.3\ V}{380kHz \cdot 0.6A} \cdot \frac{3.3\ V}{12\ V}$$
$$= 10.5\ \mu H \quad \cdots\cdots\cdots\cdots(2)$$

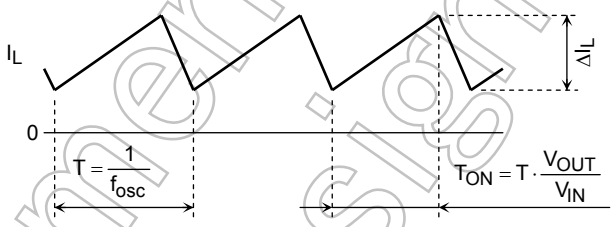


Figure 2 Inductor Current Waveform

Setting the Output Voltage

A resistive voltage divider is connected as shown in Figure 3 to set the output voltage; it is given by Equation 3 based on the reference voltage of the error amplifier (0.8 V typ.), which is connected to the Feedback pin, V_{FB}. R_{FB1} should be up to 30 kΩ or so, because an extremely large-value R_{FB1} incurs a delay due to parasitic capacitance at the V_{FB} pin. It is recommended that resistors with a precision of ±1% or higher be used for R_{FB1} and R_{FB2}.

$$V_{OUT} = V_{FB} \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$
$$= 0.8\ V \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \quad \cdots\cdots(3)$$

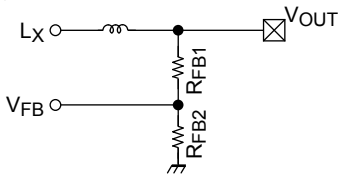


Figure 3 Output Voltage Setting Resistors

Setting the Phase Compensation Circuit

Connect a resister (R_P) in series with a capacitor (C_P) to COMP pin as a phase compensation. The following calculated value provides an estimation of the constant of phase compensation.

$$F0 = \frac{1}{2\pi} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot Gm(EA)Rp \cdot \frac{Gm(IS)}{C_{OUT}}$$

$$Fz = \frac{1}{2\pi} \cdot \frac{1}{Cp \cdot Rp} \quad \cdots\cdots(4)$$

F0=Frequency in loop gain being 0dB
: Set approximately to one-tenth of the switching frequency
Fz=Frequency of pole-zero
: Set approximately to one-tenth of the F0
Design value (reference):
Gm(EA)=Error Amp Gm : 200(μS)
Gm(IS)=Current detection circuit Gm : 4(S)

The optimum value of phase compensation may change with the characteristics of C_{OUT} and another. Carry out sufficient evaluation on an actual operating condition.

Output Filter Capacitor Selection

Use a low-ESR electrolytic or ceramic capacitor as the output filter capacitor. Since a capacitor is generally sensitive to temperature, choose one with excellent temperature characteristics. The large capacitance improves load response characteristics. As a rule of thumb, its capacitance should be 10 μF or greater for applications. The capacitance should be set to an optimal value that meets the system's ripple voltage requirement and transient load response characteristics. Since the ceramic capacitor has a very low ESR value, it helps reduce the output ripple voltage; however, because the ceramic capacitor provides less phase margin, it should be thoroughly evaluated.

Rectifier Selection

A Schottky barrier diode should be externally connected to the TB7107FN as a rectifier between the L_X and GND pins. It is recommended that either CRS30I30A, be used as the Schottky barrier diode. If a large voltage overshoot is on the L_X pin, it reduces the voltage to connect a series CR network consisting of a resistor of R_S = 4.7 Ω and a capacitor of C_S = 470 pF with the Schottky barrier diode in parallel. Power loss of the Schottky barrier diode tends to increase due to an increased reverse current caused by the rise in ambient temperature and self-heating due to a supplied current. The rated current should therefore be derated to allow for such conditions in selecting an appropriate diode.

Soft-Start Feature

The TB7107FN has a soft-start feature.

If the SS pin is left open, the soft-start time, t_{SS}, for V_{OUT} defaults to 1 ms (typ.) internally.

The soft-start time can be extended by adding an external capacitor (C_{SS}) between the SS and GND pins. The soft-start time can be calculated as follows:

$$t_{SS2} = 0.16 \cdot C_{SS} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (5)$$

t_{SS2}: Soft-start time (in seconds) when an external capacitor is connected between SS and GND.

C_{SS}: Capacitor value (μF)

The soft-start feature is activated when the TB7107FN exits the undervoltage lockout (UVLO) state after power-up and when the voltage at the EN pin has changed from logic low to logic high.

Overcurrent Protection（OCP）

The TB7107FN has built-in overcurrent protection with pulse skip. When the peak current of L_X pin exceeds I_{LIM}=3.5A(typ.), the ON time of the high-side switch(internal) will be limited. Switching frequency will be reduced and output current will be restricted further if output voltage falls and the voltage of V_{FB} pin drops below the overcurrent pulse skip detection voltage V_{LOC} (0.3V typ.) during overcurrent protection .

Undervoltage Lockout (UVLO)

The TB7107FN has undervoltage lockout (UVLO) protection circuitry. The TB7107FN does not provide output voltage (V_{OUT}) until the input voltage has reached V_{UVR} (3.5 V typ.). UVLO has hysteresis of 0.3 V (typ.). After the switch turns on, if V_{IN} drops below V_{UV} (3.2 V typ.), UVLO shuts off the switch at V_{OUT}.

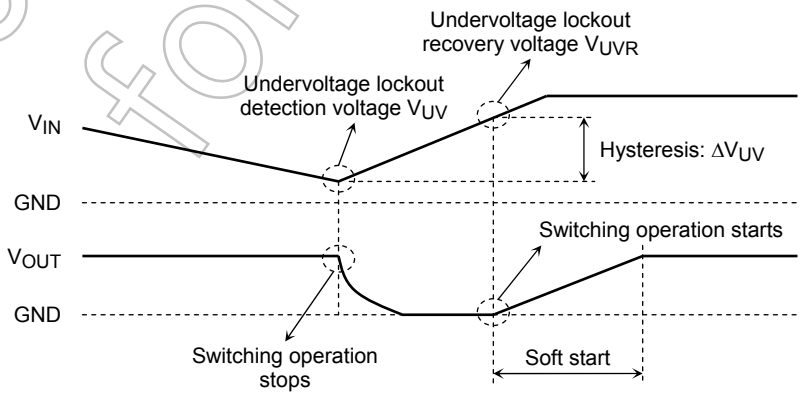


Figure 4 Undervoltage Lockout Operation

Thermal Shutdown (TSD)

The TB7107FN provides thermal shutdown. When the junction temperature continues to rise and reaches T_{SD} (160°C typ.), the TB7107FN goes into thermal shutdown and shuts off the power supply. TSD has a hysteresis of about 15°C (typ.). The device is enabled again when the junction temperature has dropped by approximately 15°C from the TSD trip point. The device resumes the power supply when the soft-start circuit is activated upon recovery from TSD state.

Thermal shutdown is intended to protect the device against abnormal system conditions. It should be ensured that the TSD circuit will not be activated during normal operation of the system.

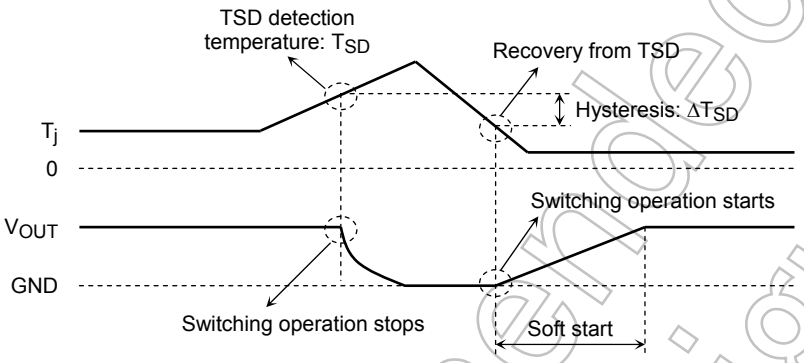


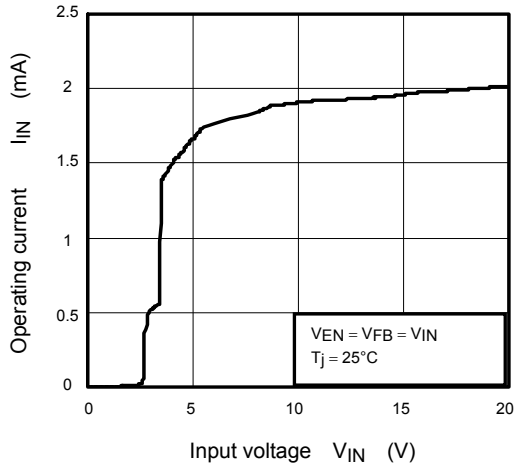
Figure 5 Thermal Shutdown Operation

Usage Precautions

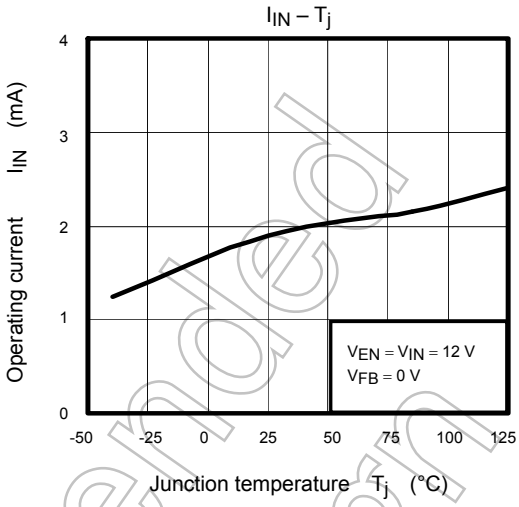
- The input voltage, output voltage, output current and temperature conditions should be considered when selecting capacitors, inductors and resistors. These components should be evaluated on an actual system prototype for best selection.
- External components such as capacitors, inductors and resistors should be placed as close to the TB7107FN as possible.
- C_{IN} should be connected as close to the GND and V_{IN1} pins as possible. Operation might become unstable due to board layout.
- The minimum programmable output voltage is 0.8 V (typ.). If the difference between the input and output voltages is small, the output voltage might not be regulated accurately and fluctuate significantly.
- GND pin is connected with the back of IC chip and serves as the heat radiation pin. Secure the area of a GND pattern as large as possible for greater of heat radiation.
- The overcurrent protection circuits in the Product are designed to temporarily protect Product from minor overcurrent of brief duration. When the overcurrent protective function in the Product activates, immediately cease application of overcurrent to Product. Improper usage of Product, such as application of current to Product exceeding the absolute maximum ratings, could cause the overcurrent protection circuit not to operate properly and/or damage Product permanently even before the protection circuit starts to operate.
- The thermal shutdown circuits in the Product are designed to temporarily protect Product from minor overheating of brief duration. When the overheating protective function in the Product activates, immediately correct the overheating situation. Improper usage of Product, such as the application of heat to Product exceeding the absolute maximum ratings, could cause the overheating protection circuit not to operate properly and/or damage Product permanently even before the protection circuit starts to operate.

Typical Performance Characteristics

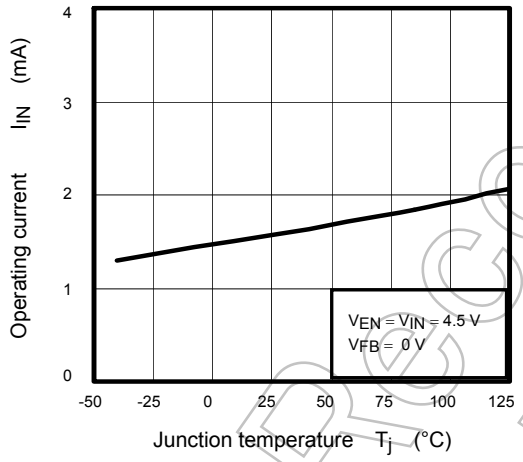
$I_{IN} – V_{IN}$



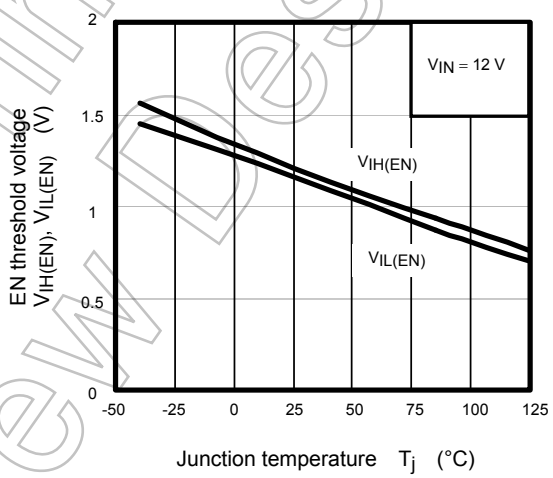
$I_{IN} – T_j$



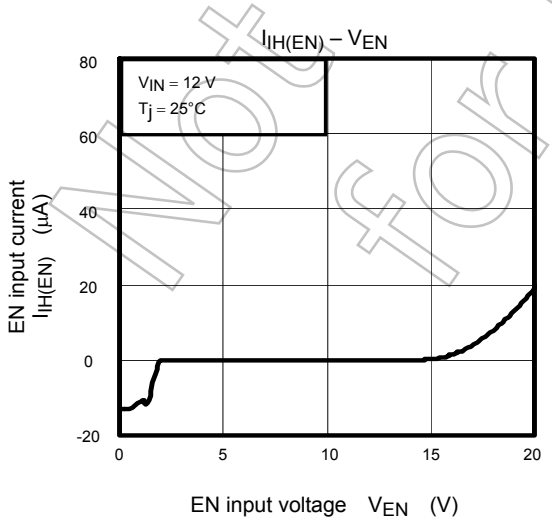
$I_{IN} – T_j$



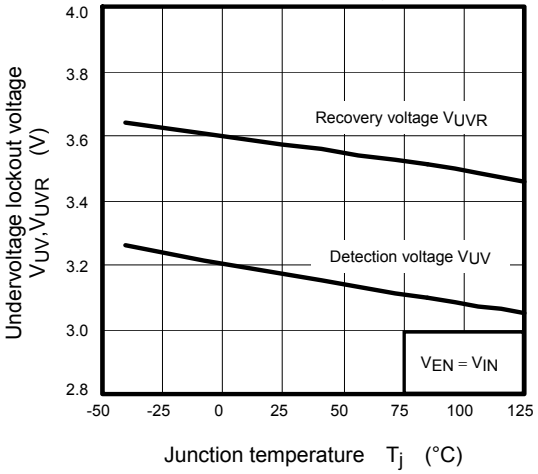
$V_{IH(EN)}, V_{IL(EN)} – T_j$



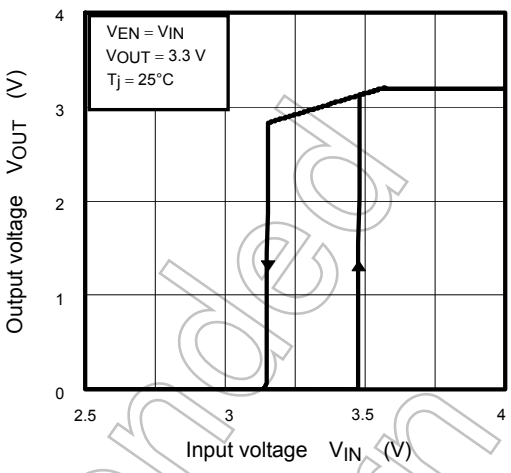
$I_{IH(EN)} – V_{EN}$



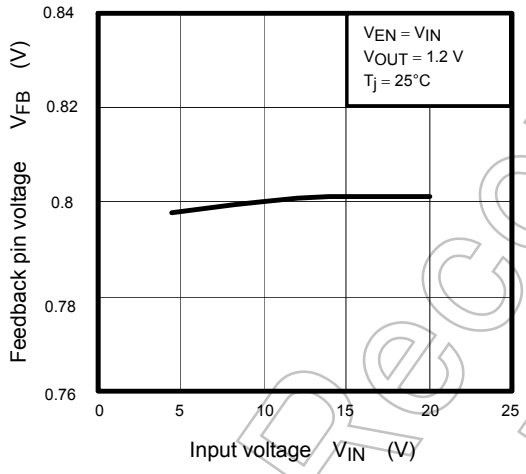
V_{UV}, V_{UVR} – T_j



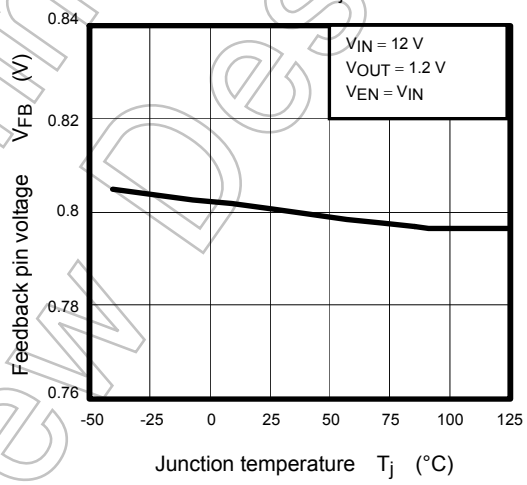
V_{OUT} – V_{IN}



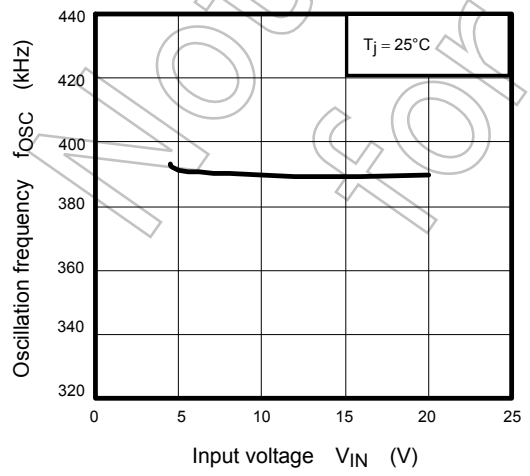
V_{FB} – V_{IN}



V_{FB} – T_j



f_{OSC} – V_{IN}



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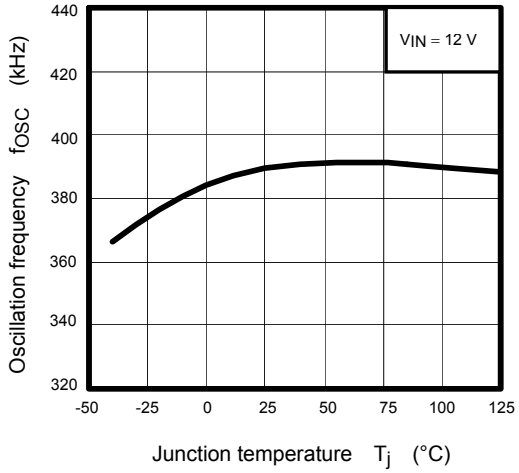
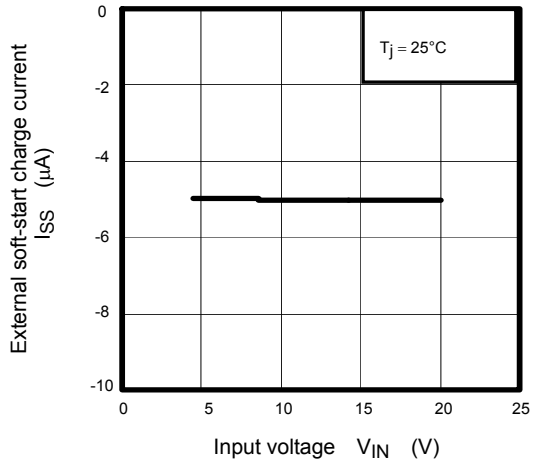
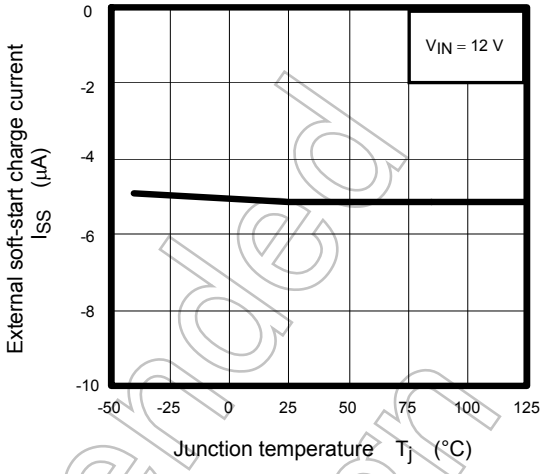


$I_{SS} - V_{IN}$



$I_{SS} - T_j$



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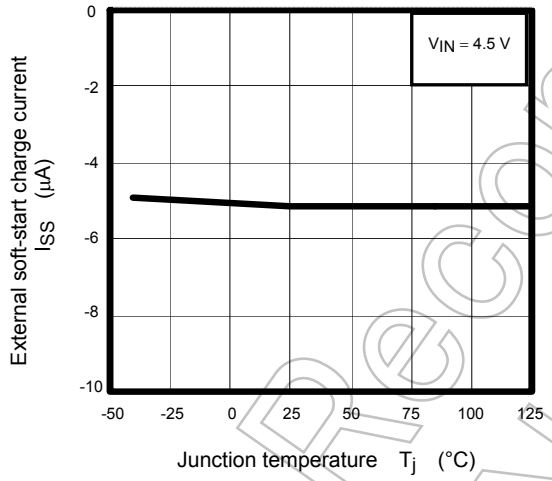
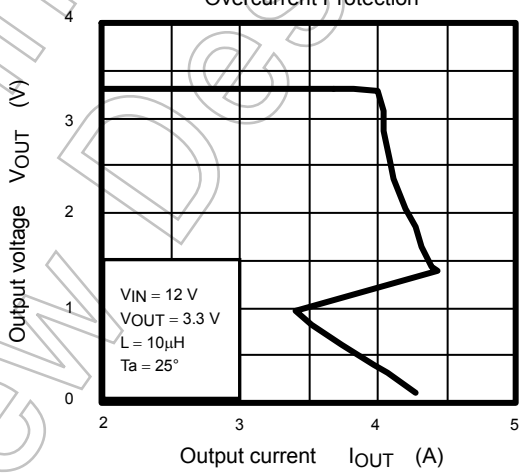
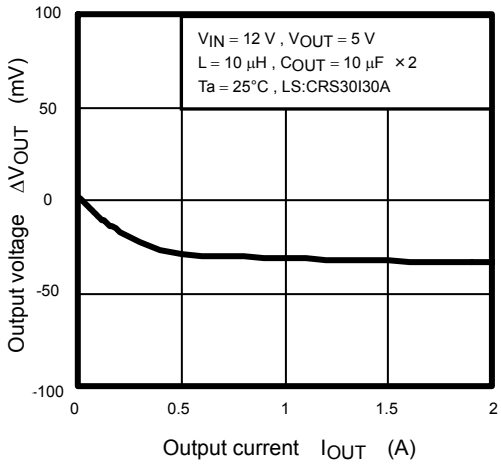


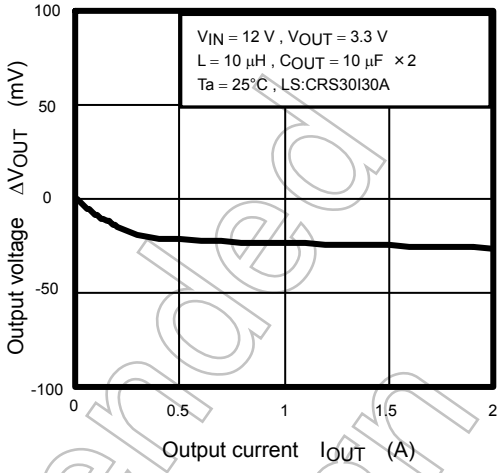
Overcurrent Protection



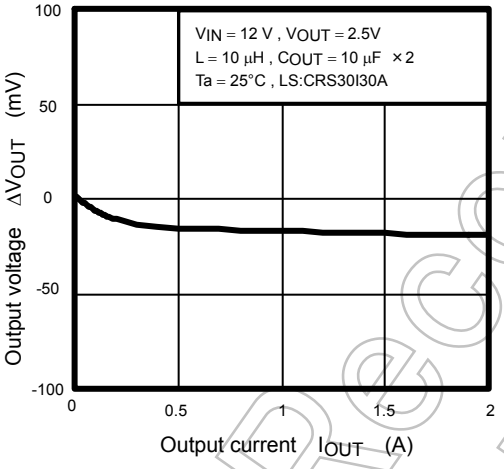
$\Delta V_{OUT} - I_{OUT}$



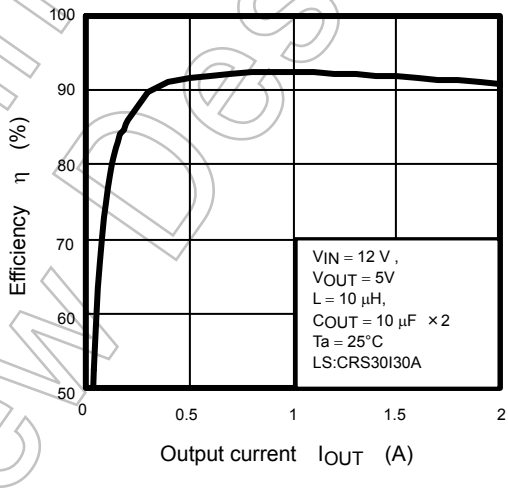
$\Delta V_{OUT} - I_{OUT}$



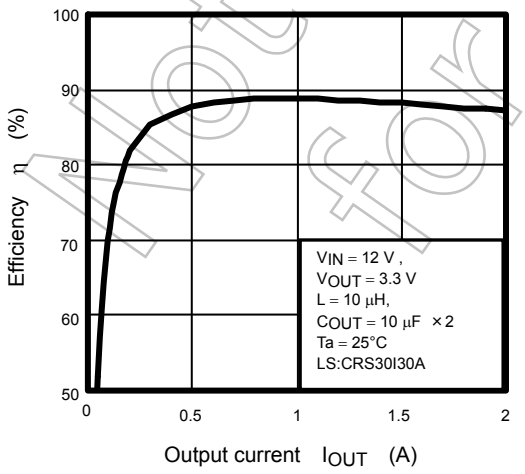
$\Delta V_{OUT} - I_{OUT}$



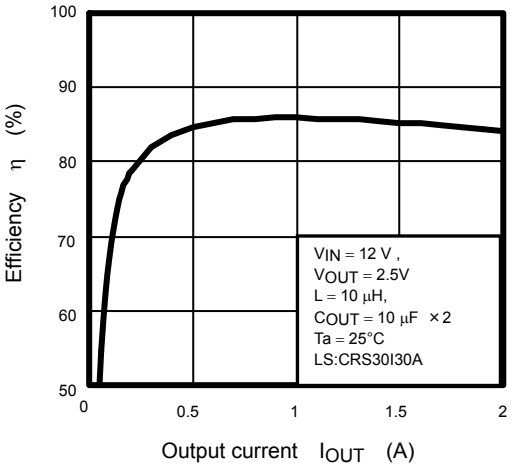
$\eta - I_{OUT}$



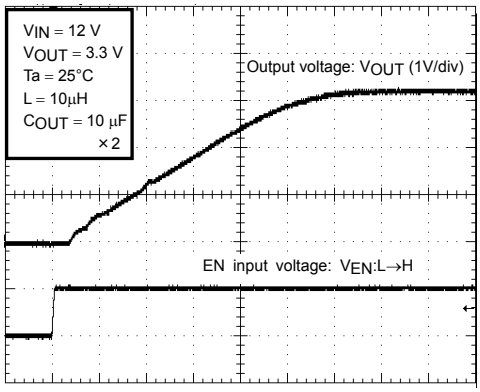
$\eta - I_{OUT}$



$\eta - I_{OUT}$

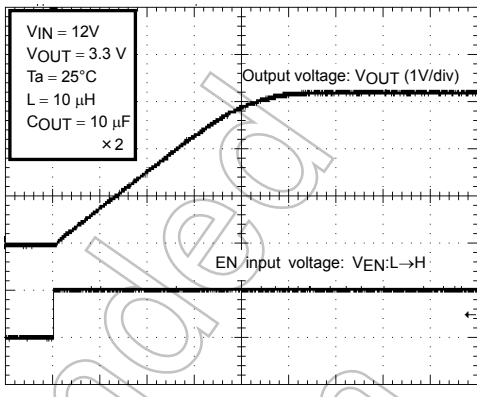


Startup Characteristics
(Internal Soft-Start Time)



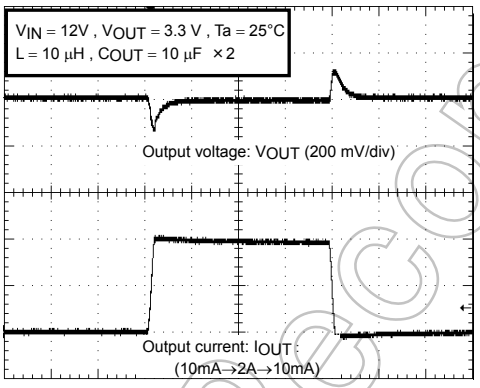
200 μs/div

Startup Characteristics
(C_{SS} = 0.1 μF)



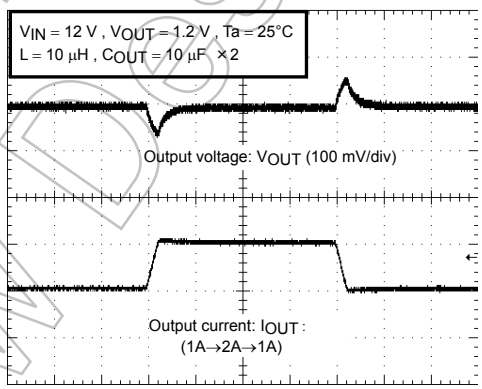
4 ms/div

Load Response Characteristics



200 μs/div

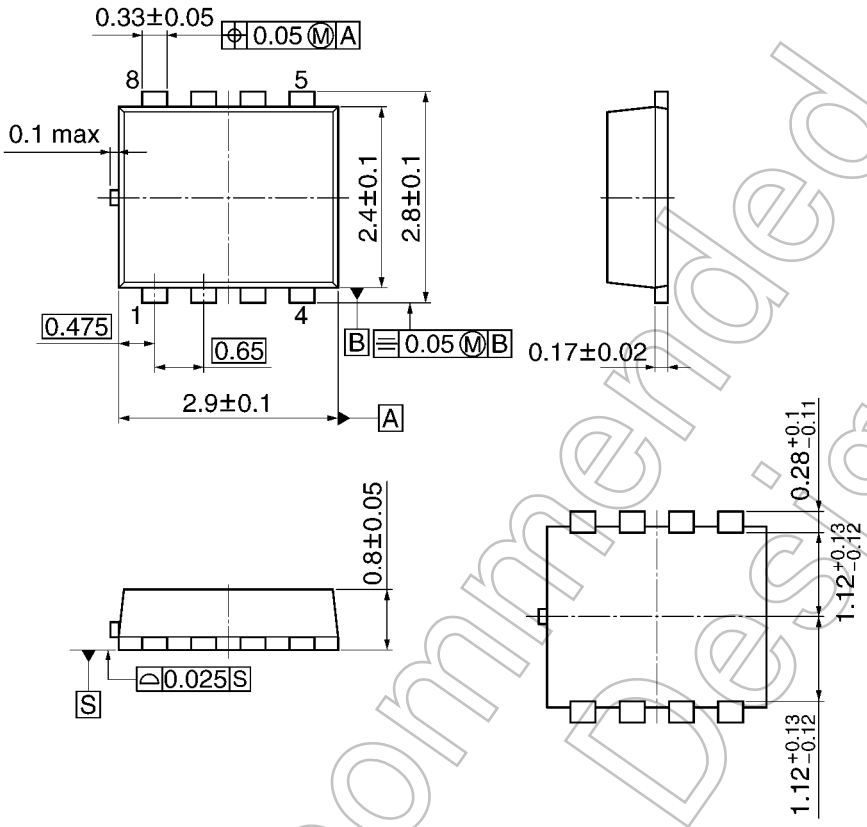
Load Response Characteristics



200 μs/div

Package Dimensions

SON8-P-0303-0.65A Unit: mm



Weight: 0.017 g (typ.)

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