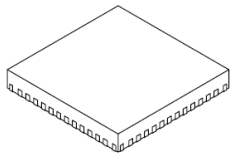
Toshiba BiCD process integrated circuit silicon monolithic

TB67S265FTG

8bit Serial controlled bipolar stepping motor driver

1. Description

The TB67S265FTG is a two phase bipolar stepping motor driver using a PWM chopper, controlled by 8-bit serial.
Fabricated by the BiCD process, the TB67S265FTG is rated at 50 V/2.0 A(Maximum current).
The internal voltage regulator allows to control the device with a single VM power supply.



P-WQFN48-0707-0.50-003

Weight: 0.10 g (Typ.)

2. Features

- BiCD process integrated monolithic IC.
- Capable of controlling one bipolar stepping motor.
- PWM controlled constant-current drive.
- Built-in serial-parallel convert circuit (8bit shift register)
- 3-line (Data, Clock, Latch) serial output function for cascade connection
- Allows full, half step operation
- 4 bit (16 steps) adjustable torque function (TRQ1,TRQ2,TRQ3,TRQ4).
- Low on-resistance MOSFET output stage.(Ron(D-S))
- High voltage and current (for specification, please refer to the absolute maximum ratings and operation ranges).
- Built-in error detection circuits (Thermal shutdown (TSD), over current shutdown (ISD), and power on reset(POR)).
- Built-in VCC regulator for internal use.
- Chopping frequency of a motor can be customized by external resistance and capacitor.
- Package type: P-WQFN48-0707-0.50-003

Note: Please be careful about thermal conditions during use.

3. Pin assignment

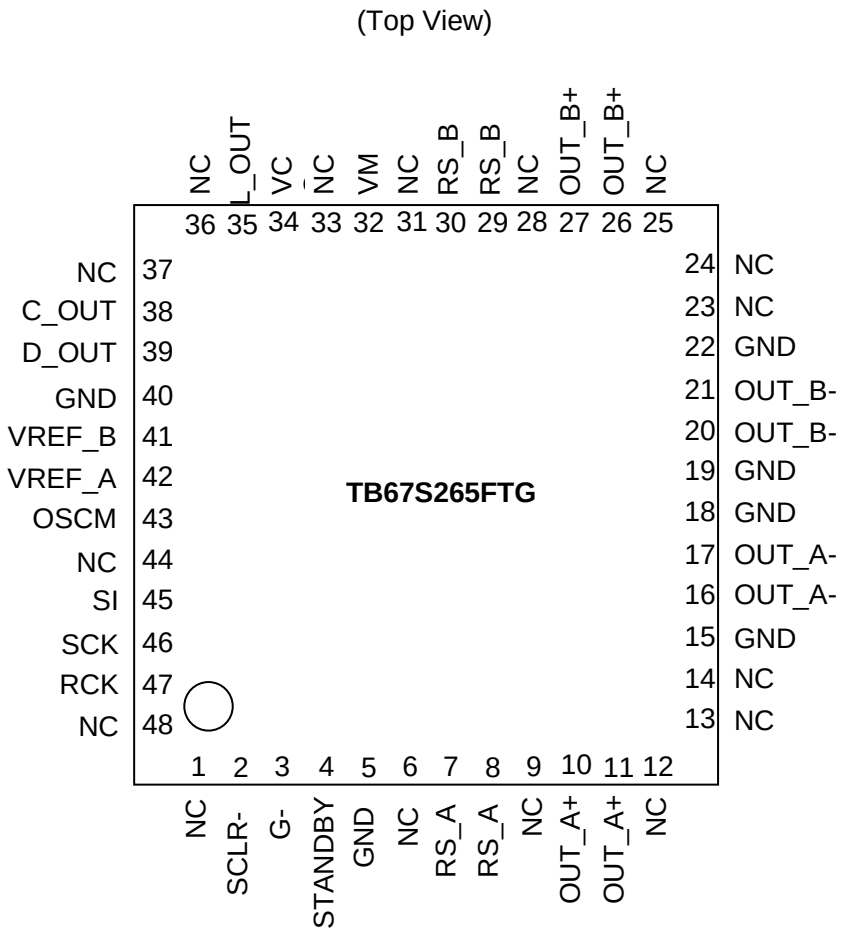


Figure3 Pin assignment

Note: Please mount the four corner pins of the QFN package and the exposed pad to the GND area of the PCB.

4. Block diagram

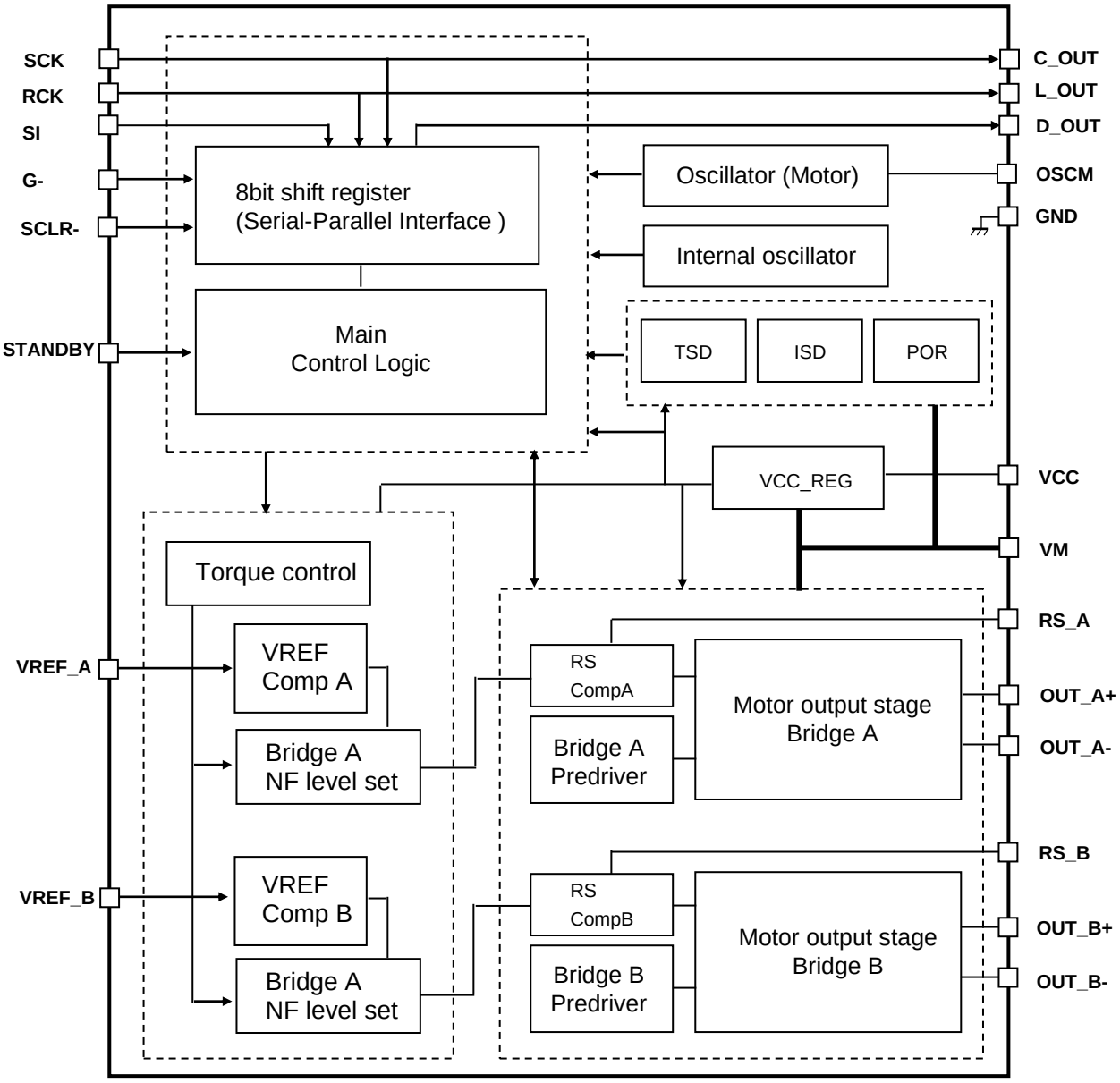


Figure4 Block diagram

Note: Functional blocks/circuits/constants in the block diagram may be omitted or simplified for explanatory purposes.

Note: All the grounding wires of the TB67S265 must run on the solder mask on the PCB, and be externally connected at a single point. Also, the grounding method should be considered for efficient heat dissipation.
Careful attention should be paid to the layout of the output, VM and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged.
Also, the utmost care should be taken for pattern designing and implementation of the device since it has power supply pins (VM, RS, OUT, GND) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may be destroyed.
The logic input pins must also be wired correctly. Otherwise, the device may be damaged owing to a current running through the IC that is larger than the specified current.

5. Pin explanations

Table5.1 Pin No.1 to 28 explanations

Pin No.	Pin Name	Function
1	NC(Note 1)	Non-connection pin
2	SCLR-	Serial register clear pin (low active)
3	G-	Serial data enable pin (low active)
4	STANDBY	Standby pin
5	GND	Ground pin
6	NC(Note 1)	Non-connection pin
7	RS_A(Note 2)	Motor Ach current sense pin
8	RS_A(Note 2)	Motor Ach current sense pin
9	NC(Note 1)	Non-connection pin
10	OUT_A+(Note 2)	Motor Ach (+) pin
11	OUT_A+(Note 2)	Motor Ach (+) pin
12	NC(Note 1)	Non-connection pin
13	NC(Note 1)	Non-connection pin
14	NC(Note 1)	Non-connection pin
15	GND	Ground pin
16	OUT_A-(Note 2)	Motor Ach (-) pin
17	OUT_A-(Note 2)	Motor Ach (-) pin
18	GND	Ground pin
19	GND	Ground pin
20	OUT_B-(Note 2)	Motor Bch (-) pin
21	OUT_B-(Note 2)	Motor Bch (-) pin
22	GND	Ground pin
23	NC(Note 1)	Non-connection pin
24	NC(Note 1)	Non-connection pin
25	NC(Note 1)	Non-connection pin
26	OUT_B+(Note 2)	Motor Bch (+) pin
27	OUT_B+(Note 2)	Motor Bch (+) pin
28	NC(Note 1)	Non-connection pin

Table5.2 Pin No.29 to 48 explanation

Pin No.	Pin Name	Function
29	RS_B(Note 2)	Motor Bch current sense pin
30	RS_B(Note 2)	Motor Bch current sense pin
31	NC(Note 1)	Non-connection pin
32	VM	Motor power supply pin
33	NC(Note 1)	Non-connection pin
34	VCC	Internal VCC regulator monitor pin
35	L_OUT	Serial ‘Latch’ output pin (logic output pin)
36	NC(Note 1)	Non-connection pin
37	NC(Note 1)	Non-connection pin
38	C_OUT	Serial ‘Clock’ output pin (logic output pin)
39	D_OUT	Shift register data output pin (logic output pin)
40	GND	Ground pin
41	VREF_B	Motor Bch output current set pin
42	VREF_A	Motor Ach output current set pin
43	OSCM	Oscillating circuit frequency for PWM chopping set pin
44	NC(Note 1)	Non-connection pin
45	SI	Serial ‘Data’ input pin
46	SCK	Serial ‘Clock’ input pin
47	RCK	Serial ‘Latch’ input pin
48	NC(Note 1)	Non-connection pin

Note 1: Please do not run patterns under NC pins.
Note 2: Please connect the pins with the same pin name.

6. INPUT/OUTPUT equivalent circuit

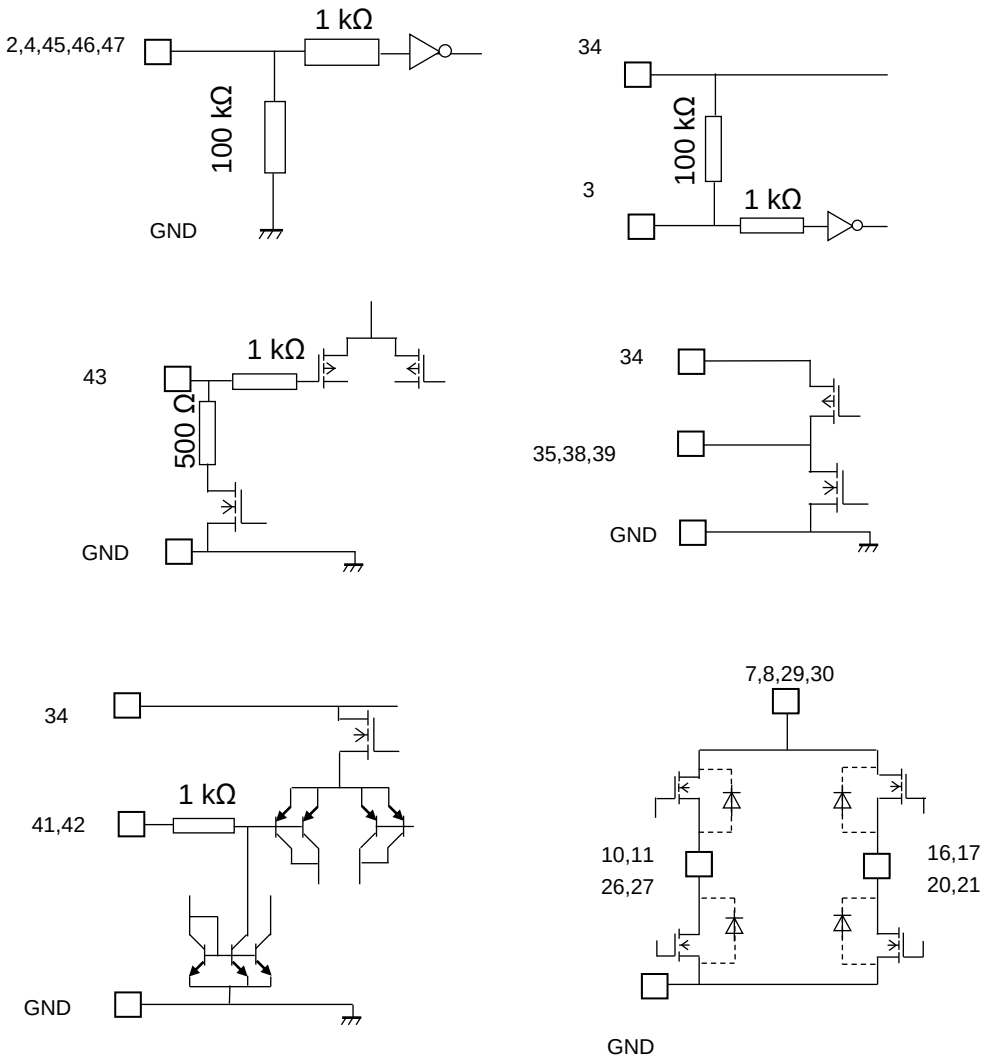


Figure6 INPUT/OUTPUT equivalent circuit

Table6 Pin Description

Pin No.	Pin Name	Pin No.	Pin Name
2	SCLR-	29	RS_B
3	G-	30	RS_B
4	STANDBY	32	VM
7	RS_A	34	VCC
8	RS_A	35	L_OUT
10	OUT_A+	38	C_OUT
11	OUT_A+	39	D_OUT
16	OUT_A-	41	VREF_B
17	OUT_A-	42	VREF_A
20	OUT_B-	43	OSCM
21	OUT_B-	45	SI
26	OUT_B+	46	SCK
27	OUT_B+	47	RCK

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

7. INPUT interface (8bit shift register + 8bit storage register)

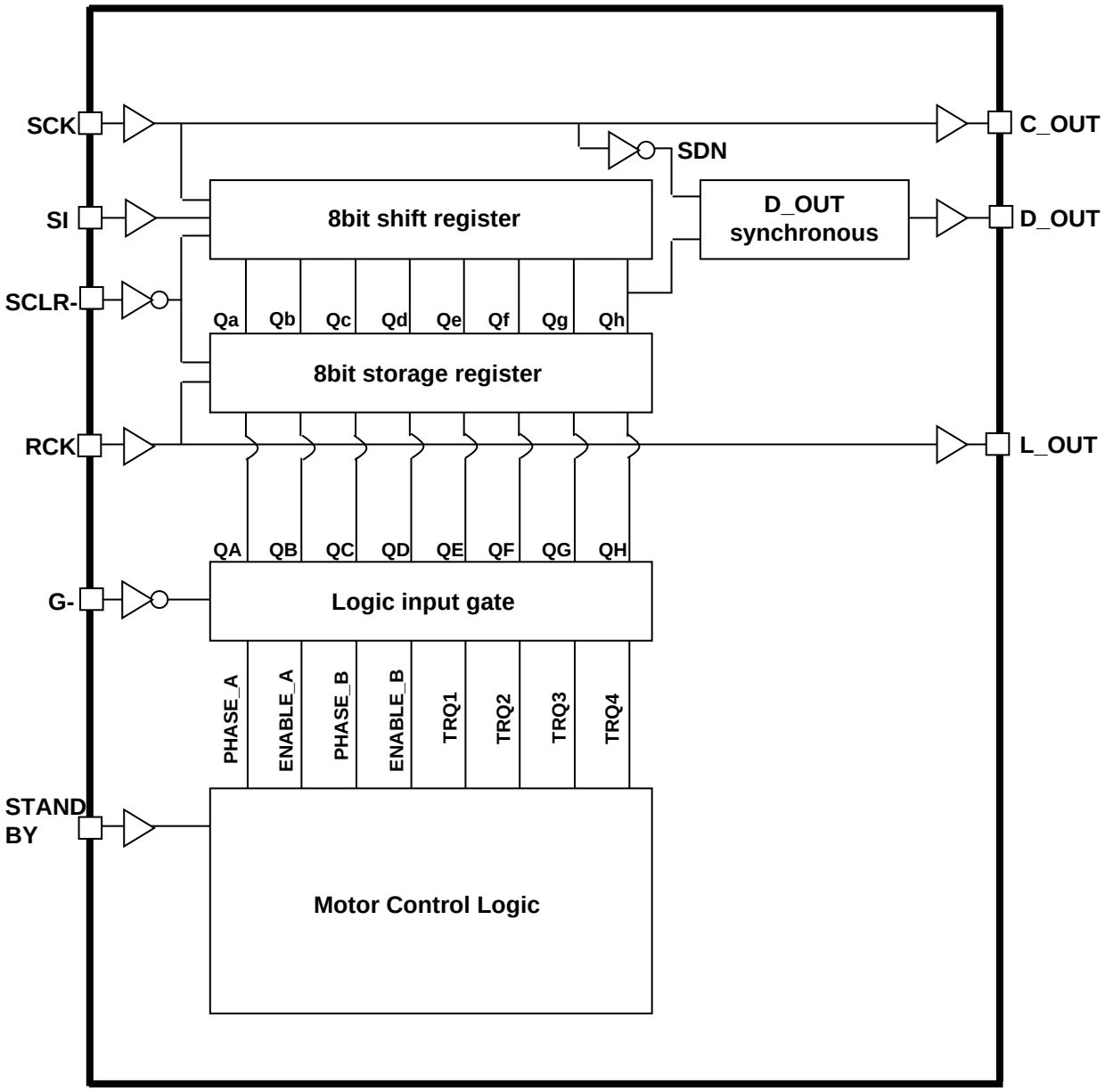


Figure 7 Input interface

Table 7.1 Initial status of logic input signal

Input signal	Initial status
SCK	Low
SI	Low
SCLR-	Low
RCK	Low
G-	High
STANDBY	Low

Note: If the logic signal is not asserted, the initial status of the logic pins will be as shown above.
SCLR-: Low=shift register and storage register is at the initial status.
G-: High=PHASE_A,ENABLE_A,PHASE_B,ENABLE_B,TRQ1,TRQ2,TRQ3,TRQ4=Disable
STANDBY=Low: Standby mode

Table7.2 Truth table

Input					Function
SI	SCK	SCLR-	RCK	G-	
X	X	X	X	H	PHASE_A,PHASE_B,ENABLE_A,ENABLE_B,TRQ1,TRQ2,TRQ3,TRQ4=Disable
X	X	X	X	L	PHASE_A,PHASE_B,ENABLE_A,ENABLE_B,TRQ1,TRQ2,TRQ3,TRQ4=Enable
X	X	L	X	X	Shift register and storage register is initialized
L	↑	H	X	X	The first data of the shift register is L, and the other register will be stored with the data before.
H	↑	H	X	X	The first data of the shift register is H, and the other register will be stored with the data before.
X	↓	H	X	X	The shift register data will maintain its status. The data after the shift register(Qh) will be output from D_OUT pin.
X	X	H	↑	X	Shift register data will be stored to the storage register.
X	X	H	↓	X	The storage register data will maintain its status.

X: Don't care

Note: To send the logic output data correctly to the next IC, please make sure to end the SCK data transfer with a Low signal.

8. Function explanation (Stepping motor mode)

The motor current is defined as plus when the current flows from OUT_X+ to OUT_X-, and defined minus when the current flows from OUT_X- to OUT_X+.

Table8.1 Function explanation

Signal	H	L	Notes
ENABLE_X	OUTPUT: ON	OUTPUT: OFF	When ENABLE_X is set to L, no matter what the PHASE status are, the corresponding output stage will be set OFF(Hi-z).
PHASE_X	OUT_X+: H OUT_X-: L	OUT_X+: L OUT_X-: H	When set to H, the current will flow from OUT_X+ to OUT_X- at charge status.
STANDBY	Motor operational	Standby mode	When STANDBY is set to L, the internal OSC circuit as well as output stage is set OFF; therefore the motor will not operate.

Table8.2 <Full step>

Ach			Bch		
INPUT		OUTPUT	INPUT		OUTPUT
PHASE_A	ENABLE_A	IOUT (A)	PHASE_B	ENABLE_B	IOUT (B)
H	H	+100 %	H	H	+100 %
L	H	-100 %	H	H	+100 %
L	H	-100 %	L	H	-100 %
H	H	+100 %	L	H	-100 %

Table8.3 <Half step>

Ach			Bch		
INPUT		OUTPUT	INPUT		OUTPUT
PHASE_A	ENABLE_A	IOUT (A)	PHASE_B	ENABLE_B	IOUT (B)
H	H	+100 %	H	H	+100 %
x	L	0 %	H	H	+100 %
L	H	-100 %	H	H	+100 %
L	H	-100 %	x	L	0 %
L	H	-100 %	L	H	-100 %
x	L	0 %	L	H	-100 %
H	H	+100 %	L	H	-100 %
H	H	+100 %	x	L	0 %

X : Don't care

Table8.4 Torque (TRQ) function: Current Ratio

TRQ1	TRQ2	TRQ3	TRQ4	Current Ratio
L	L	L	L	0 %
L	L	L	H	5 %
L	L	H	L	10 %
L	L	H	H	15 %
L	H	L	L	25 %
L	H	L	H	29 %
L	H	H	L	38 %
L	H	H	H	43 %
H	L	L	L	52 %
H	L	L	H	60 %
H	L	H	L	67 %
H	L	H	H	74 %
H	H	L	L	80 %
H	H	L	H	86 %
H	H	H	L	94 %
H	H	H	H	100 %

9. Absolute Maximum Ratings (T_a = 25 °C)

Table9 Absolute Maximum Ratings

Characteristics		Symbol	Rating	Unit	Remarks
Motor power supply		V_M	50	V	-
Motor output voltage		V_{OUT}	50	V	-
Motor output current (per channel)		I_{OUT}	2.0	A	(Note 1)
Internal VCC voltage		V_{CC}	6.0	V	When externally supplied
Logic input voltage		V_{IH}	6.0	V	
Logic output current		I_{OH}	-7.0	mA	
		I_{OL}	7.0	mA	
VREF input voltage		V_{REF}	5.0	V	
Power dissipation	WQFN48	P_D	1.3	W	(Note 2)
Operating temperature		T_{opr}	-20 to 85	°C	
Storage temperature		T_{stg}	-55 to 150	°C	
Junction temperature		T_j	150	°C	

Note 1: Usually the maximum current value should be controlled below 70 %($I_{OUT} \leqq 1.4$ A) or less of the absolute maximum ratings for a standard based on thermal rating. The maximum output current may be further limited due to thermal considerations, depending on ambient temperature and board conditions.

Note 2: Device alone. (T_a =25 °C)
If the ambient temperature is above 25 °C, the power dissipation must be de-rated by 10.4 mW/°C.

T_a: Ambient temperature

T_{opr} : Ambient temperature while the device is active

T_j: Junction temperature while the device is active. The maximum junction temperature is limited by the thermal shutdown(TSD) circuitry. It is advisable to keep the maximum current below a certain level so that the maximum junction temperature, T_j(max), will not exceed 120 °C.

Caution: Absolute maximum ratings

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded,
even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. The device does not have overvoltage detection circuit. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied.
All voltage ratings, including supply voltages, must always be followed. The other notes and considerations described later should also be referred to.

10. Operation ranges (T_a = 0 to 85 °C)

Table10 Operation ranges

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Motor power supply	V_M	10	24	47	V	-
Motor output current	I_{OUT}	-	1.4	2.0	A	(Note 1)
Logic input voltage	$V_{IN(H)}$	3.0	-	5.5	V	Logic H level
	$V_{IN(L)}$	0	-	2.0	V	Logic L level
Chopping frequency set range	$f_{chop(range)}$	40	100	150	kHz	-
VREF input voltage	V_{REF}	GND	3.0	3.6	V	-

Note 1: Maximum current for actual usage may be limited by the operating circumstances such as operating conditions (exciting mode, operating time, etc), ambient temperature, and heat conditions (board condition and so on).

11. Electrical Specifications 1(DC) (T_a = 25 °C, V_M = 24 V, unless specified otherwise)

Table11 Electrical Specifications 1

Characteristics		Symbol	Test conditions	Min	Typ.	Max	Unit
Logic input voltage	HIGH	$V_{IN(H)}$	Logic input (Note 1)	3.0	-	5.5	V
	LOW	$V_{IN(L)}$	Logic input (Note 1)	0	-	2.0	V
Logic input hysteresis		$V_{IN(HYS)}$	Logic input (Note 1)	300	-	500	mV
Logic input current	HIGH	$I_{IN(H)}$	Logic input voltage:3.3 V	-	33	50	μA
	LOW	$I_{IN(L)}$	Logic input voltage:0 V	-	-	1	μA
Logic output pin voltage	HIGH	$V_{OH(LO)}$	I_{OH}=-3 mA, VCC based	-0.41	-0.34	-0.27	V
	LOW	$V_{OL(LO)}$	I_{OL}=3 mA, GND based	0.20	0.25	0.30	V
Power consumption		I_{M1}	Output pins=open Standby mode	-	2	3.5	mA
		I_{M2}	Output pins=open Standby release ENABLE=Low	-	3.5	5.5	mA
		I_{M3}	Output pins=open Full step resolution	-	5.5	7	mA
Output leakage current	HIGH	I_{OH}	V_{RS}=V_M=50 V,V_{OUT}=0 V	-	-	1	μA
	LOW	I_{OL}	V_{RS}=V_M=V_{OUT}=50 V	1	-	-	μA
Motor current channel differential		ΔI_{OUT1}	Current differential between channels	-5	0	5	%
Motor current setting accuracy		ΔI_{OUT2}	I_{OUT}=1.0 A (Note 2)	-5	0	5	%
RS pin current		I_{RS}	V_{RS}=V_M=24 V	0	-	10	μA
Output MOSFET On resistance (High+Low side)		$R_{on(S)\_PN}$	T_j=25 °C, I_{OUT}=2.4 A, Forward direction (High-side+Low-side)	-	0.8	0.9	Ω

Note1: $V_{IN(H)}$ is defined as the V_{IN} voltage that causes the outputs (OUTA,OUTB) to change when a pin under test is gradually raised from 0 V. $V_{IN(L)}$ is defined as the V IN voltage that causes the outputs (OUTA, OUTB) to change when the pin is then gradually lowered from 5 V. The difference between $V_{IN(H)}$ and $V_{IN(L)}$ is defined as the $V_{IN(HYS)}$.

Note2: When using the internal VCC regulator and for VREF input voltage with a resistance divider; taking VCC accuracy and VREF ratio in to consideration, the motor current setting accuracy specification will be ±8 %.

Note: When the logic signal is applied to the device whilst the V_M power supply is not asserted; the device is designed not to function, but for safe usage, please apply the logic signal after the V_M power supply is asserted and the V_M voltage reaches the proper operating range.

12. Electrical Specifications 2(DC) (T_a=25 °C, V_M=24 V, unless specified otherwise)

Table12 Electrical Specifications 2

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
VREF input voltage	V_{REF}	V_M=24 V,V_{CC}=5 V	GND	3.0	3.6	V
VREF input current	I_{REF}	V_{REF}=3 V	-	0	1	μA
VCC pin voltage	V_{CC}	I_{CC}=5 mA	4.75	5.0	5.25	V
VCC pin current	I_{CC}	V_{CC}=5 V	-	2.5	5	mA
VREF ratio	$V_{REF(gain)}$	V_{REF}=2 V	1/5.2	1/5.0	1/4.8	-
Thermal shutdown threshold	T_{SD}	(Note 1)	140	150	170	°C
VM POR threshold	V_{MR}	-	7	8	9	V
Over-current detection threshold	I_{SD}	(Note 2)	2.1	3.0	4.0	A

Note1: About Thermal shutdown (TSD)

When the junction temperature of the device reaches the TSD threshold, the TSD circuit is triggered; the internal reset circuit then turns off the output transistors. Noise rejection blanking time is built-in to avoid misdetection.

Once the TSD circuit is triggered; the detect latch signal can be cleared by reasserting the VM power source, or setting the device to standby mode. The TSD circuit is a backup function to detect a thermal error, therefore is not recommended to be used aggressively.

Note2: About Over-current detection (ISD)

When the output current reaches the threshold, the ISD circuit is triggered; the internal reset circuit then turns off the output transistors. In order to avoid malfunction due to the switching, IC have a dead time. Once the ISD circuit is triggered, the detect latch signal can be cleared by reasserting the VM power source, or setting the device to standby mode. For fail-safe, please insert a fuse to avoid secondary trouble.

12.1. Back-EMF

While the motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.

If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the device or other components will be damaged or fail due to the motor back-EMF.

12.2. Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety. If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.

The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

12.3. IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

13. Electrical Specification 3(AC) (T_a = 25 °C, V_M = 24 V, L=6.8 mH, R=5.7 Ω)

Table13 Electrical Specification 3

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Minimum pulse width (SCK,RCK,SI input signal)	$t_{w(H)}$	f_{OSCM}=1600 kHz	250	-	-	ns
	$t_{w(L)}$	f_{OSCM}=1600 kHz	250	-	-	ns
Minimum setup time	t_{set1}	SCLR- → SCK	50	-	-	ns
	t_{set2}	SI → SCK	50	-	-	ns
	t_{set3}	SCK → RCK	50	-	-	ns
Minimum clock signal cycle (SCK,RCK)	t_{cyc}	f_{OSCM}=1600 kHz	500	-	-	ns
Minimum hold time	t_{hold1}	SCK → SI	50	-	-	ns
	t_{hold2}	SCLR- → Data	50	-	-	ns
Output transistor switching specific	t_r	Motor output	70	120	170	ns
	t_f	Motor output	100	150	200	ns
Analog noise blanking time	At_{BLK}	V_M=24 V,I_{OUT}=1 A Analog t_{BLK}	250	400	550	ns
Oscillator reference frequency	f_{OSCM}	C_{OSC}=270 pF, R_{OSC}=3.6 kΩ	1360	1600	1840	kHz
Chopping frequency	f_{chop}	Output ACTIVE (I_{OUT}=1 A), f_{OSCM}= 1600 kHz	-	100	-	kHz

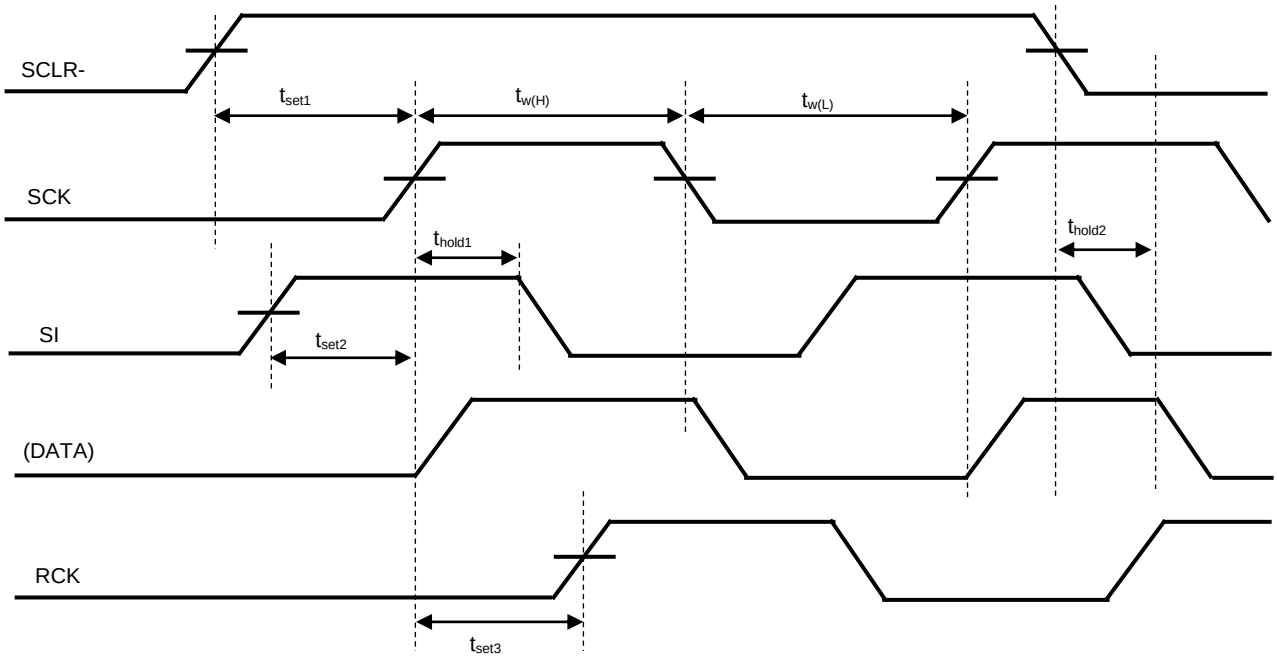


Figure13 AC Timing charts

Note: Timing charts may be simplified for explanatory purpose.

14. Decay function

14.1. ADMD(Advanced Dynamic Mixed Decay) constant current control

The Advanced Dynamic Mixed Decay threshold, which determines the current ripple level during current feedback control, is a unique value.

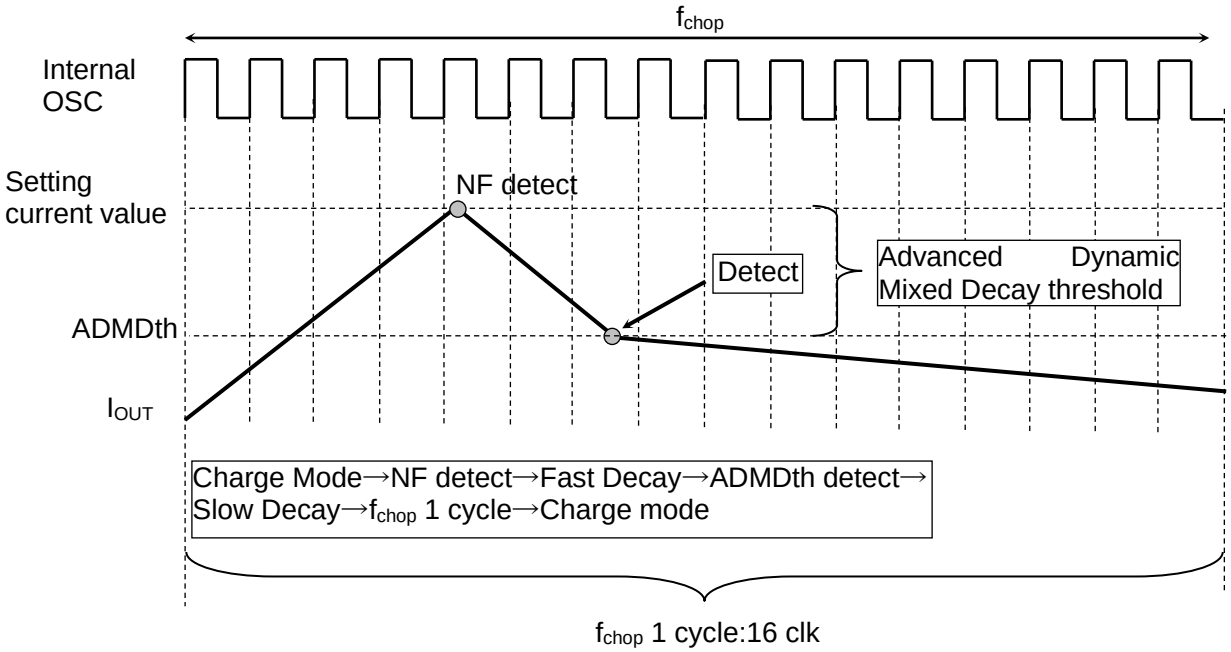


Figure14.1 ADMD(Advanced Dynamic Mixed Decay) constant current control

14.2. Auto Decay Mode current waveform

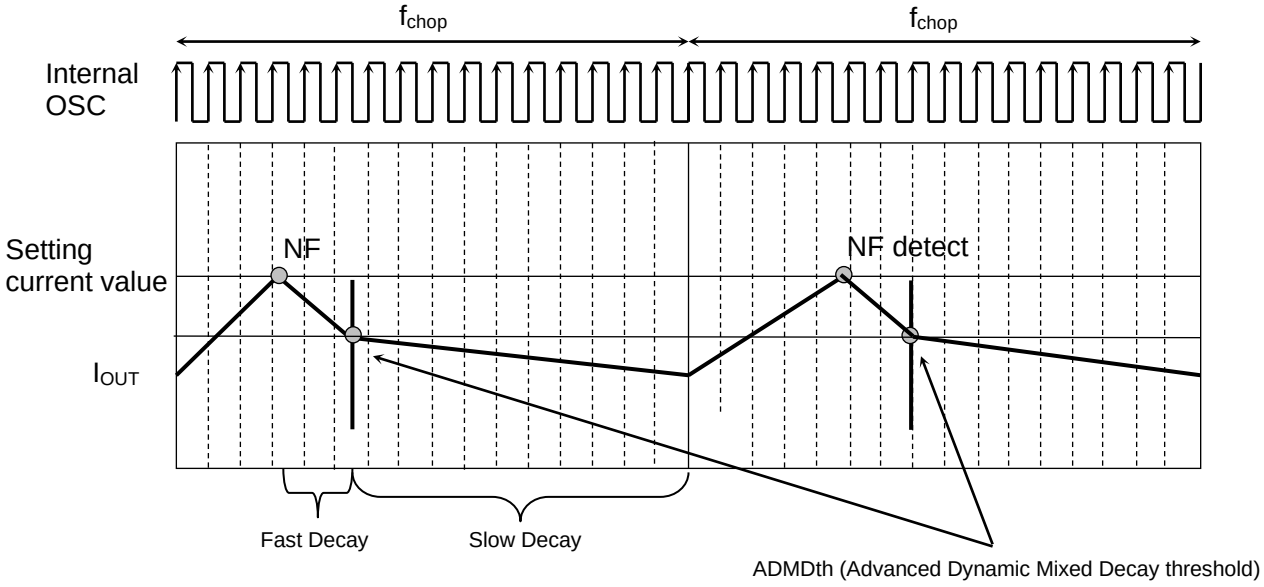


Figure14.2. Auto Decay Mode current waveform

Note: Timing charts may be simplified for explanatory purpose.

14.3. ADMD current waveform

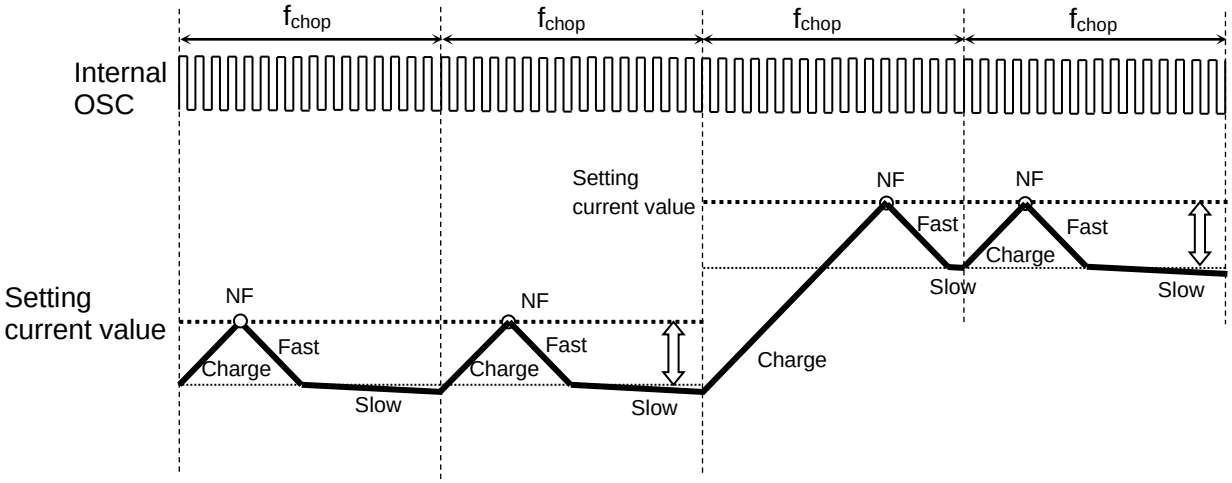


Figure14.3.1 When the next current step is higher

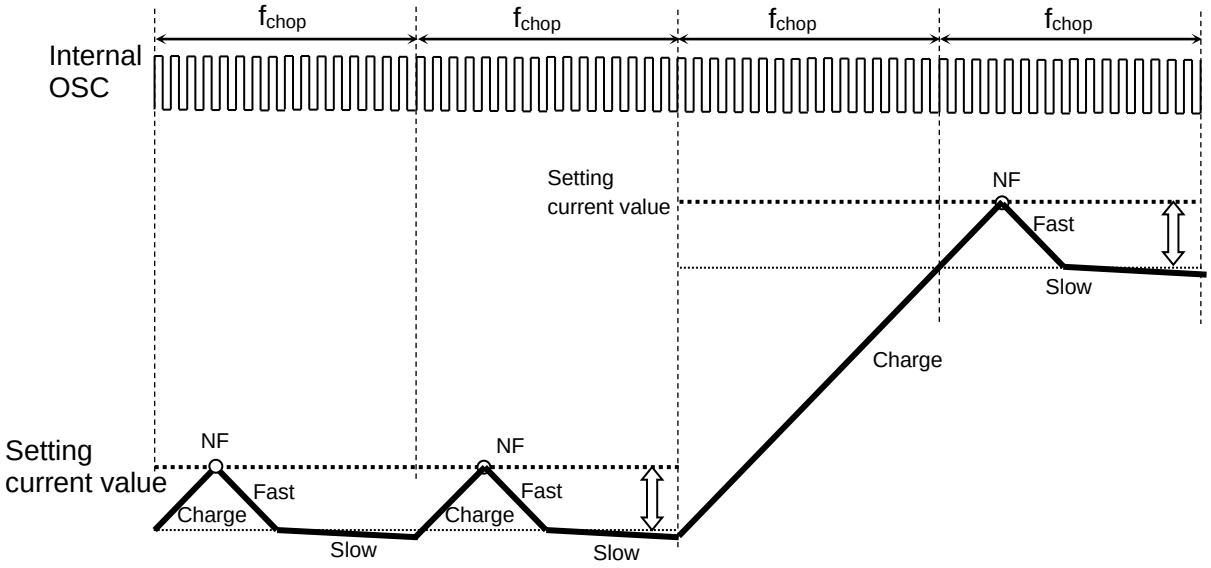


Figure14.3.2 When Charge period is more than 1 fchop cycle

Note : When the Charge period is longer than fchop cycle, the Charge period will be extended until the motor current reaches the NF threshold. Once the current reaches the next current step, then the sequence will go on to ADMD control.

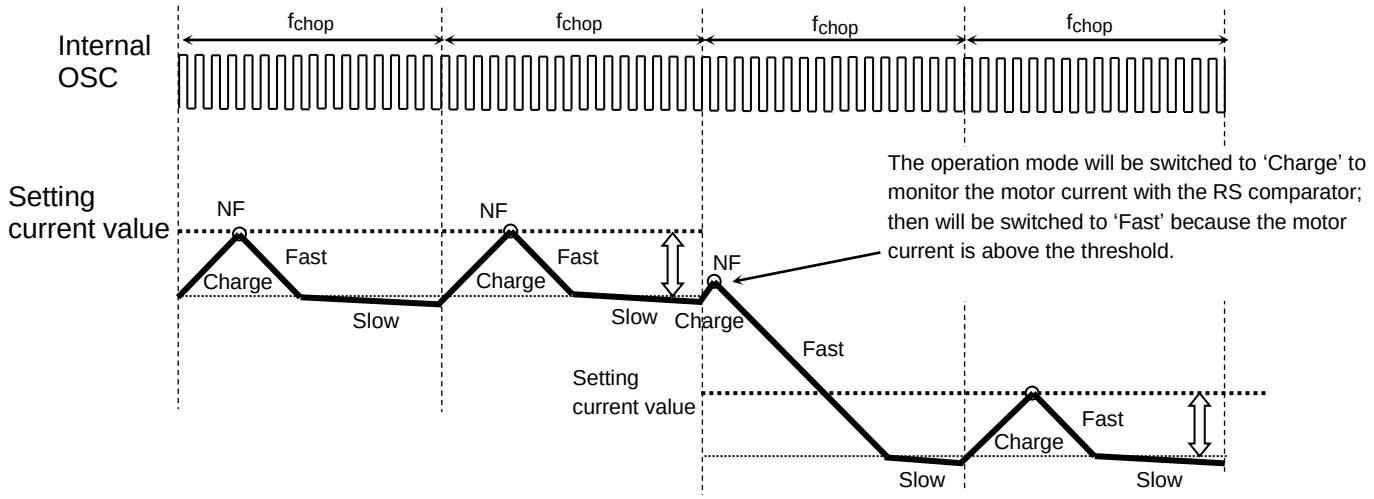


Figure14.3.3 When the next current step is lower

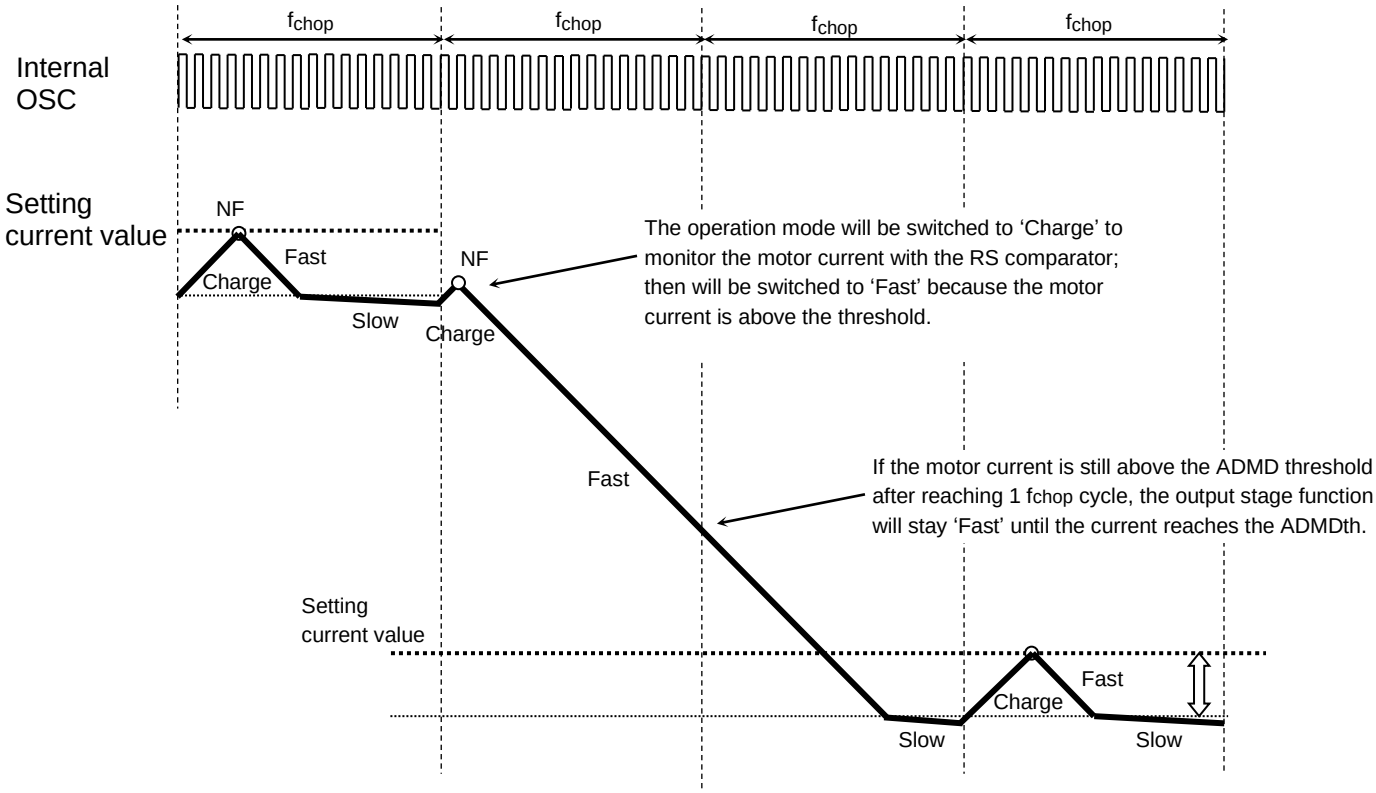
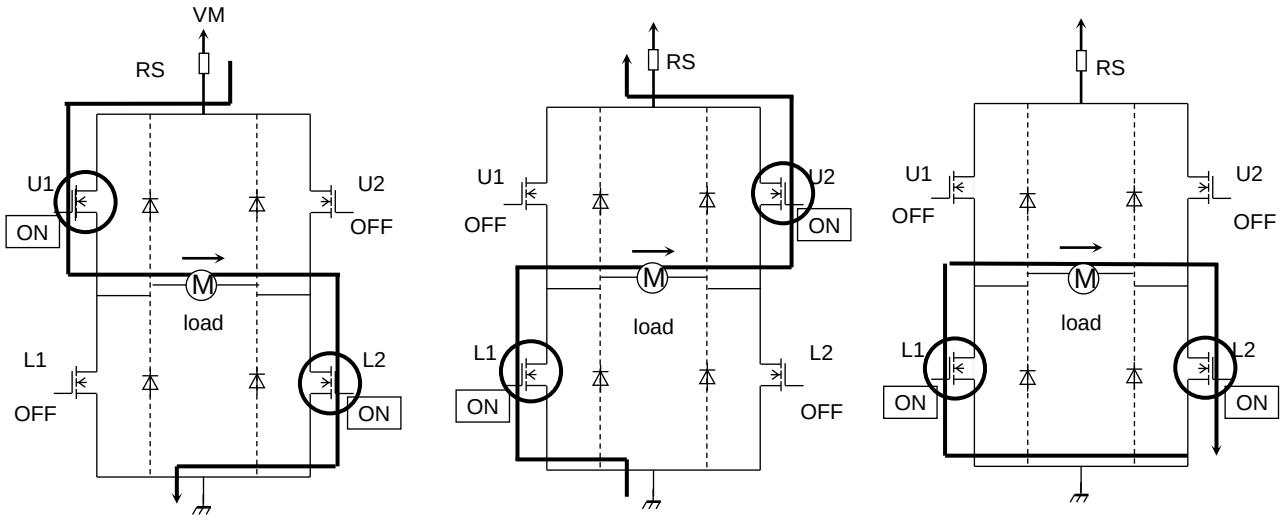


Figure14.3.4 When the Fast continues past 1 f_{chop} cycle
(the motor current not reaching the ADMD threshold during 1 f_{chop} cycle)

15. Output transistor function mode



Charge mode
Flows the current into the load.

Slow mode
Circulates the current within the device and load.

Fast mode
Recirculates the energy back to the power supply.

Figure15 Motor output MOSFET operation mode

15.1. Output transistor function

Table15.1.1 At positive current

MODE	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: This table shows an example of when the current flows as indicated by the arrows in the figures shown above.
If the current flows in the opposite direction, refer to the following table.

Table15.1.2 At negative current

MODE	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

Note: This IC controls the motor current to be constant by 3 modes listed above.
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

16. Calculation of the Predefined Output Current

For PWM constant-current control, this IC uses a clock generated by the OSCM oscillator.
The peak output current (Peak current) can be set via the current-sensing resistor (R_S) and the reference voltage (V_{ref}), as follows:

$$I_{OUT(max)} = V_{ref(gain)} \times \frac{V_{ref}(V)}{R_{RS}(\Omega)}$$

$V_{ref(gain)}$: the V_{ref} decay rate is 1/ 5.0 (typ.)

For example : In the case of a 100 % setup
when V_{ref} = 3.0 V, Torque=100 %,R_S=0.51 Ω, the motor constant current (Peak current) will be calculated as:

I_{OUT} = 3.0 V / 5.0 / 0.51 Ω= 1.18 A

17. Calculation of the OSCM oscillation frequency (chopper reference frequency)

An approximation of the OSCM oscillation frequency (f_{OSCM}) and chopper frequency (f_{chop}) can be calculated by the following expressions.

f_{OSCM}=1/[0.56x{Cx(R_1+500)}]
*C,R_1: External components for OSCM (C=270 pF , R_1=5.1 kΩ => f_{OSCM}= 1.12 MHz(Typ.))

f_{chop} = f_{OSCM} / 16
*f_{OSCM}=1.12 MHz => f_{chop} =About 70 kHz

If chopping frequency is raised, Rippl of current will become small and wave-like reproducibility will improve. However, the gate loss inside IC goes up and generation of heat becomes large.

By lowering chopping frequency, reduction in generation of heat is expectable. However, Rippl of current may become large. It is a standard about about 70 kHz. A setup in the range of 50 to 100 kHz is recommended.

18. Power consumption of the IC

Power of the IC is consumed by the transistor of the output block and that of the logic block mainly.

18.1. Power consumption of the motor output block (R_{on} = 0.6 Ω)

Power of the output block ($P_{(out)}$) is consumed by MOSFET of upper and lower H-Bridge.

$P_{(out)}$=Number of H-Bridge × I_{OUT} (A) × V_{DS} (V) = 2 (ch) × I_{OUT} (A) × I_{OUT} (A) × R_{on} (Ω)…….(1)

When the current waveform of the motor output corresponds to the ideal waveform, average power of output block can be provided as follows;

When R_{on} = 0.6 Ω, $I_{OUT\ (peak:\ Max)}$ = 1.0 A, V_M = 24 V
$P_{(out)}$ = 2 (ch) × 1.0 (A) × 1.0 (A) × 0.6 (Ω)…….....(2)
= 1.2 (W)

18.2. Power consumption of logic and IM systems

Power consumptions of logic and IM systems are calculated by separating the states (operating and stopping).

$I_{(IM3)}$ = 5.5 mA (typ.) : Operating
$I_{(IM2)}$ = 3.5 mA (typ.) : Stopping

Output system is connected to V_M (24 V). (Output system: Current consumed by the circuit connected to VM+ Current consumed by switching output steps)

Power consumption is calculated as follows;

$P_{(IM)}$ = 24 (V) × 0.0055 (A)…….(3)
= 0.132 (W)

18.3. Power consumption

Total power consumption $P_{(total)}$ is calculated from the values of formula (2) and (3).

$P_{(total)} = P_{(out)} + P_{(IM)}$ = 1.2+ 0.132 = 1.332(W)

Standby mode is released. The power consumption in non-operation mode of the motor (waiting mode) is calculated as follows;

$P_{(standby)}$ = 24 (V) × 0.0035 (A) = 0.084 (W)

Refer to the above equations, evaluate the heat design of the board by the actual board enough, and configure the appropriate margin.

19. Step resolution sequence

19.1. Full step resolution sequence

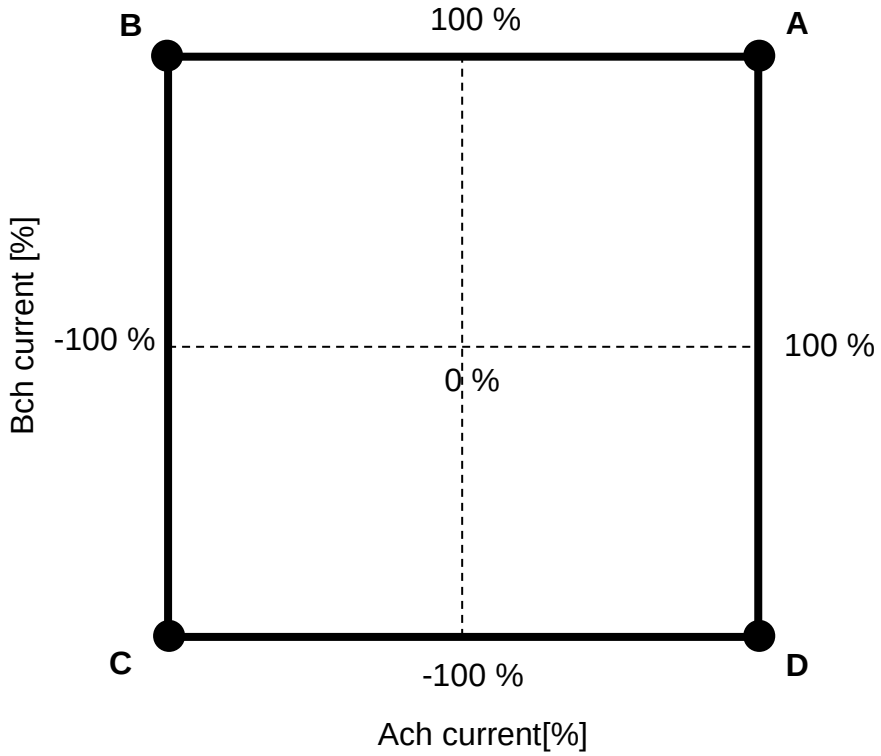


Figure19.1.1 Full step resolution sequence

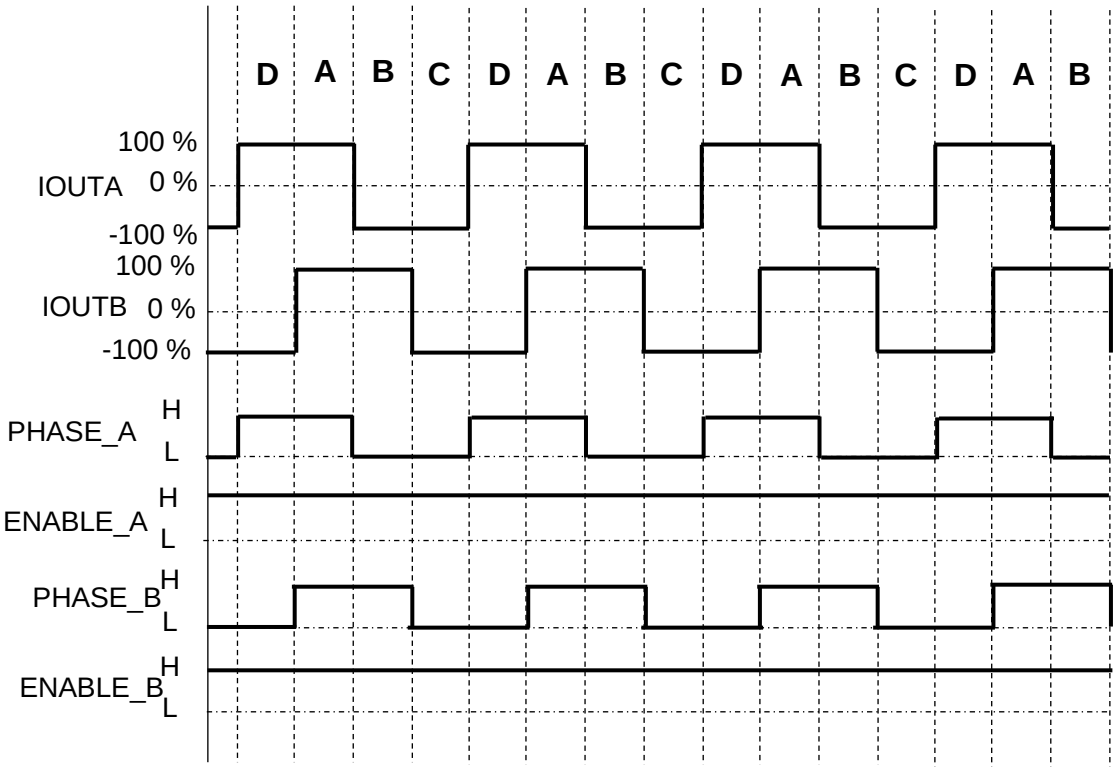


Figure19.1.2 Full step resolution sequence timing chart

Note: Timing charts may be simplified for explanatory purpose.

19.2. Half step(a) resolution sequence

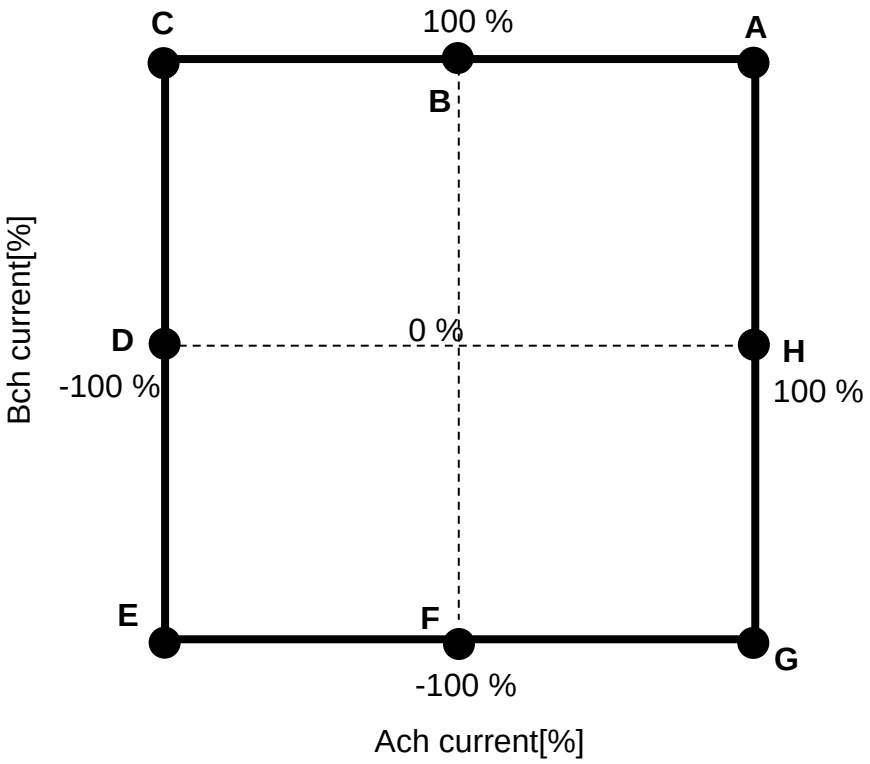


Figure19.2.1 Half step(a) resolution sequence

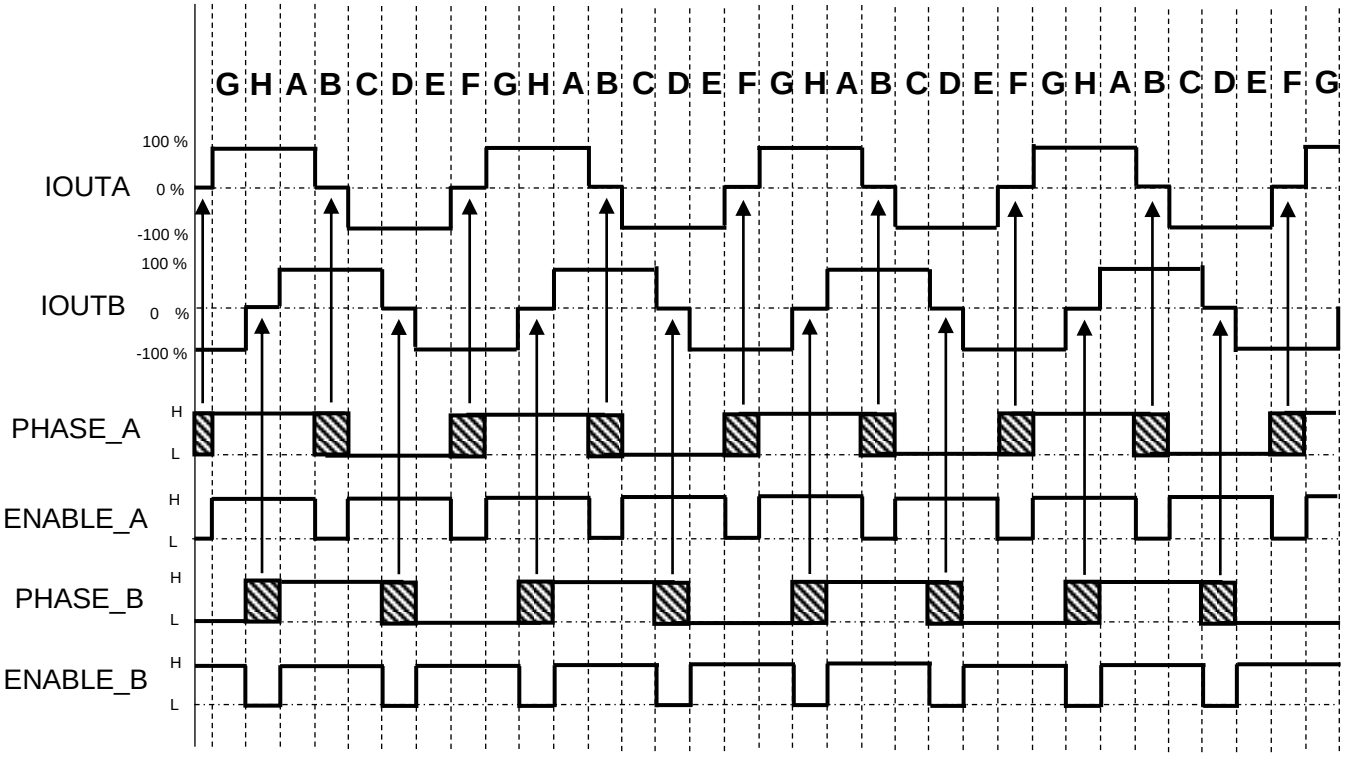


Figure19.2.2 Half step(a) resolution sequence timing chart

Note: Timing charts may be simplified for explanatory purpose.

20. Step resolution sequence

20.1. Full step resolution sequence (TRQ1/TRQ2,TRQ3,TRQ4 settings)

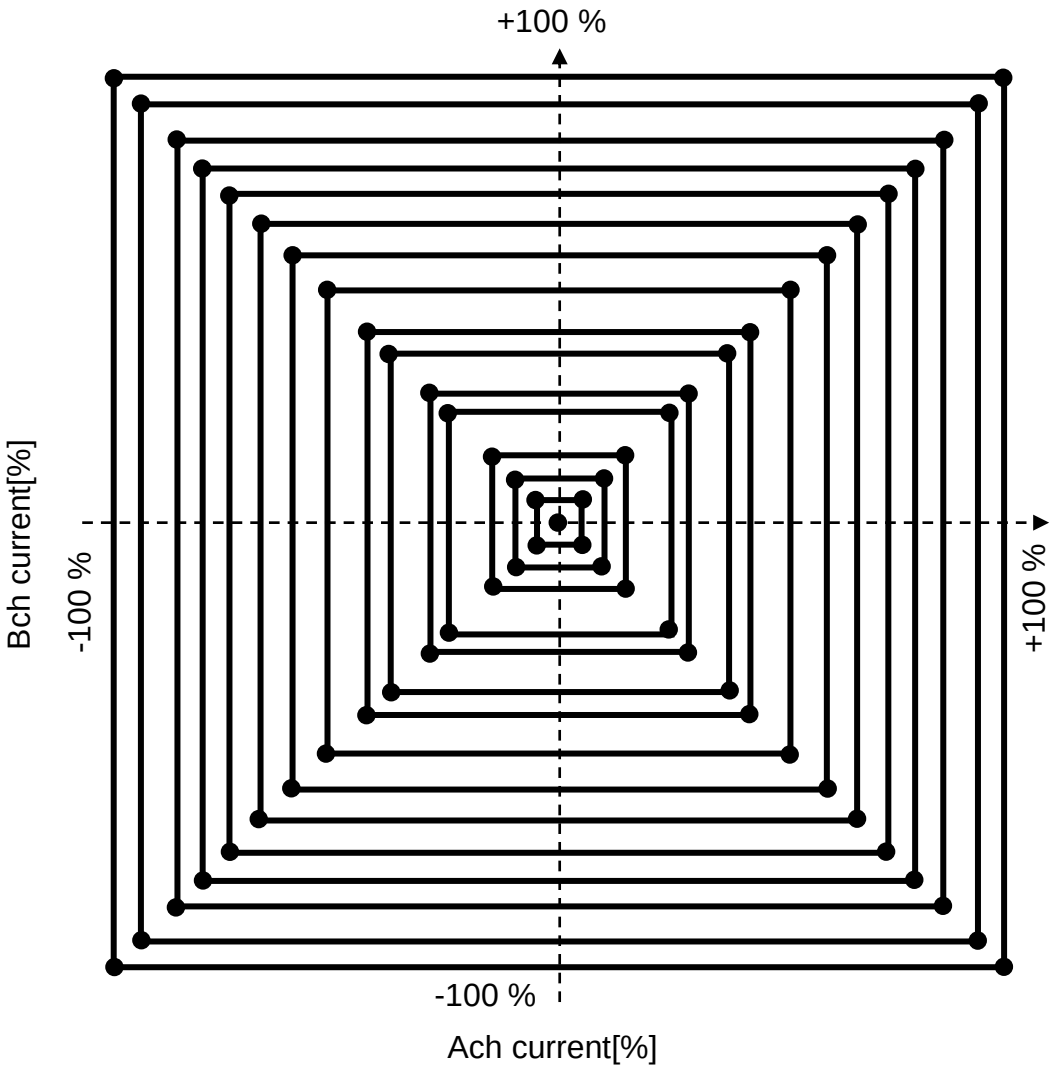


Figure20.1 Full step resolution sequence (TRQ1/TRQ2,TRQ3,TRQ4 settings)

Table20.1.1 (Example) <Full step resolution> (TRQ1,TRQ2,TRQ3,TRQ4=H,H,H,H=100 %)

Ach			Bch		
INPUT		OUTPUT	INPUT		OUTPUT
PHASE_A	ENABLE_A	I_{OUT}(A)	PHASE_B	ENABLE_B	I_{OUT} (B)
H	H	+100 %	H	H	+100 %
L	H	-100 %	H	H	+100 %
L	H	-100 %	L	H	-100 %
H	H	+100 %	L	H	-100 %

Table20.1.2 (Example) <Full step resolution> (TRQ1,TRQ2,TRQ3,TRQ4=H,L,L,H=60 %)

Ach			Bch		
INPUT		OUTPUT	INPUT		OUTPUT
PHASE_A	ENABLE_A	I_{OUT}(A)	PHASE_B	ENABLE_B	I_{OUT}(B)
H	H	+60 %	H	H	+60 %
L	H	-60 %	H	H	+60 %
L	H	-60 %	L	H	-60 %
H	H	+60 %	L	H	-60 %

20.2. Half step resolution sequence (TRQ1,TRQ2,TRQ3,TRQ4 settings)

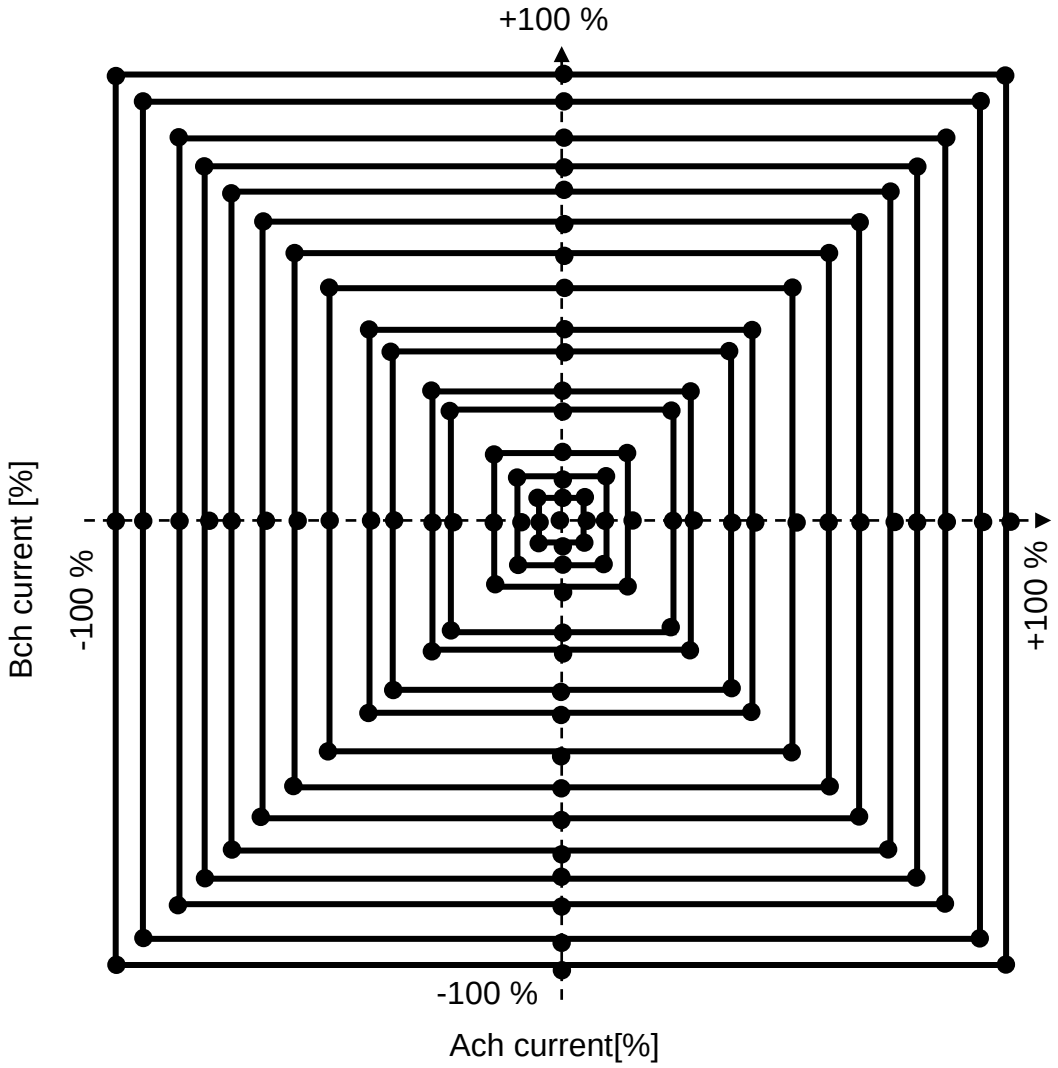


Figure20.2 Half step resolution sequence (TRQ1,TRQ2,TRQ3,TRQ4 settings)

Table20.2.1 (Example) <Half step(a) resolution> (TRQ1,TRQ2,TRQ3,TRQ4=H,H,H,H=100 %)

Ach			Bch		
INPUT		OUTPUT	INPUT		OUTPUT
PHASE_A	ENABLE_A	I_{OUT} (A)	PHASE_B	ENABLE_B	I_{OUT} (B)
H	H	+100%	H	H	+100 %
x	L	0 %	H	H	+100 %
L	H	-100 %	H	H	+100 %
L	H	-100 %	x	L	0 %
L	H	-100 %	L	H	-100 %
x	L	0 %	L	H	-100 %
H	H	+100 %	L	H	-100 %
H	H	+100 %	x	L	0 %

Table20.2.2 (Example) <Half step(a) resolution> (TRQ1,TRQ2,TRQ3,TRQ4=L,H,L,L=25 %)

Ach			Bch		
INPUT		OUTPUT	INPUT		OUTPUT
PHASE_A	ENABLE_A	I_{OUT} (A)	PHASE_B	ENABLE_B	I_{OUT} (B)
H	H	+25 %	H	H	+25 %
x	L	0 %	H	H	+25 %
L	H	-25 %	H	H	+25 %
L	H	-25 %	x	L	0 %
L	H	-25 %	L	H	-25 %
x	L	0 %	L	H	-25 %
H	H	+25 %	L	H	-25 %
H	H	+25 %	x	L	0 %

21. Blanking time for over current detection (ISD)

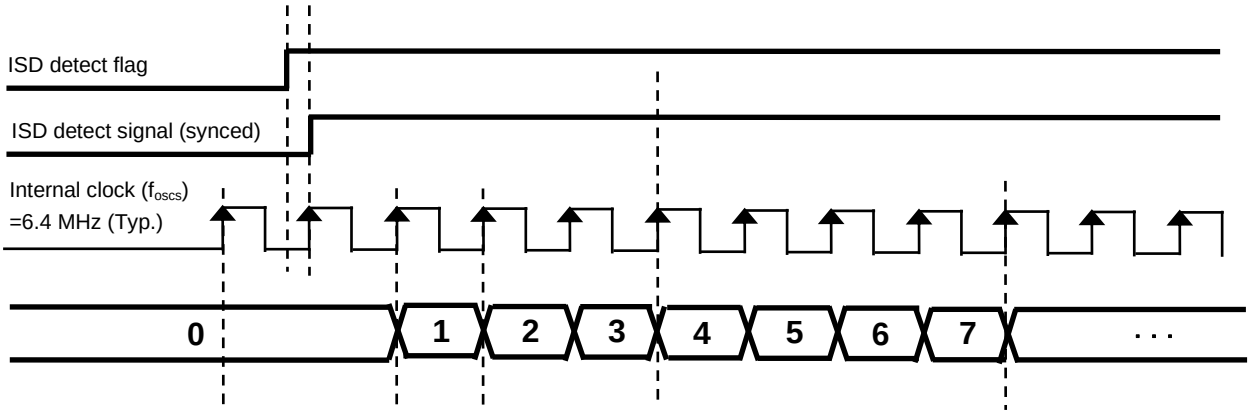


Figure21 Blanking time for over current detection timing chart

Note: Timing charts may be simplified for explanatory purpose.

To avoid miss detecting, the over current detection circuit has a blanking time to reject any spike current which may or may not appear when switching operation. This blanking time is counted by the internal OSC(6.4 MHz (Typ.)).

*f_{oscs}=6.4 MHz(Typ.) internal clock
$1/f_{oscs}$ × 7 to 8 clk worth(1.09 μs to 1.25 μs)

Please note that this blanking time is an example when the current flows ideally, therefore the ISD circuit may not function correctly in some cases. Therefore please insert protective fuse for safe use. Fuse constants may change due to usage conditions; so please select which operates correctly.

22. Blanking time for thermal shutdown detection (TSD)

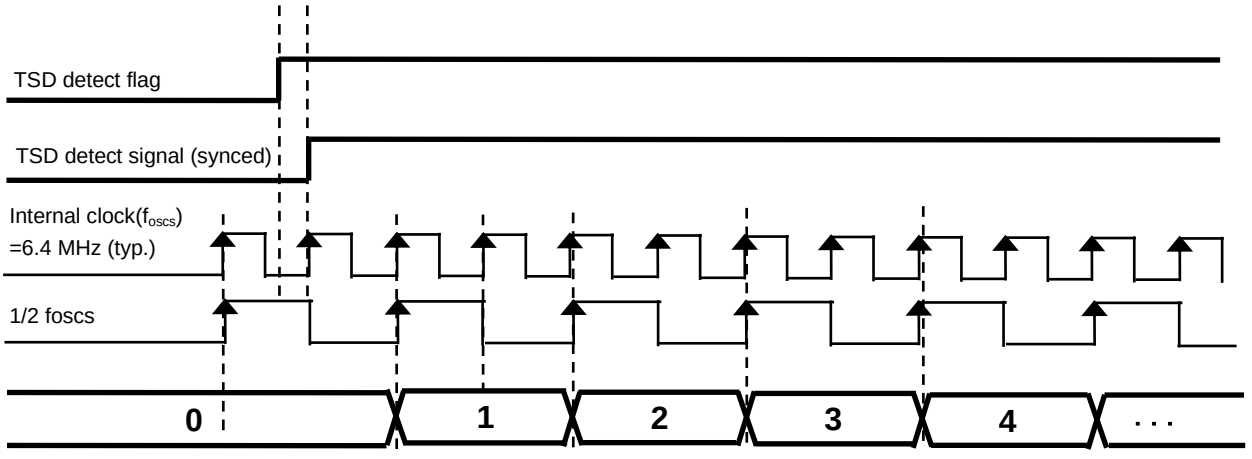


Figure22 Blanking time for over thermal detection timing chart

Timing charts may be simplified for explanatory purpose.

To avoid miss detecting, the thermal shutdown detection circuit has a blanking time to reject any spike current which may or may not appear when switching operation. This blanking time is counted by the internal OSC(6.4 MHz (Typ.).

*f_{oscs}=6.4 MHz(Typ.) internal clock
$1/(f_{oscs}/2)$ × 7 to 8 clk=$1/f_{oscs}$ × 14 to 16clk worth(2.5 μs to 2.8 μs)

23. (For reference) PD-Ta graph

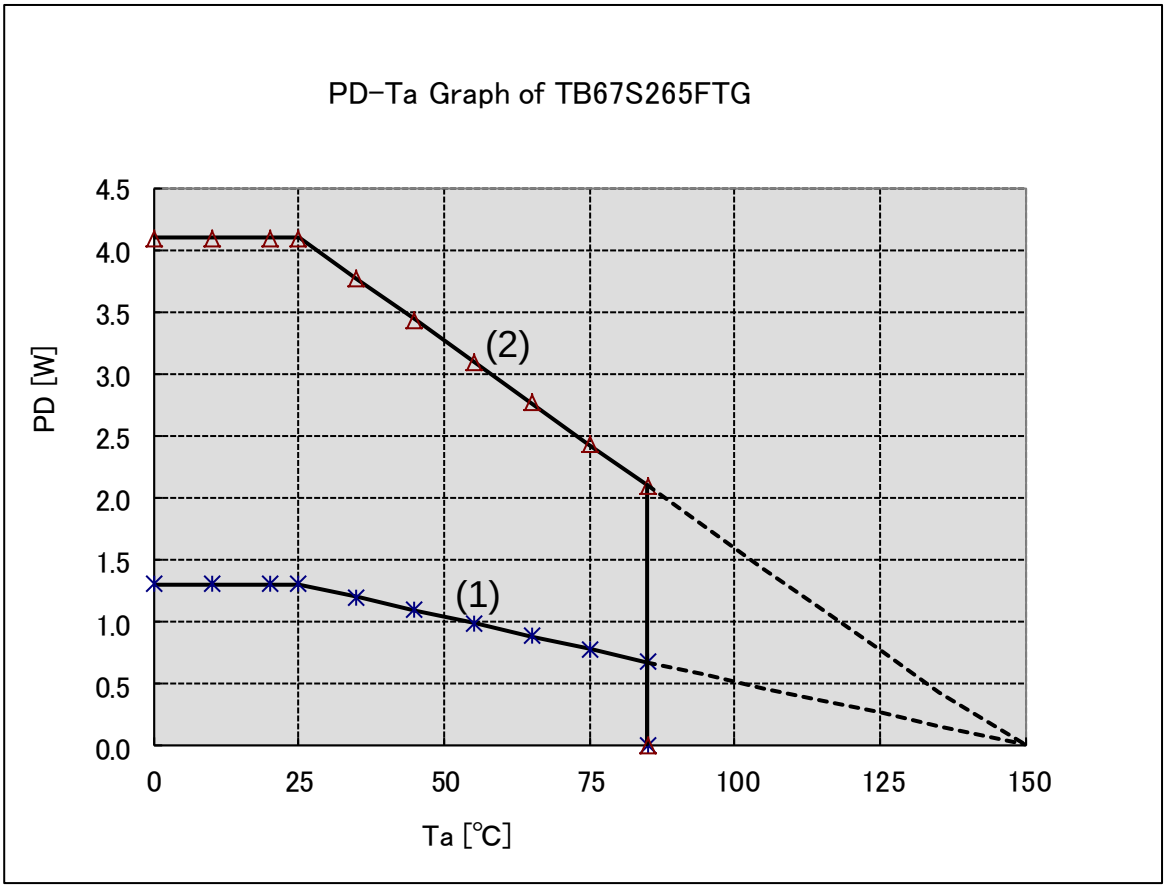


Figure23 (For reference) PD-Ta graph

(1) Rth(j-a) Device alone (96 °C/W)

If the ambient temperature is above 25 °C, please de-rate by 10.4 mW/°C.

(2) When mounted to a 4-layer glass epoxy board (power dissipation example of Rth(j-a)=25 °C/W (when mounted); dependent of board and mount condition.)

If the ambient temperature is above 25 °C, please de-rate by 33.3 mW/°C.

24. TB67S265FTG Application circuit example

(Each constant of external components is for reference.)

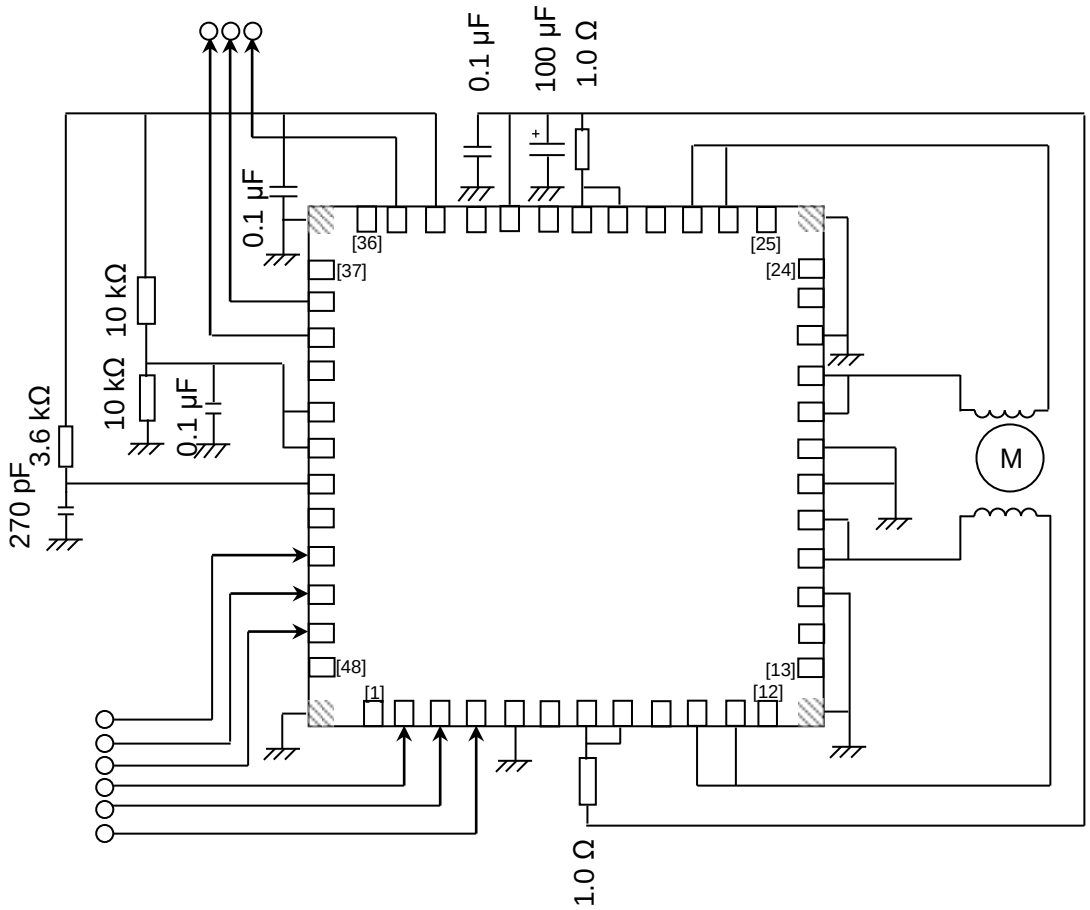


Figure24 TB67S265FTG Application circuit

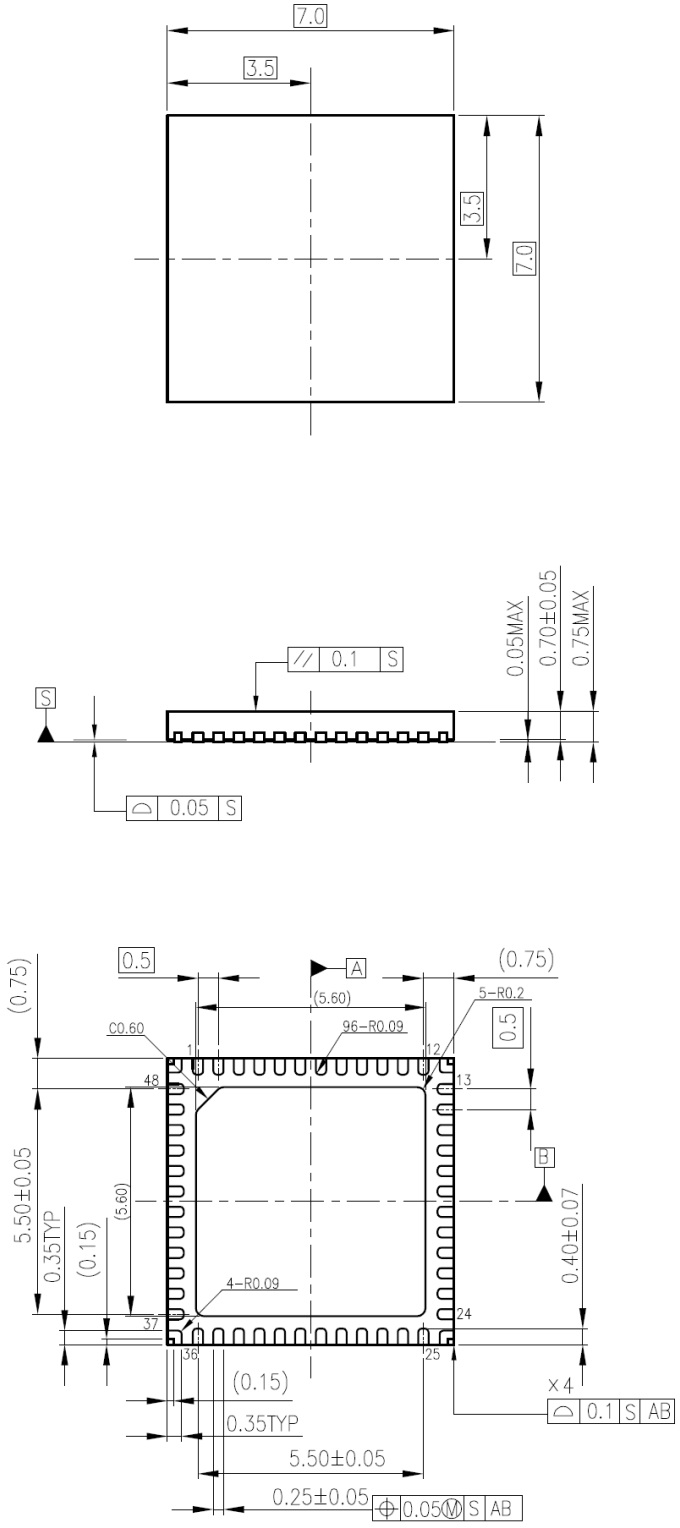
Note: The shaded area above shows the GND pin and area, also the area shown in gray is non-connection pins.

Note: Please consider adding capacitors if necessary. Also, make sure that the GND pattern is connected at a single point if possible. There are two pins each for OUT_A-, OUT_A+, OUT_B-, OUT_B+, therefore make sure to connect both pins when using the device.

Note: Please mount the four corner pins of the QFN package and the exposed pad to the GND area of the PCB. The application circuit above is an example; therefore, mass-production design is not guaranteed.

25. Package Dimensions

P-WQFN48-0707-0.50-003 **Unit: mm**



Weight: 0.10 g (Typ.)

Figure26 Package dimensions

26. Notes on Contents

Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Timing Charts
Timing charts may be simplified for explanatory purposes.

Application Circuits
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Test Circuits
Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

27. IC Usage Considerations

27.1. Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage, or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke, or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke, or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

27.2. Points to remember on handling of ICs

(1) Over Current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator, or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops, or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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