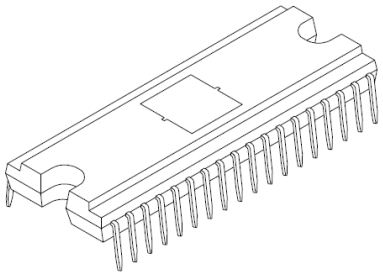
TOSHIBA Bi-CMOS Power Integrated Circuit Multi-Chip Package (MCP)

TB67B000HG

High voltage

3-Phase Full-Wave Sine-Wave PWM Brushless Motor Driver

The TB67B000HG is a high-voltage PWM BLDC motor driver. The product integrates a sine-wave PWM/wide-angle commutation controller and the high-voltage driver in a single package ("two-in-one"). It is designed to change the speed of a BLDC directly motor by using a speed control signal (analog) from a microcontroller.



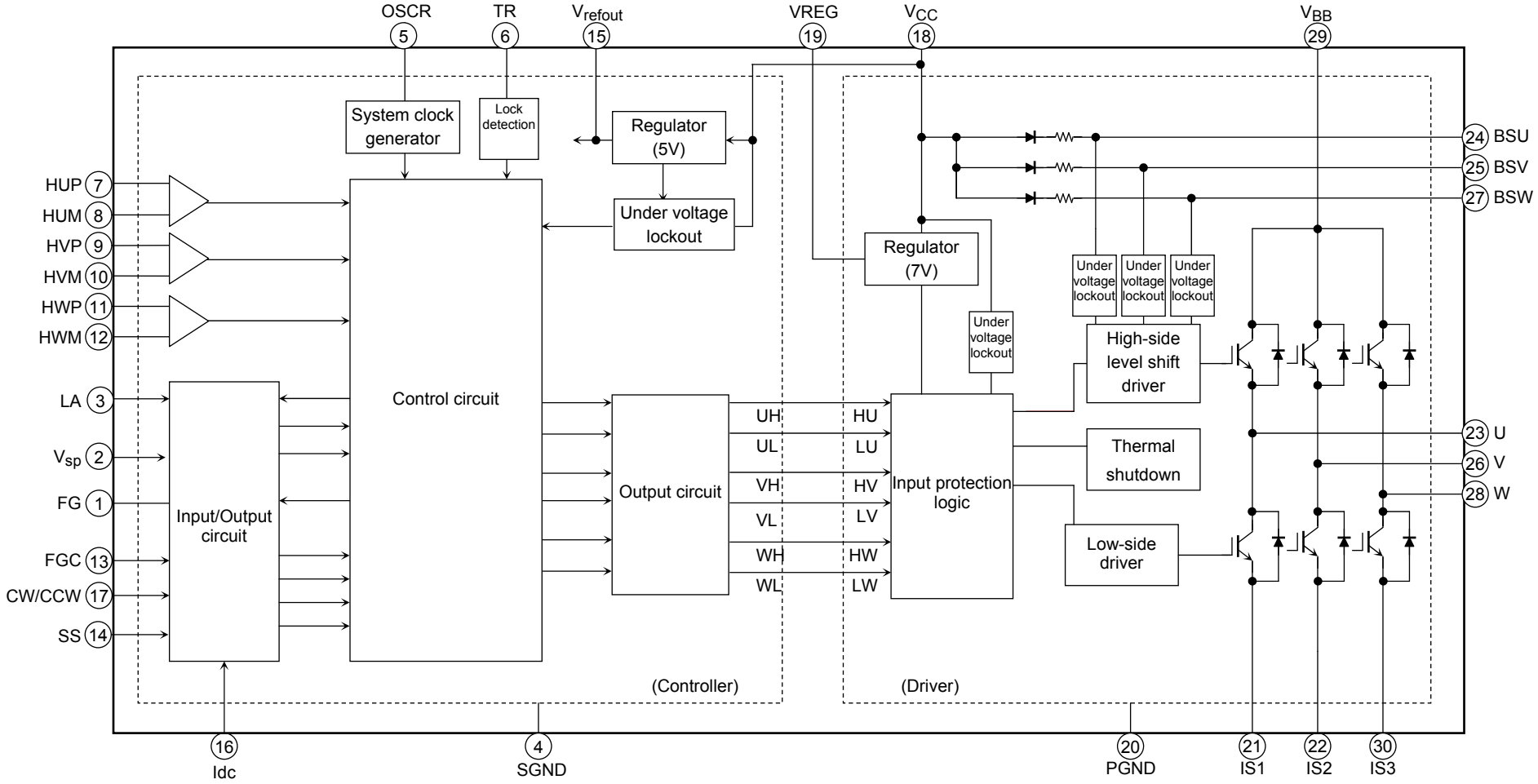
P-HDIP30-1233-1.78-001

Weight: 2.59 g (typ.)

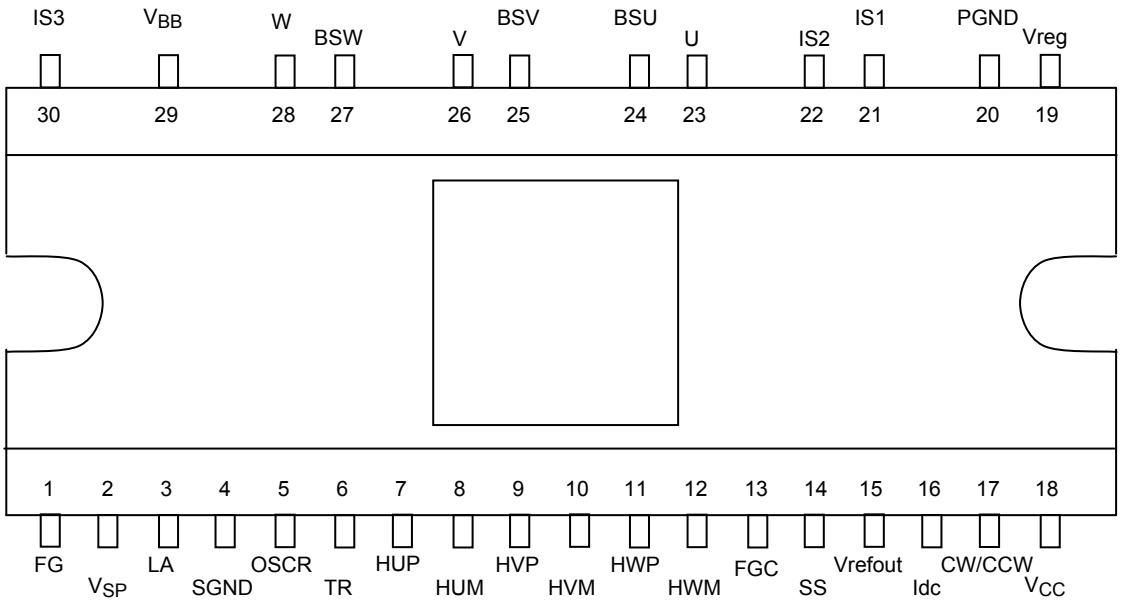
Features

- A Controller and a high-voltage driver integrated in a single package.
  Sine-wave PWM drive or wide-angle commutation drive is selectable.
- IGBTs arranged in three bridge units
- Built-in oscillator circuit (carrier frequency = f_{osc}/252 (Hz))
- High-side bootstrap supply: Built-in bootstrap diode
- Built-in overcurrent protection, thermal shutdown, undervoltage lockout, and motor-lock detection.
- On-chip regulator (V_{reg} = 7 V (typ.), 30 mA (max), Vrefout = 5 V (typ.), 35 mA (max))
- Operating power supply voltage range: V_{CC} = 13.5 to 16.5 V
- Motor power supply operating voltage range: V_{BB} = 50 to 450 V

Block Diagram



Pin Assignment



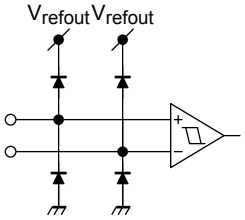
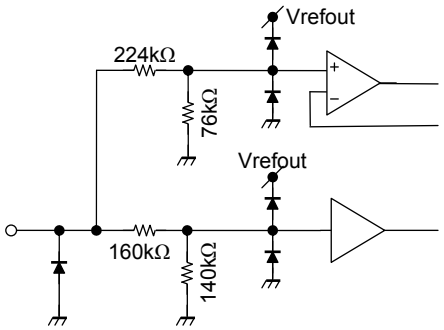
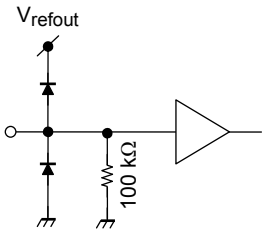
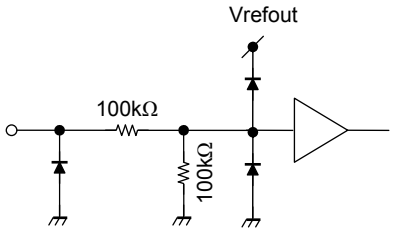
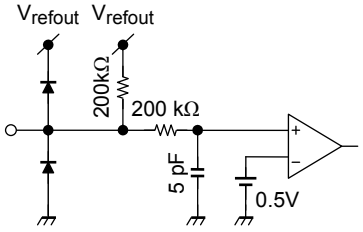
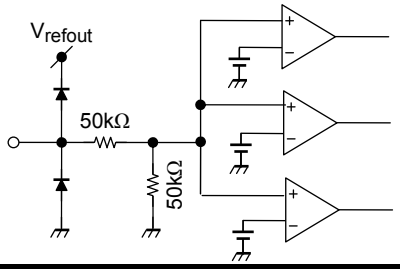
Note: Die pad on surface and PGND is connected. When using the heat sink, handle it not to short with the IC therminals. When applying the different potential with GND level to the heat sink, insulate with die pad and the heat sink.

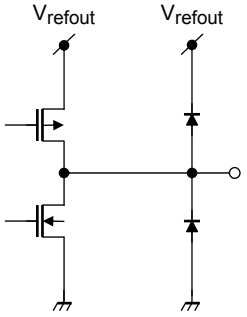
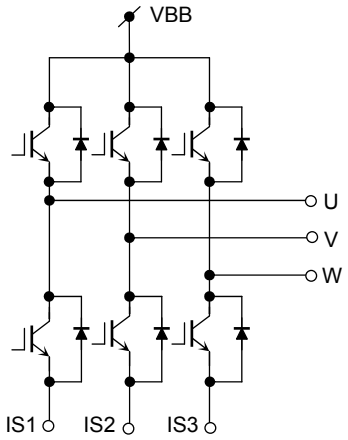
Pin Description

Pin No.	Symbol	Description	Function
1	FG	FG signal output	FGC = H: FG = output 1ppr FGC = M: FG = output 2.4ppr FGC = L: FG = output 3ppr ppr: one pulse per one electrical angle
2	V_{SP}	Voltage command input	This pin has a pull-down resistor. (150 kΩ)
3	LA	Lead angle control input	This pin has a pull-down resistor. (200 kΩ) Input voltage range: 0 to 5V (V_{refout}) SS=H: 0 to 28° in 16 steps. SS=L: 0 to 58° in 32 steps.
5	OSCR	Resistor for oscillation	Connect a resistor for internal clock oscillation.
6	TR	Motor lock detection	Connect a capacitor for motor lock detection oscillation or connect to GND.
7	HUP	U-phase hall input+	When position signal outputs HHH or LLL, gate block protection drives. Built-in digital filter (≃ 1.6 μs)
8	HUM	U-phase hall input-	
9	HVP	V-phase hall input+	
10	HVM	V-phase hall input-	
11	HWP	W-phase hall input+	
12	HWM	W-phase hall input-	
13	FGC	FG output signal switch	This pin has a pull-down resistor. (100 kΩ) H: FG=output 1ppr. M: FG=output 2.4ppr. L: FG=output 3ppr. ppr: one pulse per one electrical angle
15	V_{refout}	Reference voltage output	5 V (typ.), 35 mA (max), Connecting a capacitor for voltage stability.
14	SS	Switch for commutation waveform	This pin has a pull-down resistor. (100 kΩ) H: Wide-angle commutation (150° commutation) L: Sine-wave PWM drive (180° commutation)
17	CW/CCW	Forward/Reverse switching input	This pin has a pull-down resistor. (100 kΩ) H: Forward L: Reverse
16	Idc	Current limit input	This pin has a pull-up resistor. (200 kΩ) DC link input Reference potential of 0.5 V. This pin has a RC filter (≈ 1 μs) and a digital filter (≈ 0.6 μs).
4	SGND	Ground pin	Signal ground. Connect with PGND.
19	VREG	Reference voltage output	7V (typ.), 30 mA (max). Connecting a capacitor for voltage stability.
18	V_{CC}	Power supply pin for the power stage	15 V (typ.)
20	PGND	Ground pin	Power ground Connect with SGND.
23	U	U-phase output pin	—
24	BSU	Bootstrap supply (phase U)	For connecting a bootstrap capacitor to the U-phase output.
21	IS1	U-phase IGBT emitter	For connecting a detecting resistor for motor coil current to the PGND pin.
22	IS2	V-phase IGBT emitter	For connecting a detecting resistor for motor coil current to the PGND pin.
25	BSV	Bootstrap supply (phase V)	For connecting a bootstrap capacitor to the V-phase output.
26	V	V-phase output pin	—
29	V_{BB}	High-voltage power supply pin	Power supply pin for driving a motor.
27	BSW	Bootstrap supply (phase W)	For connecting a bootstrap capacitor to the W-phase output.
28	W	W-phase output pin	—
30	IS3	W-phase IGBT emitter	For connecting a detecting resistor for motor coil current to the PGND pin.

Input/Output Equivalent Circuits

Equivalent circuit diagrams may be partially omitted or simplified for explanatory purposes.

Pin	Input/Output Signal	Internal Circuit
HUP HUM HVP HVM HWP HWM	Analog / Digital Hysteresis: ±7.5 mV (typ.) Digital filter time constant: 1.6 μs (typ.)	
V_{SP}	Analog V_{SP} voltage range: 0 to 10 V Internal pull-down resistor: 150kΩ	
CW/CCW SS	Digital L: 0.8 V (max) H: V_{refout} − 1 V (min) Internal pull-down resistor: 100kΩ	
LA	Analog LA voltage range: 0 to 5 V (V_{refout}) Internal pull-down resistor: 200kΩ	
Idc	Analog Analog filter time constant: 1.0 μs (typ.) Digital filter time constant: 0.6 μs (typ.) Internal pull-up resistor: 200kΩ	
FGC	Digital L: 0.8 V (max) M: 2.0V(min) 3.0V(max) H: V_{refout} − 1 V (min) Internal pull-down resistor: 100kΩ	

Pin	Input/Output Signal	Internal Circuit
FG	Digital Push-pull output (±2 mA max) FGC=H: 1ppr FGC=M: 2.4ppr FGC=L: 3ppr	
U V W IS1 IS2 IS3	U,V,W-phase output pin U,V,W-phase IGBT emitter pin	

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{BB}	500	V
	V_{CC}	18	
Input voltage	$V_{in\ (1)}$	−0.3 to V_{CC} (Note 1)	V
	$V_{in\ (2)}$	−0.3 to V_{refout} +0.3 (Note 2)	
Output current (DC)	I_{OUT}	2	A
Output current (pulse 1ms)	I_{OUTP}	3 (Note 3)	A
V_{reg} current	I_{reg}	30	mA
V_{refout} current	I_{refout}	35	mA
Power dissipation	P_D	35 (Note 4)	W
Operating temperature	T_{opr}	−30 to 115 (Note 5)	°C
Strage temperature	T_{stg}	−55 to 150	°C

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.Please use the TB67B000HG within the specified operating ranges.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: $V_{in\ (1)}$ pin: V_{SP} and LA

Note 2: $V_{in\ (2)}$ pin: HUP, HUM, HVP, HVM, HWP, HWM, SS, FGC, CW/CCW, and I_{dc}.

Note 3: Apply pulse

Note 4: Package thermal resistance (θ j-c = 1 °C/W) with an infinite heat sink at Ta = 25°C

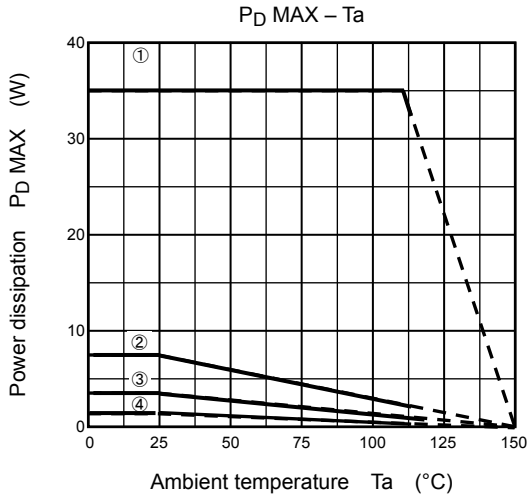
Note 5: The operating temperature range is determined according to the P_D MAX − Ta characteristics.

Operating conditions (Ta = 25°C)

Characteristics	Symbol	Min	Typ.	Max	Unit
Power supply voltage	V_{BB}	50	280	450	V
	V_{CC}	13.5	15	16.5	
Oscillation frequency	F_{OSC}	3.5	5	6.4	MHz
Output current	Iout	—	—	2	A
Operating temperature	T_{opr}	−30 (Note 6)	—	115 (Note 6)	°C

Note 6: The operating temperature range is determined according to the P_D MAX − Ta characteristics.

Package Power Dissipation



① INFINITE HEAT SINK
: Rθj-c = 1°C/W

② When mounted on the board (74.2 × 114.3 × 1.6 mm, Cu20%), HEAT SINK (10 × 10 × 1 mm, Cu)
: Rθj-a = 17°C/W

③ When mounted on the board (74.2 × 114.3 × 1.6 mm, Cu20%)
: Rθj-a = 35°C/W

④ IC only
: Rθj-a = 53°C/W

Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol		Test Condition	Min	Typ.	Max	Unit
Current dissipation		I_{BB}		V_{BB} = 450 V	—	—	0.5	mA
		I_{CC}		V_{CC} = 15 V	—	5	10	
Current consumption of bootstrap		$I_{BS\ (ON)}$		V_{BS} = 15 V, high-side ON	—	210	410	μA
		$I_{BS\ (OFF)}$		V_{BS} = 15 V, high-side OFF	—	180	370	
Input current		$I_{IN(LA)}$		Vin = 5 V, LA	—	25	50	μA
		$I_{IN(Vsp)}$		Vin = 5 V, V_{sp}	—	35	70	
		$I_{IN(Idc)}$		Vin = GND, I_{dc}	—	-25	-50	
		$I_{IN(1)}$		Vin = 5 V, CW/CCW, FGC, SS	—	50	100	
Input voltage		V_{IN1}	H	CW/CCW, FGC, SS	V_{refout} − 1	—	V_{refout}	V
			L		0	—	0.8	
		V_{IN2}	H	FGC	4	—	V_{refout}	V
			M		2	—	3	
			L		0	—	1	
		$V_{SP(H)}$	T	Test mode for motor shipping SS=H	8.2	—	10	V
			H	PWM ON duty 95% SS=H	5.1	5.4	5.7	
			M	Refresh → Start motor operation, SS=H	1.8	2.1	2.4	
			L	Turned-off → Refresh SS=H	0.7	1.0	1.3	
		$V_{SP(L)}$	T	Test mode for motor shipping SS=L	8.2	—	10	V
			H	PWM ON duty 92% SS=L	5.1	5.4	5.7	
			M	Refresh → Start motor operation, SS=L	1.8	2.1	2.4	
			L	Turned-off → Refresh SS=L	0.7	1.0	1.3	
PWM oscillation frequency (Carrier frequency)		$F_{C\ (20)}$		OSC/R = 68 kΩ	18	20	22	kHz
		$F_{C\ (18)}$		OSC/R = 75 kΩ	16.2	18	19.8	
Motor lock detection		TONTR		TR=0.01μF Driving time (Note)	3.33	5	8.33	s
		TOFFTR		TR=0.01μF Turn off time (Note)	20	30	46.15	s
		FTR		TR=0.01μF frequency	65	100	150	Hz
Lead angle offset (LA)		$T_{LAH(0)}$		LA = 0 V or open, Hall IN = 100 Hz SS=H	—	0	—	°
		$T_{LAH(2.5)}$		LA = 2.5 V, Hall IN = 100 Hz SS=H	11.25	15	18.75	
		$T_{LAH\ (5)}$		LA = 5 V, Hall IN = 100 Hz SS=H	26.25	28.125	—	
Lead angle offset		$T_{LAL(0)}$		LA = 0 V or Open, Hall IN = 100 Hz SS=L	—	0	—	°
		$T_{LAL\ (2.5)}$		LA = 2.5 V, Hall IN = 100 Hz SS=L	26	30	33	
		$T_{LAL\ (5)}$		LA = 5 V, Hall IN = 100 Hz SS=L	52	57	60	
Hall device input	Input sensitivity	V_S		Difference input	40	—	—	mVpp
	In-phase range	V_W			0.5	—	4.0	V

	Input hysteresis	$V_{H\ (1)}$	(Note)	±1.5	±7.5	±13.5	mV
Hall IC input		V_{IN4} H	HUP, HVP, HWP: HUM,HVM,HWM=Vrefout/2	V_{refout} − 1	—	V_{refout}	V
		V_{IN4} L		0	—	0.8	
Current detection		V_{dc}	$I_{dc,}$	0.475	0.5	0.525	V
Output voltage		$V_{FG\ (H)}$	I_{OUT} = 2 mA FG	4	—	—	V
		$V_{FG\ (L)}$	I_{OUT} = −2 mA FG	—	—	1	
		$V_{refout1}$	I_{OUT} = 15 mA V_{refout}	4.7	5.0	5.3	
		$V_{refout2}$	I_{OUT} = 35 mA V_{refout}	4.5	5.0	5.3	
		V_{reg}	I_{OUT} = 30 mA V_{reg}	6.5	7	7.5	
Output saturated voltage		$V_{CEsat}H$	V_{CC} = 15 V, IC = 1 A, High side	—	2.3	3.2	V
		$V_{CEsat}L$	V_{CC} = 15 V, IC = 1 A, Low side	—	2.3	3.2	
Forward voltage of FRD		$V_F H$	I_F = 1 A, High side	—	2.1	3.1	V
		$V_F L$	I_F = 1 A, Low side	—	2.1	3.1	
Forward voltage of BSD		$V_{F\ (BSD)}$	I_F = 500 μA	—	0.9	1.2	V
Over heat protection		TSD	(Note)	135	—	185	°C
		TSDhys		—	50	—	
V_{CC} Undervoltage lockout (Driver)		V_{CC} (H)	Undervoltage positive-going threshold	10.5	11.5	12.5	V
		V_{CC} (L)	Undervoltage negative-going threshold	10	11	12	
VBS Undervoltage lockout (Driver)		VBS (H)	Undervoltage positive-going threshold	8.5	9.5	10.5	V
		VBS (L)	Undervoltage negative-going threshold	8	9	9.5	
Output delay time		t_{on}	V_{BB} = 280 V, V_{CC} = 15 V, I_C = 1 A	—	1.2	3	μs
		t_{off}	V_{BB} = 280 V, V_{CC} = 15 V, I_C = 1 A	—	1	3	
Input delay time		T_{DC}	I_{dc} (f_{osc} = 5 MHz)	—	3.5	—	μs
FRD reverse recovery time		t_{rr}	V_{BB} = 280 V, V_{CC} = 15 V, I_C = 1 A	—	150	—	ns

(Note): Toshiba does not implement testing before shipping.

Functional Description

1. Basic operation

The motor is driven by 120° commutation. When the positional signal reaches number of rotations f = 1 Hz or higher, the rotor position is estimated according to the positional signal and the motor is driven with the lead angle based on the input voltage of the LA pin.

From start to 1 Hz: Driven by square wave (120° commutation)

1Hz or higher: Driven by sine-wave PWM (180° commutation) or wide-angle commutation (150° commutation)

When fosc = 5MHz, approx. 1 Hz.

*: When f is 1Hz or higher, the motor is driven by the command of the LA pin.
When f is 1Hz or less or the motor is driven with reverse rotation direction (according to the timing chart), it is driven by 120° commutation (lead angle is 0°).

Driven system (sine-wave PWM or wide-angle commutation) can be switched by the SS pin. Setting of lead angle is different between these driving systems.

SS	Driving system	Lead angle
Low	Sine-wave PWM drive (180° commutation)	0 to 58° / 32 steps
High	Wide-angle commutation (150° commutation)	0 to 28° / 16 steps

2. Voltage Command (V_{SP}) Signal and Bootstrap Voltage Regulation

SS=L

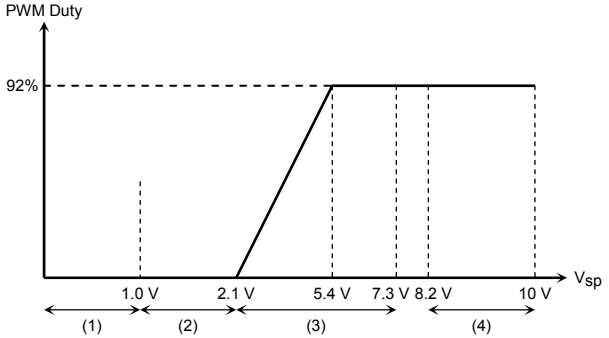
(1) When $V_{SP} \leq 1.0$ V:
The commutation signal outputs are disabled (i.e., gate protection is activated).

(2) When $1.0\ V < V_{SP} \leq 2.1$ V:
The low-side transistors are turned on at a regular (PWM carrier) frequency. (ON duty: 18/fosc)

(3) When $2.1\ V < V_{SP} \leq 7.3$ V:
During sine-wave PWM drive, the commutation signals directly appear externally. During square-wave drive, the low-side transistors are forced on at a regular (PWM carrier) frequency. (ON duty: 18/fosc)
In stop state (Forward: 1Hz or less, Reverse: 5Hz or less), commutation signals are outputted after V_{SP} ($V_{SP} > 2.1$ V) is inputted and the refresh function operates for 1.5ms (typ.). In operation state (Forward: more than 1Hz, Reverse: more than 5Hz), commutation signals are outputted after V_{SP} ($V_{SP} > 2.1$ V) is inputted.

Note: In startup, low-side transistor should be turned on ($1.0\ V < V_{SP} \leqq 2.1$ V) for a certain period to charge gate power supply of high-side transistors.

(4) When $8.2\ V \leq V_{SP} \leq 10$ V (test mode for motor shipping):
The TB67B000HG drives in sine-wave drive mode with lead angle of zero. However, it drives in square-wave mode in detecting reverse rotation.
When V_{SP} reaches 7.9 V (typ.), lead angle switches to zero.
The PWM duty cycle is calculated as *PWM_carrier_frequency* × 92% (typ.) and kept the constant value (5.4 V(typ.) ≤ V_{SP}).



SS=H

(1) When $V_{SP} \leq 1.0$ V:
The commutation signal outputs are disabled (i.e., gate protection is activated).

(2) When $1.0 \text{ V} < V_{SP} \leq 2.1$ V:
The low-side transistors are turned on at a regular (PWM carrier) frequency. (ON duty: 18/fosc)

(3) When $2.1 \text{ V} < V_{SP} \leq 7.3$ V:
During wide-angle commutation, the commutation signals directly appear externally. During square-wave drive, the low-side transistors are forced on at a regular (PWM carrier) frequency. (ON duty: 18/fosc)
In stop state (Forward: 1Hz or less, Reverse: 5Hz or less), commutation signals are outputted after V_{SP} ($V_{SP} > 2.1$ V) is inputted and the refresh function operates for 1.5ms (typ.). In operation state (Forward: more than 1Hz, Reverse: more than 5Hz), commutation signals are outputted after V_{SP} ($V_{SP} > 2.1$ V) is inputted.

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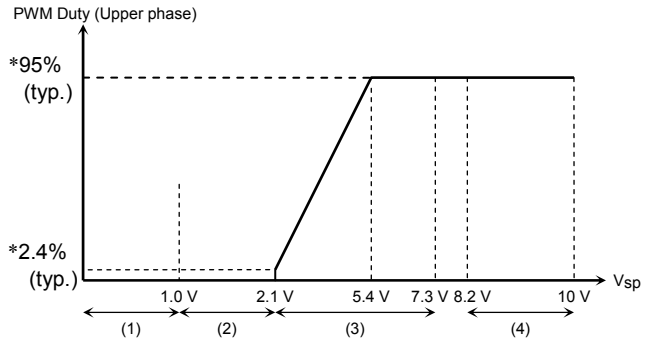
When V_{SP} reaches 7.9 V (typ.), lead angle switches to zero.
The PWM duty cycle is calculated as *PWM_carrier_frequency* × 95% (typ.) and kept the constant value ($5.4 \text{ V} \leq V_{SP}$ (typ.)).



*: Maximum ON duty: Ton = 95% (typ.) when V_{SP} = 5.4 V (typ.)
Minimum ON duty: Ton = 2.4% (typ.) when V_{SP} = 2.1 V (typ.).

Ex.: When f_{osc} = 5 MHz, maximum ON time = 48 μs (typ.) (f_C = 19.8 kHz)
minimum ON time = 1.2 μs (typ.) (f_C = 19.8 kHz)

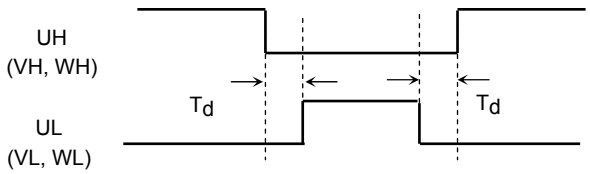
3. Dead Time Insertion (cross conduction protection)

To prevent a short-circuit between external low-side and high-side power elements during sine-wave PWM drive, a dead time is digitally inserted between the turn-on of one side and the turn-off of the other side. (The dead time is also implemented at the full duty cycle during square-wave drive.)

$T_d = 9/f_{osc}$

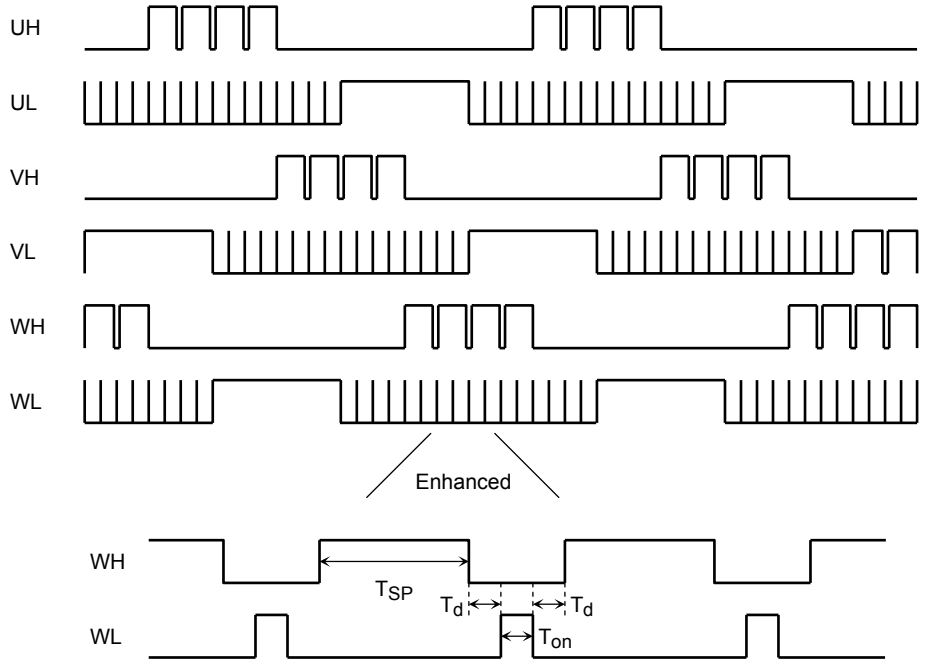
When f_{osc} = 5 MHz, T_d ≃ 1.8 μsec ($9/f_{osc}$)

f_{osc} = reference clock (CR oscillation frequency)



When input voltage (V_{SP}) is more than 2.1 V and the hall signal frequency is 1Hz or less, the upper phase (UH, VH, and WH) operates PWM drives (according to V_{SP}) with120° commutation. And the lower phase (UL, VL, and WL) operates with 120° commutation. It refreshes in off timing. (In case of reverse direction drive, the operation is the same as forward direction drive.)

Output waveform (Image)



T_{SP}: Changeable by V_{SP}. (The condition in this figure: V_{SP} = 5.4 V (typ.)), $T_{on} = 18/f_{osc}$, $Td = 9/f_{osc}$.

*: Lead angle offset (LA pin) is not activated when hall signal frequency is 1 Hz or less. The lead angle is also deactivated in detecting of reverse rotation.

4. Lead Angle Control

The lead angle can be adjusted between 0° and 58° according to the induced voltage level on the LA input.

SS=L

LA analog input (0 to 5 V in 32 separate steps.)
0 V = 0°
5 V = 58° (A lead angle of 58° is assumed when the LA voltage exceeds 5 V.)

SS=H

LA analog input (0 to 5 V in 16 separate steps).
0 V = 0°
5 V = 28° (A lead angle of 28° is assumed when the LA voltage exceeds 5 V.)

5. PWM Carrier Frequency

The triangular waveform generator provides a carrier frequency of $f_{osc}/252$ necessary for PWM generation. (The triangular wave is also used to force the switch-on of low-side transistors during square-wave drive.)

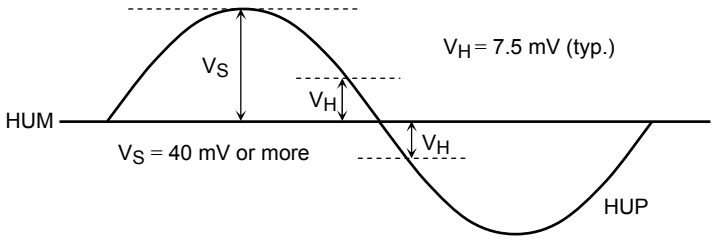
Carrier frequency: $F_C = f_{osc}/252$ (Hz),

where f_{osc} = reference clock (crystal oscillator) frequency

6. Position Detecting Pin

<Hall device input>

V_W is 0.5 to 4.0 V in in-phase range. Input hysteresis voltage (V_H) is 7.5 mV (typ.).



<Hall IC input>

Usage conditions: HUP, HVP, and HWP = GND to Vrefout

HUM, HVM, and HWM = Vrefout / 2

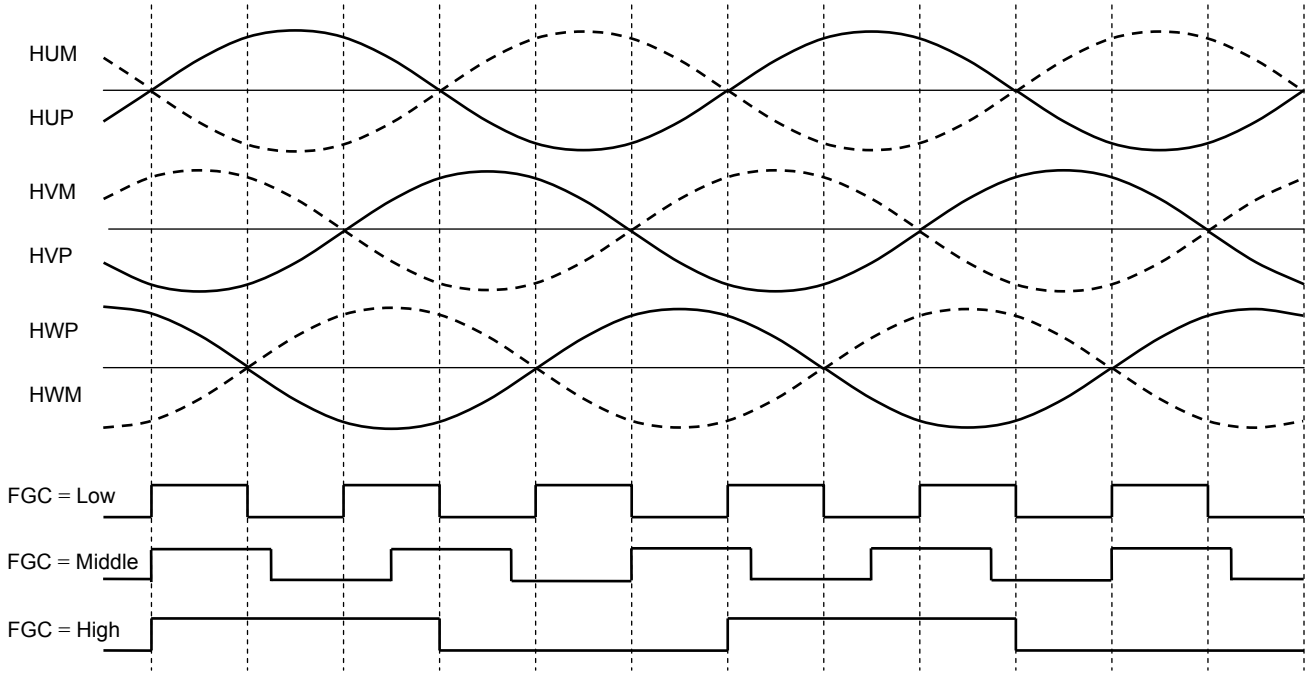
7. Rotating Pulse Output

The TB67B000HG outputs rotating pulse based on hall signal. FGC terminal can switch one pulse per electrical angle or 3 pulses per electrical angle. One pulse per electrical angle is generated from hall signal of U phase. 3 pulses per electrical angle are generated by combining each rising and falling edge of U, V, and W phases.

When the pulse is outputted at 2.4 pulses per electrical angle (FGC=M), FG terminal outputs L level under the condition that the direction of motor rotating is forward or reverse at 1Hz or less. It is outputted regardless of the input voltage of Vsp.

FGC	FG
High	1 pulse per electrical angle
Middle	2.4 pulse per electrical angle (2 pulse per 5/6 electrical angle)
Low	3 pulses per electrical angle

Timing Chart of FG Signal



8. Protection-Related Input Pins

(1) Overcurrent protection(I_{dc} pin)

If the voltage of the DC-link current exceeds the internal reference voltage, the gate block is activated and the commutation signals (U, V, and W) are forced Low. Overcurrent protection is disabled after every carrier period under the condition that the voltage is 0.5 (typ.).

Reference voltage = 0.5 V (typ.)

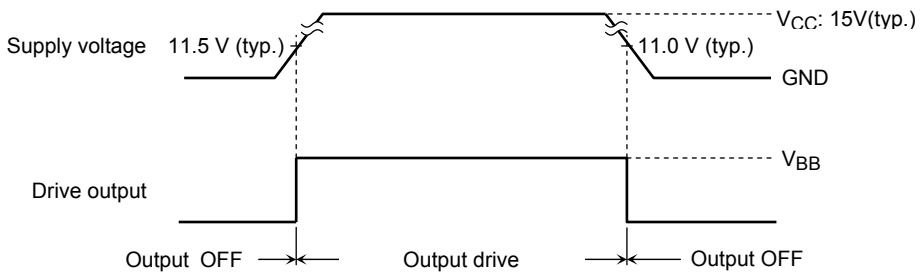
(2) Abnormal position signal protection

When the position detection signals (internal hall sensor outputs) are all Highs or all Lows, or position input signals (HUP, HUM, HVP, HVM, HWP, and HWM) are all open, the commutation outputs (U, V, and W) are forced off. When these inputs are then set to any other combination, the commutation outputs are re-enabled.

(3) Undervoltage lockout (V_{CC})

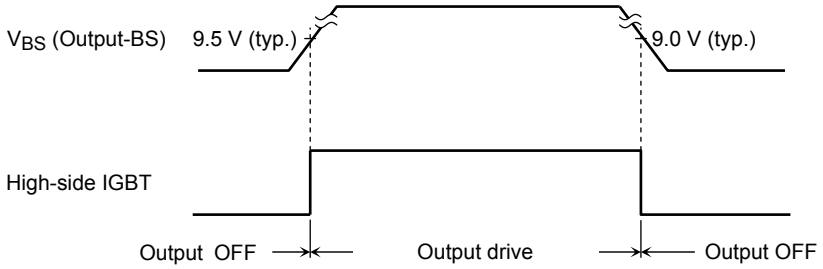
While the power supply voltage is outside the rated range during power-on or power-off, the commutation outputs (U, V, and W) are set to the high-impedance state to prevent external power elements from damage due to short-circuits.

<V_{CC}>



(4) Monitor for V_{BS} bootstrap power supply

When V_{BS} power supply falls, high-side of IGBT output is turned off.



(5) Thermal shutdown circuit

When chip temperature rises high abnormally because of internal or external heat generation, all outputs of IGBT are tuned off.

T_{SD} = 135(min.), 185°C (max.) T_{SDhys} = 50°C (typ.)

Recovery temperature after TSD: T_{SD} -T_{SDhys}

9. Motor-lock detection

When hall signal detects below state, intermitted operation (drive period: stop period = 1: 6) is repeated.

<Description of motor-lock detection>

Motor lock detection starts counting (drive period) when V_{SP} exceeds 2.1 V. When direction of motor rotation and setting direction are the same (forward direction: sine-wave PWM mode or wide-angle commutation mode), lock detection drives with 120° commutation (square-wave drive) under the condition that frequency of the hall signal is about 1 Hz or less (when f_{osc} = 5MHz).

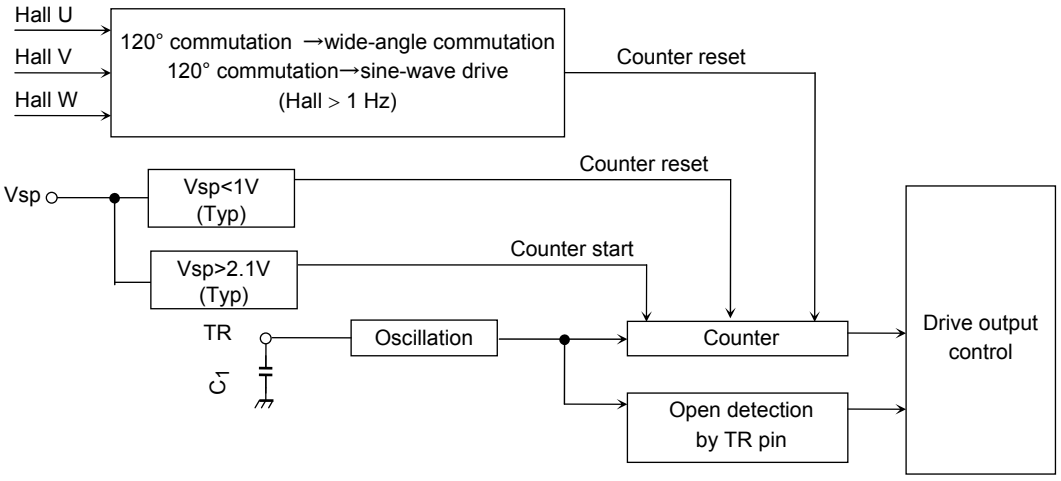
When direction of motor rotation is opposed against setting direction (reverse direction: 120° commutation mode of reverse hall input), lock detection drives under the condition that frequency of the hall signal is about 5 Hz or less (when f_{osc} = 5MHz).

When lock detection enables, operation is turned off (output drive is OFF) during stop period.

When V_{SP} is set 1.0 V or less, counter is reset and remove stop state. Then, when V_{SP} is set 2.1 V or more again, counter starts counting from initial state.

Table of lock detection

CW/CCW pin	Vsp pin > 2.1V		Vsp pin ≤2.1V
	Direction of motor rotation		-
	CW	CCW	
High(CW)	f_{osc} ≤ 1Hz (Rotating direction: set of CW/CCW pin = motor)	f_{osc} ≤ 5Hz (Rotating direction: set of CW/CCW pin ≠ motor)	Inactive
Low(CCW)	f_{osc} ≤ 5Hz (Rotating direction: set of CW/CCW pin ≠ motor)	f_{osc} ≤ 1Hz (Rotating direction: set of CW/CCW pin = motor)	Inactive



<Setting method>

Time of detection and stop outputting can be determined by an external capacitor (C_1) of TR pin.

・Setting period

Drive period Ton[s] =C1× (VH—VL) ×2/I×500 counts

Stop period Toff[s] =C1× (VH—VL) ×2/I×3000 counts (Note 1)

- Ex.: When C1 = 0.01μF, I = 3μA (typ.), VH= 2 V (typ.) and VL= 0.5V (typ.), and then Ton[s] =5s (typ.) and Toff[s] =30s (typ.).

Note 1: Bootstrap capacitor does not charge (refresh) during stop period.
To charge bootstrap capacitor in recovery, Vsp should be set as follows by voltage command input; 1.0 V < V_{sp} ≦ 2.1 V.

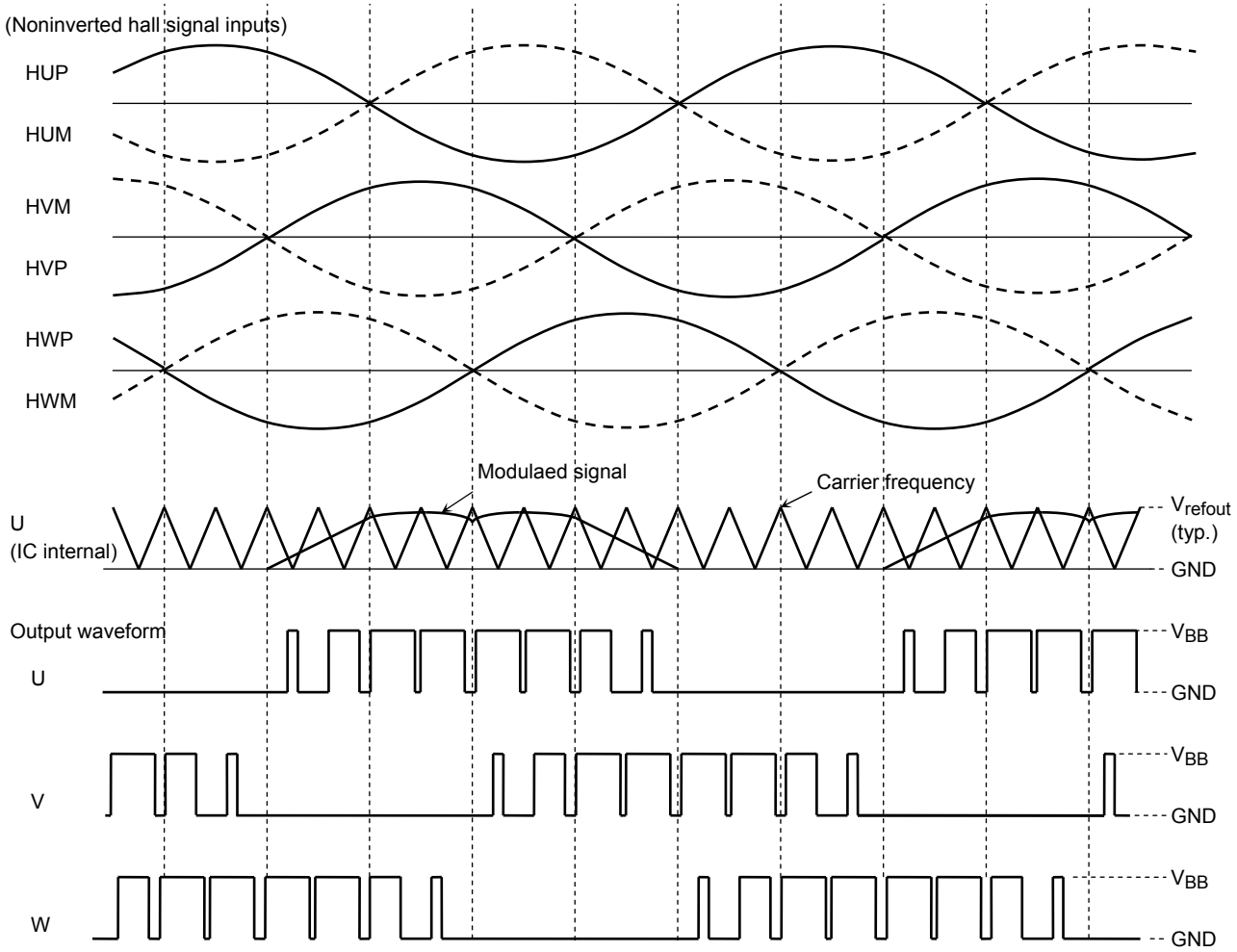
Note 2: When TR pin is open, the operation moves to stop mode (drive output OFF) by open detection.

Note 3: Counter is not activated by applying fixed voltage (GND) to the TR pin. And motor lock detection is turned off and drive mode can be continued.

Timing Chart

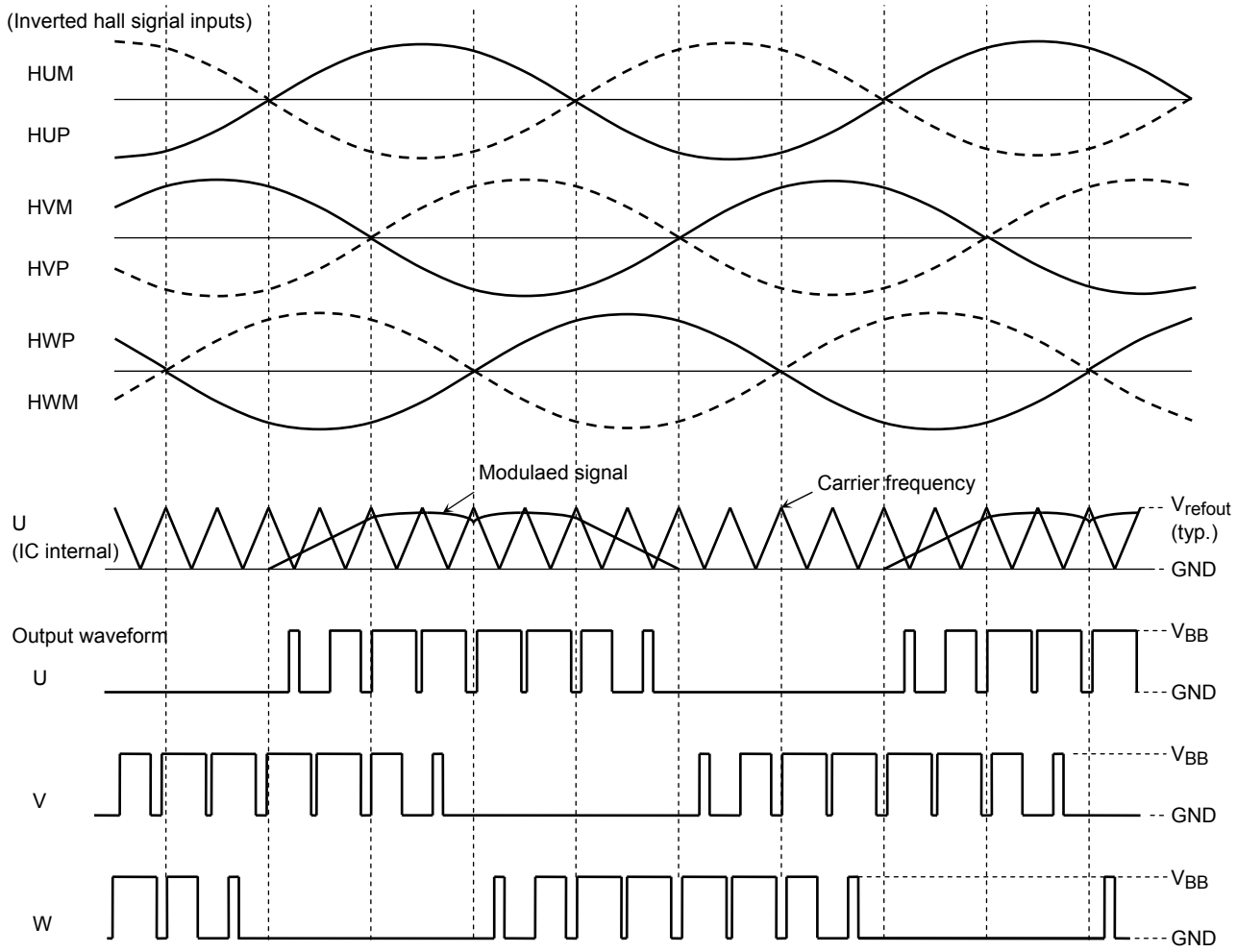
CW/CCW	SS	Hall input (frequency)	Drive method	No.
H	H	CW (1Hz or less)	Square-wave drive (120° commutation)	5
		CW (1Hz or higher)	Wide-angle commutation (150° commutation)	3
		CCW	Square-wave drive (120° commutation)	6
	L	CW (1Hz or less)	Square-wave drive (120° commutation)	5
		CW (1Hz or higher)	Sine-wave PWM drive (180° commutation)	1
		CCW	Square-wave drive (120° commutation)	6
L	H	CW	Square-wave drive (120° commutation)	8
		CCW (1Hz or less)	Square-wave drive (120° commutation)	7
		CCW (1Hz or higher)	Wide-angle commutation (150° commutation)	4
	L	CW	Square-wave drive (120° commutation)	8
		CCW (1Hz or less)	Square-wave drive (120° commutation)	7
		CCW (1Hz or higher)	Sine-wave PWM drive (180° commutation)	2

Timing Chart 1: Output waveform of sine-wave PWM drive
(CW/CCW = High, SS = Low, LA = GND, Noninverted hall signal inputs)



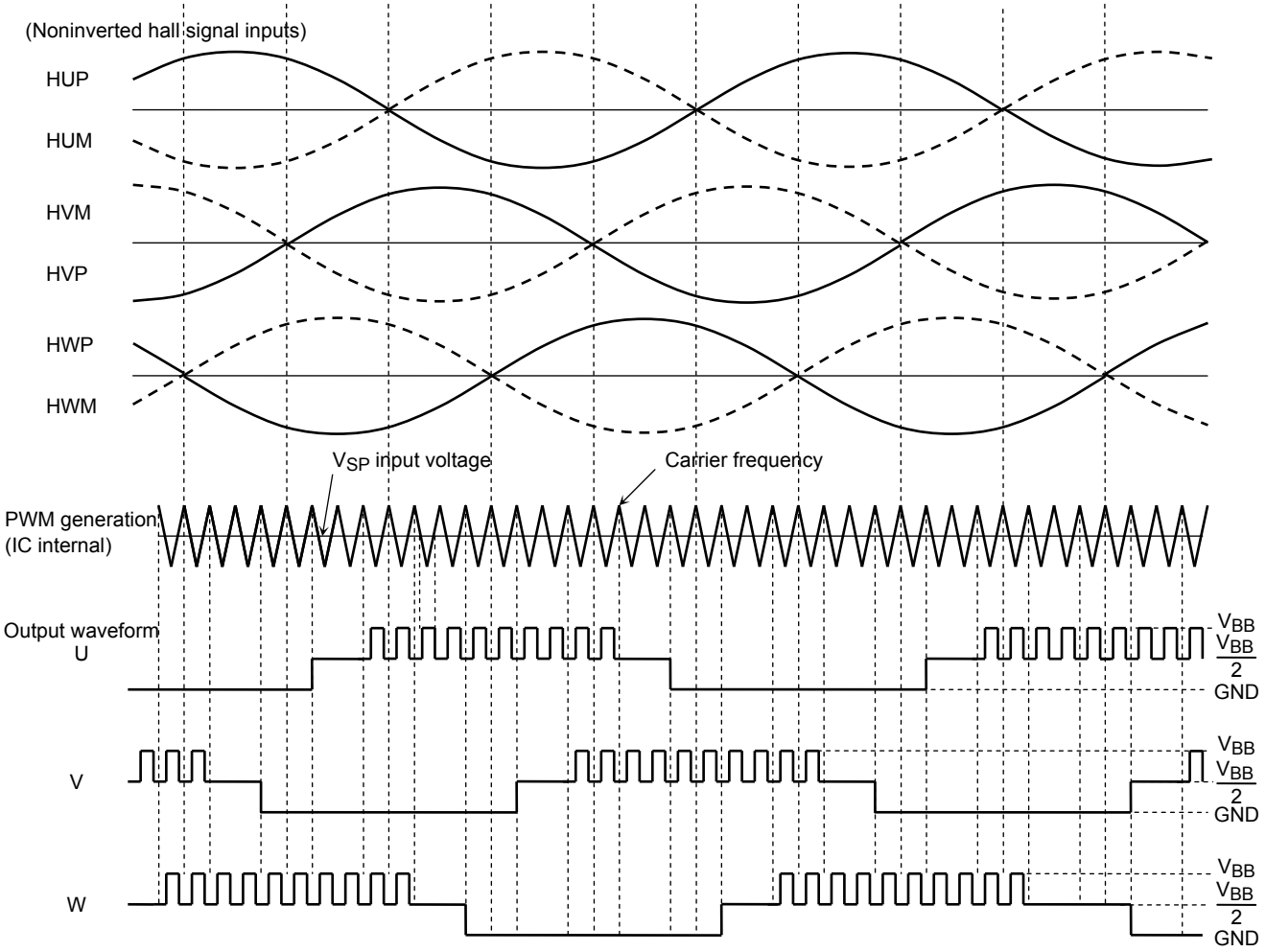
Note: The above timing chart is simplified to illustrate the function and behavior of the device.

Timing Chart 2: Output waveform of sine-wave PWM drive
(CW/CCW = Low, SS = Low, LA = GND, Inverted hall signal inputs)



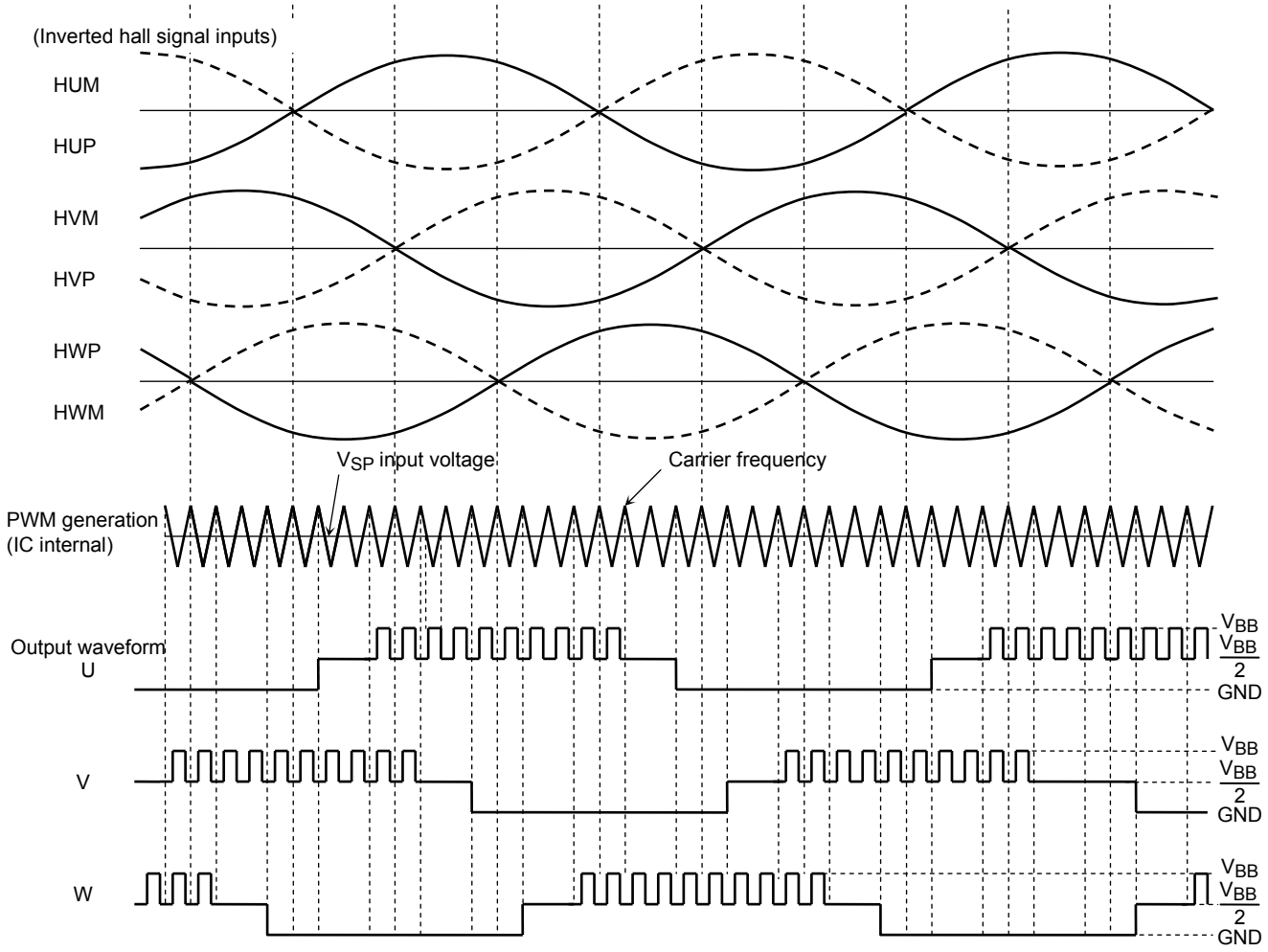
Note: The above timing chart is simplified to illustrate the function and behavior of the device.

Timing Chart 3: Output waveform of wide-angle commutation
(CW/CCW = High, SS = High, LA = GND, Noninverted hall signal inputs)



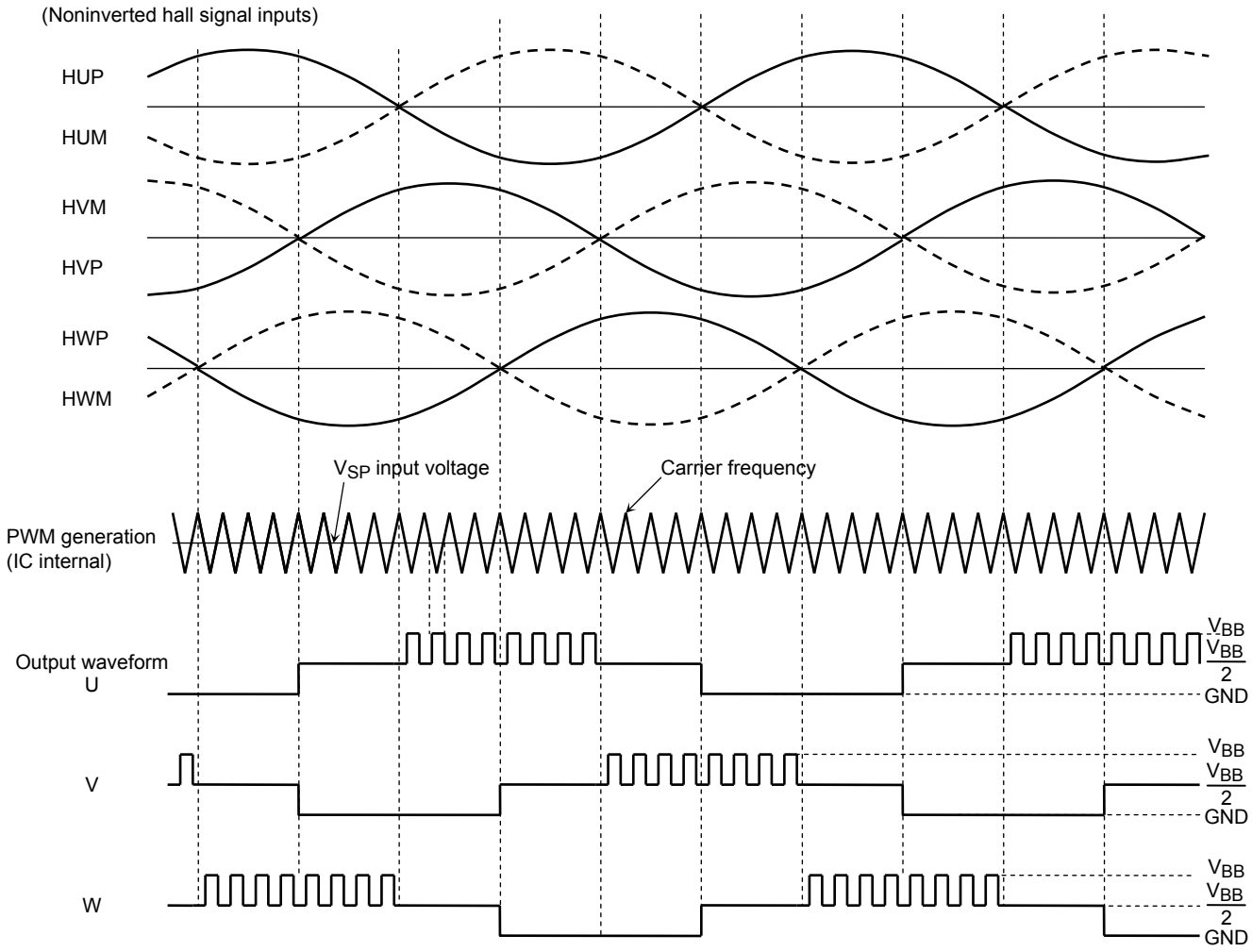
Note: The above timing chart is simplified to illustrate the function and behavior of the device.
The above U-phase waveform shows the behavior of the U-phase output signal when a resistor is connected between the U and VM pins and also between the U pin and ground to obtain $\frac{V_{BB}}{2}$. Likewise, resistors are connected to the V and W pins. $\frac{V_{BB}}{2}$ indicates the high-impedance state.

Timing Chart 4: Output waveform of wide-angle commutation
(CW/CCW = Low, SS=High, LA = GND, Inverted hall signal inputs)



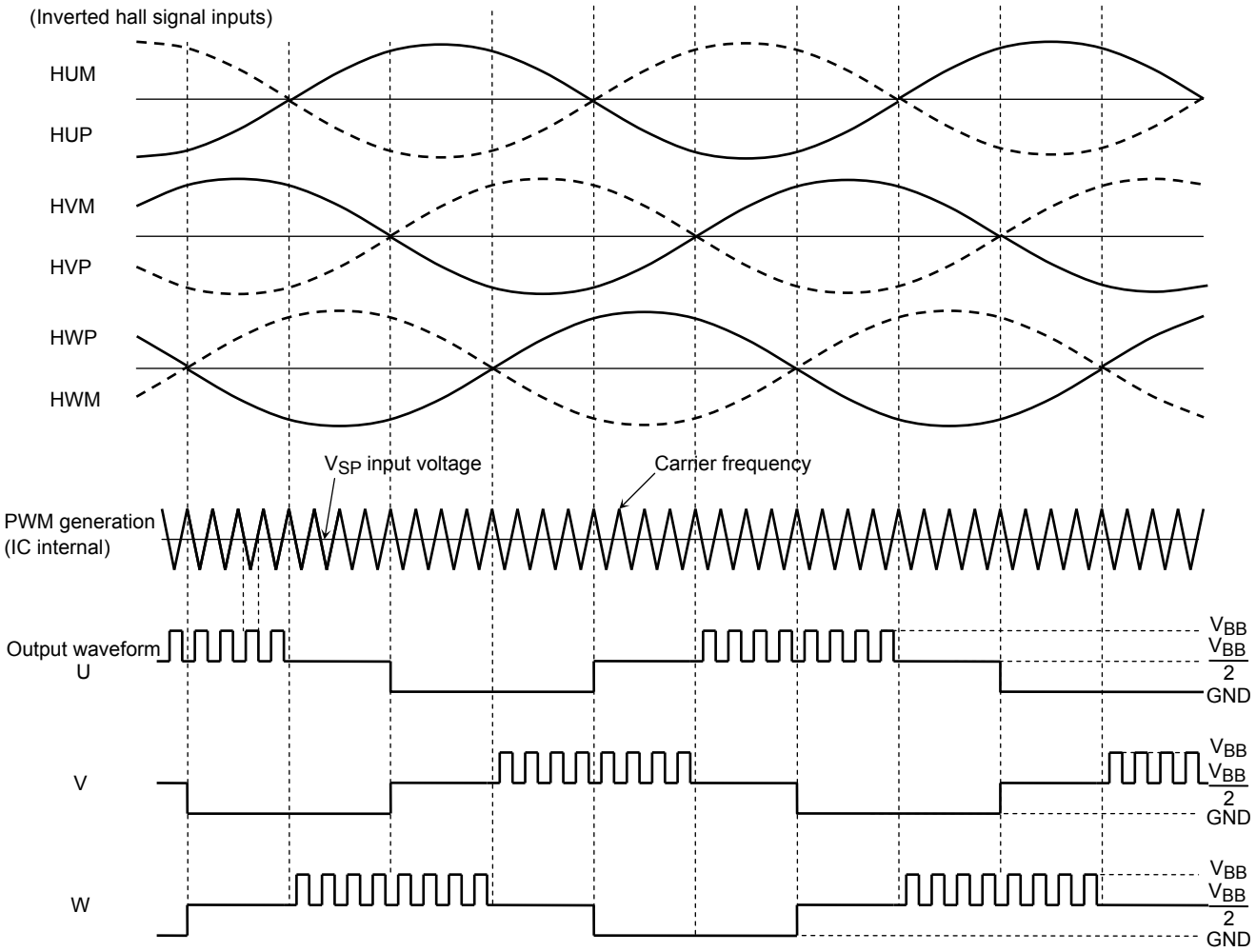
Note: The above timing chart is simplified to illustrate the function and behavior of the device.
The above U-phase waveform shows the behavior of the U-phase output signal when a resistor is connected between the U and VM pins and also between the U pin and ground to obtain $\frac{V_{BB}}{2}$. Likewise, resistors are connected to the V and W pins. $\frac{V_{BB}}{2}$ indicates the high-impedance state.

Timing Chart 5: Output waveform of square-wave drive
(CW/CCW = High, LA = GND, Noninverted hall signal inputs)



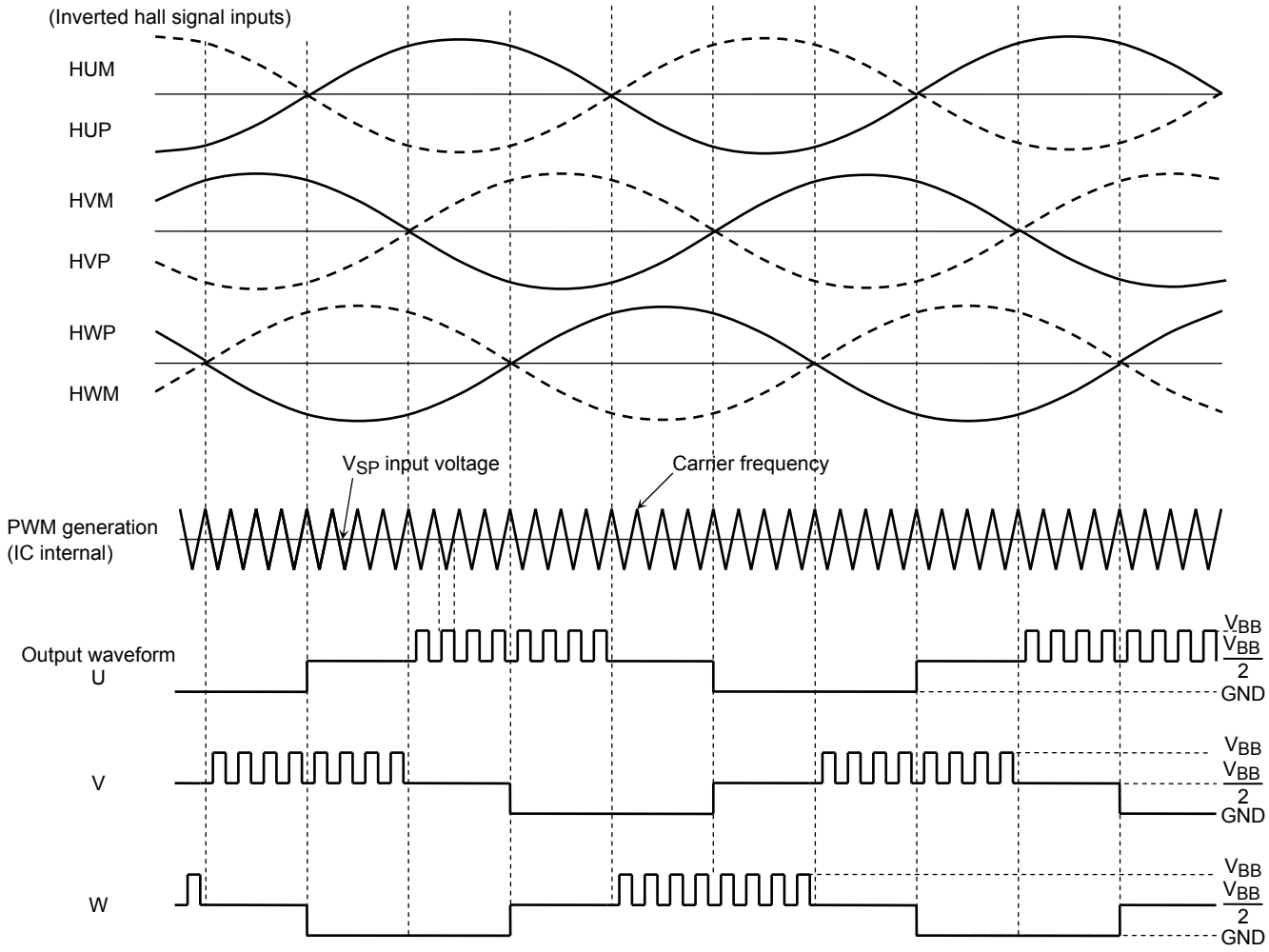
Note: The above timing chart is simplified to illustrate the function and behavior of the device.
The above U-phase waveform shows the behavior of the U-phase output signal when a resistor is connected between the U and VM pins and also between the U pin and ground to obtain $\frac{V_{BB}}{2}$. Likewise, resistors are connected to the V and W pins. $\frac{V_{BB}}{2}$ indicates the high-impedance state.

Timing Chart 6: Output waveform of square-wave drive
(CW/CCW = High, LA = GND, Inverted hall signal inputs)



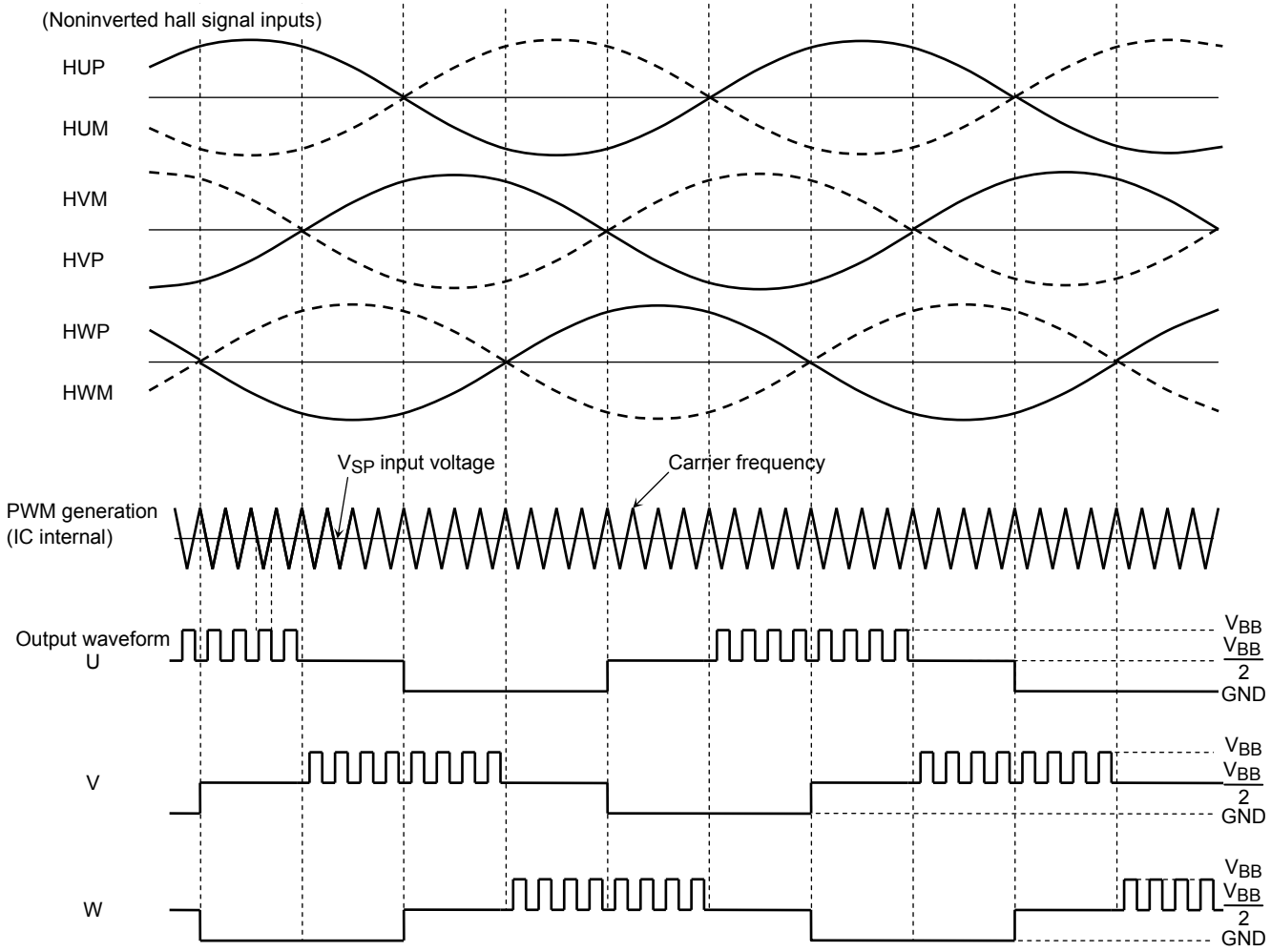
Note: The above timing chart is simplified to illustrate the function and behavior of the device.
The above U-phase waveform shows the behavior of the U-phase output signal when a resistor is connected between the U and VM pins and also between the U pin and ground to obtain $\frac{V_{BB}}{2}$. Likewise, resistors are connected to the V and W pins. $\frac{V_{BB}}{2}$ indicates the high-impedance state.

Timing Chart 7: Output waveform of square-wave drive
(CW/CCW = Low, LA = GND, Inverted hall signal inputs)



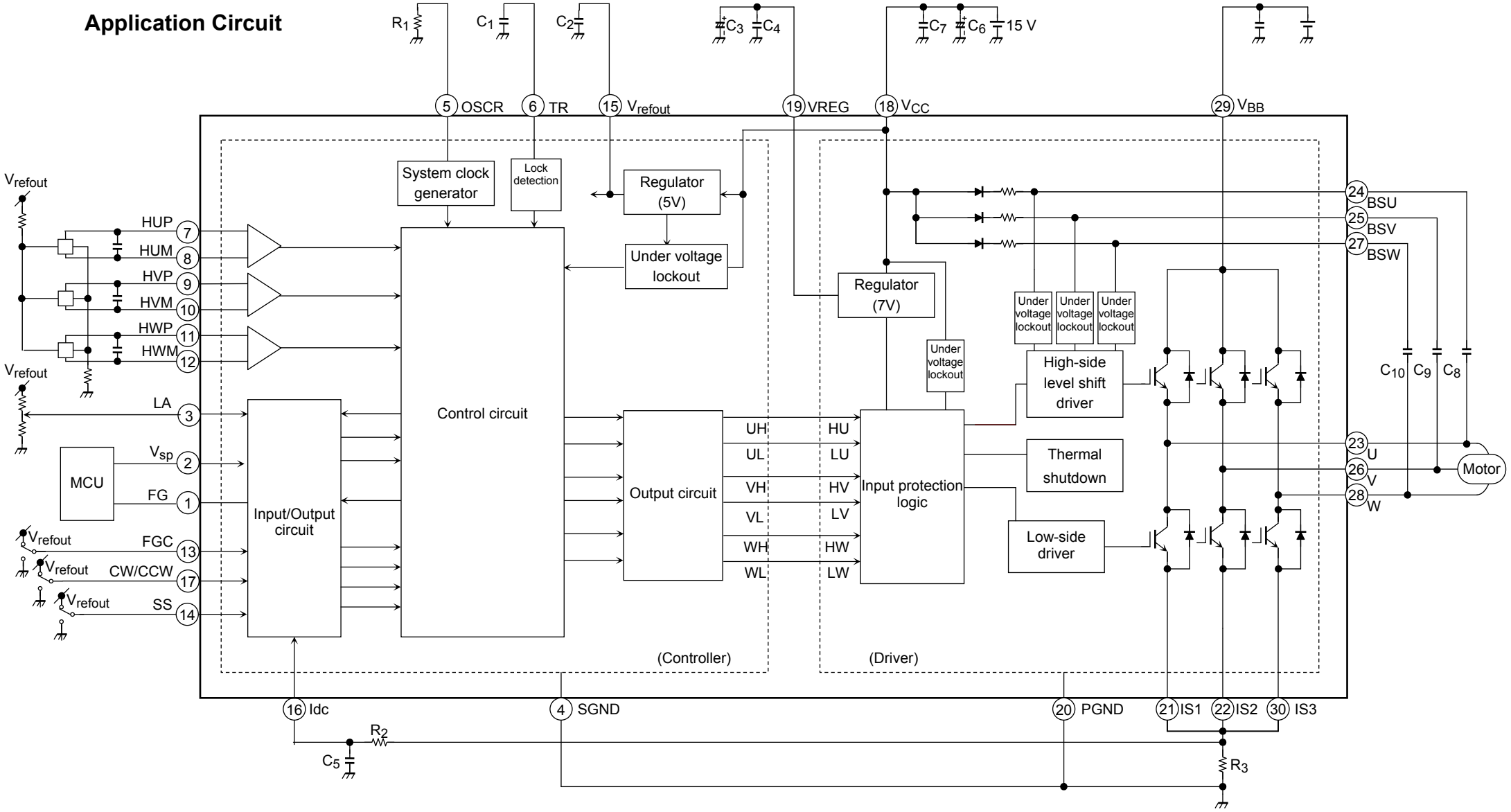
Note: The above timing chart is simplified to illustrate the function and behavior of the device.
The above U-phase waveform shows the behavior of the U-phase output signal when a resistor is connected between the U and VM pins and also between the U pin and ground to obtain $\frac{V_{BB}}{2}$. Likewise, resistors are connected to the V and W pins. $\frac{V_{BB}}{2}$ indicates the high-impedance state.

Timing Chart 8: Output waveform of square-wave drive
(CW/CCW = Low, LA = GND, Noninverted hall signal inputs)



Note: The above timing chart is simplified to illustrate the function and behavior of the device.
The above U-phase waveform shows the behavior of the U-phase output signal when a resistor is connected between the U and VM pins and also between the U pin and ground to obtain $\frac{V_{BB}}{2}$. Likewise, resistors are connected to the V and W pins. $\frac{V_{BB}}{2}$ indicates the high-impedance state.

Application Circuit



Utmost care is necessary in the design of board layout since the IC may be destroyed and cause smoke or ignition by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous pins. Specially, in the design of the output, V_{BB}, U, V, W, IS1, IS2, IS3 and GND lines which have high voltage and high current, utmost care is necessary. Add overcurrent protection such as a fuse not to allow large current continuing to flow in case of over current generation or IC breakdown.

External Parts

Symbol	Purpose	Recommended value	Note
R_1	Internal clock generation	68 kΩ	(Note 1)
C_1	Motor lock detection	10 V / 0.01 μF	(Note 2)
C_2	V_{refout} oscillation protection	10 V / 0.1 μF to 1.0 μF	(Note 3)
C_3	V_{REG} power supply stability	25 V / 1 μF	(Note 3)
C_4		25 V / 1000 pF	
C_5	Noise absorber	10 V / 1000pF	(Note 4)
R_2		5.1 kΩ	
R_3	Overcurrent detection	0.62 Ω ± 1% (1 W)	(Note 5)
C_6	V_{CC} power supply stability	25 V / 10 μF	(Note 3)
C_7		25 V / 0.1 μF	
C_8, C_9, C_{10}	Bootstrap capacitor	25 V / 2.2 μF	(Note 6)

Note 1: For carrier frequency and dead time, determin the resistor to set the oscillation frequency of 6.4 MHz or less.

Note 2: This part sets the output stop period and output drive period of motor lock detection. When this function is not used, connect it to GND. As for detailed descriptions, please refer to the section of “Motor Lock Detection” in this document.

Note 3: This part is used as a capacitor for power supply stability. Adjust the part to the application environment as required. When mounting, place it as close as possible to the base of the leads of this product to improve the noise elimination.

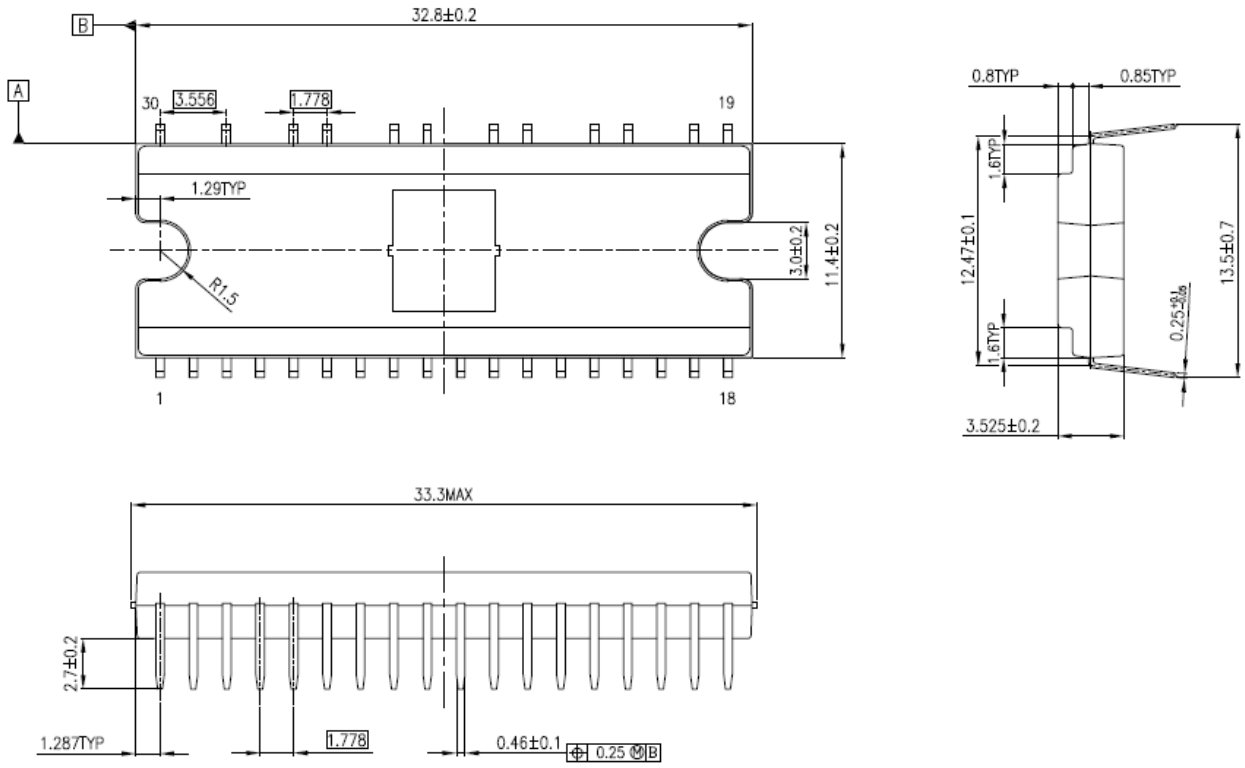
Note 4: These parts are used as a low-pass filter for noise absorption. Test to confirm noise filtering, then set the filter time-constant.

Note 5: This part is used to set the value for overcurrent detection. $I_{out\ (max)} = V_{dc} \div R_3$ (V_{dc} = 0.5 V (typ.))

Note 6: The required bootstrap capacitance value varies according to the motor drive conditions. The voltage stress for the capacitor is the value of V_{CC}.

Package Dimensions

Unit: mm



Weight: 2.59 g (typ.)

Note: Die pad on surface and PGND is connected. When using the heat sink, handle it not to short with the IC therminals. When applying the different potential with GND level to the heat sink, insulate with die pad and the heat sink.

Notes on Contents

1. Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts
Timing charts may be simplified for explanatory purposes.

4. Application Circuits
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits
Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations
Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time. Utmost care is necessary in the design of board layout since the IC may be destroyed and cause smoke or ignition by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous pins. Specially, in the design of the output, V_{BB}, U, V, W, IS1, IS2, IS3 and GND lines which have high voltage and high current, utmost care is necessary.

[5] Die pad on surface and PGND is connected.
When using the heat sink, handle it not to short with the IC therminals. When applying the different potential with GND level to the heat sink, insulate with die pad and the heat sink.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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