TOSHIBA Field Effect Transistor Silicon P Channel MOS Type(U-MOSVI)

SSM6J501NU

Power Management Switch Applications

1.5V drive

Low ON-resistance: $R_{DS(ON)} = 43.0 \text{ m}\Omega \text{ (max) } (@V_{GS} = -1.5 \text{ V})$

 $R_{DS(ON)} = 26.5 \text{ m}\Omega \text{ (max) (@V_{GS} = -1.8 V)}$

 $R_{DS(ON)} = 19.0 \text{ m}\Omega \text{ (max) (@V_{GS} = -2.5 V)}$

 $R_{DS(ON)} = 15.3 \text{ m}\Omega \text{ (max) (@V_{GS} = -4.5 V)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V_{DSS}	-20	V	
Gate-Source voltage		V _{GSS}	±8	V	
Drain current	DC	ID	-10	Α	
	Pulse	I _{DP} (Note 1)	-30		
Dower discipation		P _D (Note 2)	1	W	
Power dissipation		t≦10s	2		
Channel temperature		T _{ch}	150	°C	
Storage temperature		T _{stg}	-55 to 150	°C	

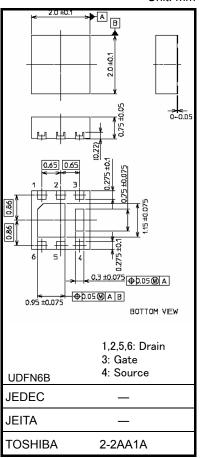
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

> Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The pulse width limited by max channel temperature.

Note 2: Mounted on an FR4 board. $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{ Cu Pad: } 645 \text{ mm}^2)$

Unit: mm



Weight: 8.5 mg (typ.)

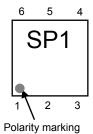
Marking(Top View)

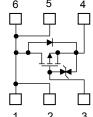
Drain

Polarity marking (on the top) *Electrodes: on the bottom

Pin Condition(Top View)

Equivalent Circuit(Top View)





Start of commercial production 2010-11

Source

Electrical Characteristics (Ta = 25°C)

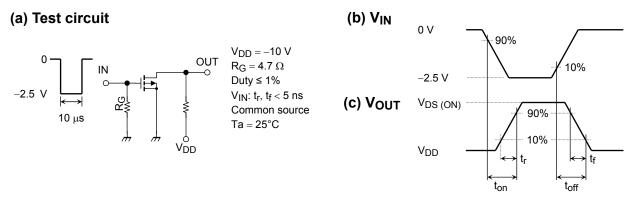
Chara	acteristic	Symbol	Test Conditions		Min	Тур.	Max	Unit		
Drain Course brookdown valtage	akdown voltago	V (BR) DSS	$I_D = -1 \text{ mA}, V_{GS} = 0 \text{ V}$		-20	_	_	V		
Drain-Source breakdown voltage		V (BR) DSX	$I_D = -1 \text{ mA}, V_{GS} = 5 \text{ V}$	(Note 4)	-15	_	_	v		
Drain cut-off current		I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V		_	_	-1	μΑ		
Gate leakage curr	ent	I _{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$		_	_	±1	μΑ		
Gate threshold vo	Itage	V _{th}	$V_{DS} = -3 \text{ V}, I_{D} = -1 \text{ mA}$		-0.3	_	-1.0	V		
Forward transfer a	admittance	Y _{fs}	$V_{DS} = -3 \text{ V}, I_{D} = -2.0 \text{ A}$	(Note 3)	11	22	_	S		
Drain-source ON-resistance		R _{DS} (ON)	$I_D = -4.0 \text{ A}, V_{GS} = -4.5 \text{ V}$	(Note 3)	_	12	15.3	· mΩ		
			I _D = -4.0 A, V _{GS} = -2.5 V	(Note 3)	_	14	19			
			I _D = -4.0 A, V _{GS} = -1.8 V	(Note 3)	_	17	26.5			
			I _D = -2.0 A, V _{GS} = -1.5 V	(Note 3)	_	20	43			
Input capacitance		C _{iss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz		_	2600	_	pF		
Output capacitance		Coss			_	290	_			
Reverse transfer capacitance		C _{rss}			_	280	_			
Total Gate Charge		Qg	V _{DD} = -10 V, I _D = -10 A V _{GS} = -4.5 V		_	29.9	_	nC		
Gate-Source Charge		Q _{gs1}			_	3.0	_			
Gate-Drain Charge		Q _{gd}			_	5.6	_			
Switching time	Turn-on time	t _{on}	$V_{DD} = -10 \text{ V}, I_D = -2.0 \text{ A},$		_	45.2	_			
	Turn-off time	t _{off}	$V_{GS} = 0 \text{ to } -2.5 \text{ V}, R_G = 4.7 \Omega$		_	201	_	ns		
Drain-Source forward voltage		V _{DSF}	I _D = 4 A, V _{GS} = 0 V	(Note 3)	_	0.70	1.1	٧		

Note 3: Pulse test

Note 4: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode.

Note that the drain-source breakdown voltage is lowered in this mode

Switching Time Test Circuit



Precaution

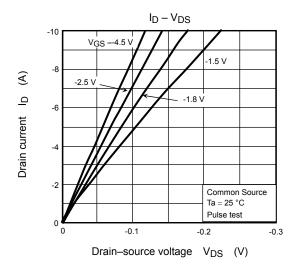
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (-1 mA for the SSM6J501NU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

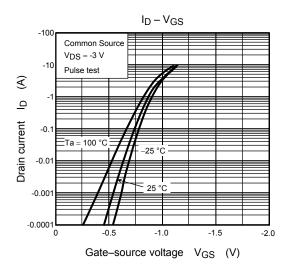
Take this into consideration when using the device.

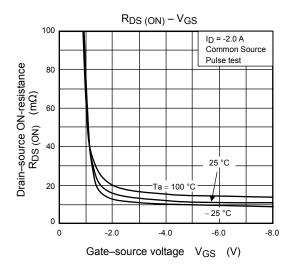
Handling Precaution

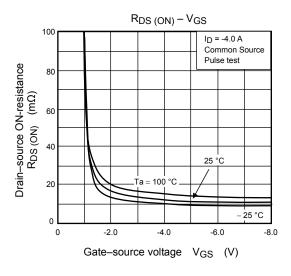
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

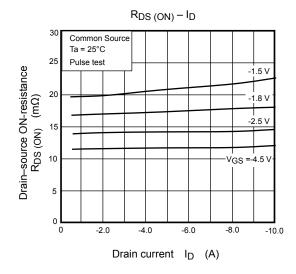
Thermal resistance R_{th} (ch-a) and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

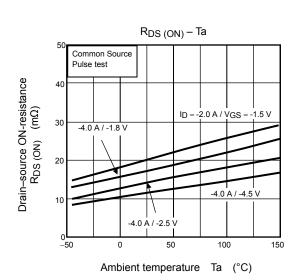




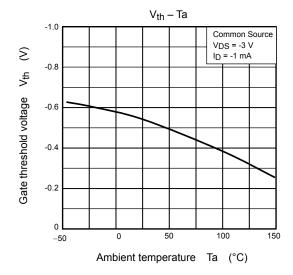


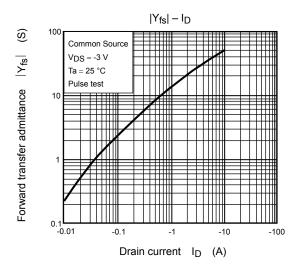


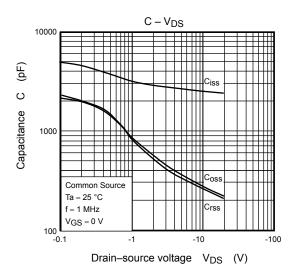


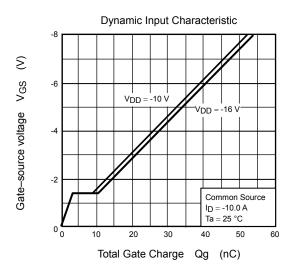


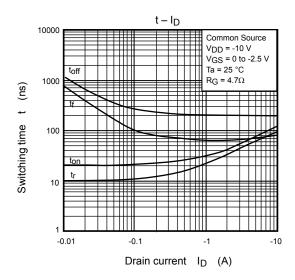
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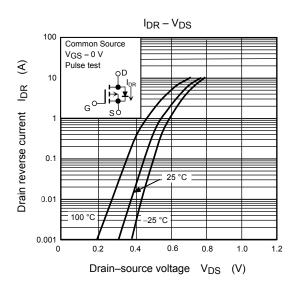




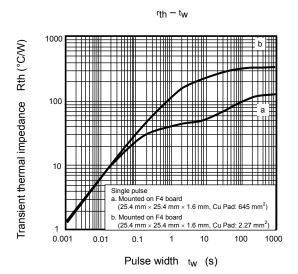


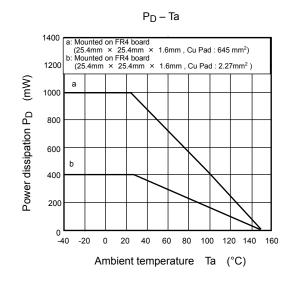






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