MOSFETs Silicon N-Channel MOS

SSM3K72CTC

1. Applications

- High-Speed Switching

2. Features

(1) ESD protected gate

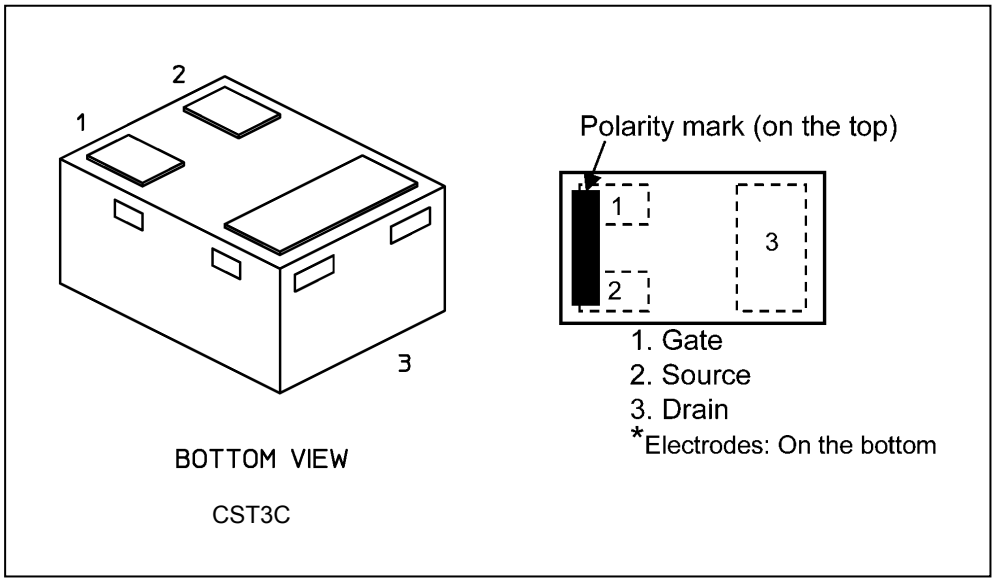
(2) Low drain-source on-resistance

: $R_{DS(ON)}$ = 2.8 Ω (typ.) (@V_{GS} = 10 V)

$R_{DS(ON)}$ = 3.1 Ω (typ.) (@V_{GS} = 5.0 V)

$R_{DS(ON)}$ = 3.2 Ω (typ.) (@V_{GS} = 4.5 V)

3. Packaging and Pin Assignment



Start of commercial production

2015-01

4. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	60	V
Gate-source voltage		V_{GSS}	±20	
Drain current (DC)	(Note 1)	I_D	150	mA
Drain current (pulsed)	(Note 1), (Note 2)	I_{DP}	600	
Power dissipation	(Note 3)	P_D	500	mW
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Repetitive rating; pulse width limited by maximum channel temperature.
pulse width ≤ 10 μs, Duty ≤ 1 %

Note 3: Device mounted on a 25.4 mm × 25.4 mm × 1.6 mm FR-4 glass epoxy board (Cu pad: 645 mm^2)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, $R_{th(ch-a)}$, and the drain power dissipation, P_D, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

5. Electrical Characteristics

5.1. Static Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±2	μA
		V_{GS} = ±10 V, V_{DS} = 0 V	—	—	±0.5	
		V_{GS} = ±5 V, V_{DS} = 0 V	—	—	±0.1	
Drain cut-off current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	—	—	1	μA
		V_{DS} = 60 V, V_{GS} = 0 V, T_{ch} = 150 °C	—	—	200	
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D = 250 μA, V_{GS} = 0 V	60	—	—	V
Gate threshold voltage	V_{th}	I_D = 250 μA, V_{DS} = V_{GS}	1.1	—	2.1	
Drain-source on-resistance (Note 1)	$R_{DS(ON)}$	I_D = 100 mA, V_{GS} = 10 V	—	2.8	3.9	Ω
		I_D = 100 mA, V_{GS} = 10 V, T_{ch} = 150 °C	—	5.4	8.1	
		I_D = 100 mA, V_{GS} = 5.0 V	—	3.1	4.4	
		I_D = 100 mA, V_{GS} = 4.5 V	—	3.2	4.7	
		I_D = 5 mA, V_{GS} = 2.5 V	—	5.7	—	
Forward transfer admittance (Note 1)	$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 200 mA	—	450	—	mS

Note 1: Pulse measurement.

5.2. Dynamic Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	11	17	pF
Reverse transfer capacitance	C_{rss}		—	0.7	—	
Output capacitance	C_{oss}		—	3	—	
Switching time (rise time)	t_r	V_{DD} = 40 V, I_D = 160 mA, V_{GS} = 0 to 10 V, R_G = 50 Ω, Duty ≤ 1 %, V_{IN}: t_r, t_f < 5 ns, Common source, See Chapter 5.3.	—	3	—	ns
Switching time (turn-on delay time)	$t_{d(on)}$		—	2	4	
Switching time (fall time)	t_f		—	24	—	
Switching time (turn-off delay time)	$t_{d(off)}$		—	7	14	

5.3. Switching Time Test Circuit

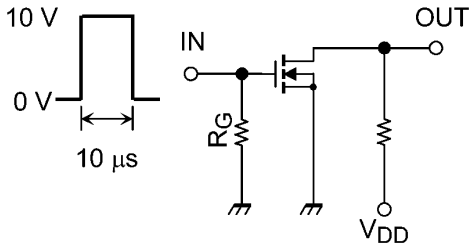


Fig. 5.3.1 Switching Time Test Circuit

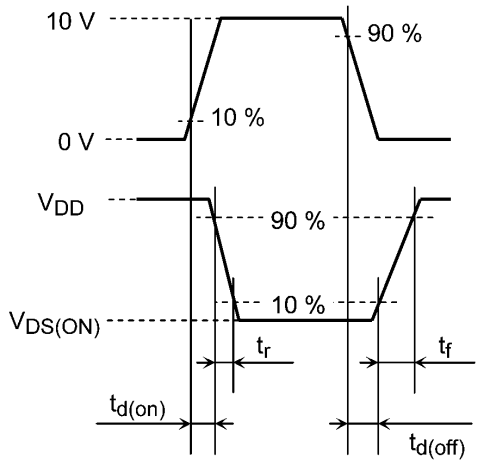


Fig. 5.3.2 Input Waveform/Output Waveform

5.4. Gate Charge Characteristics (Unless otherwise specified, T_a = 25 °C)

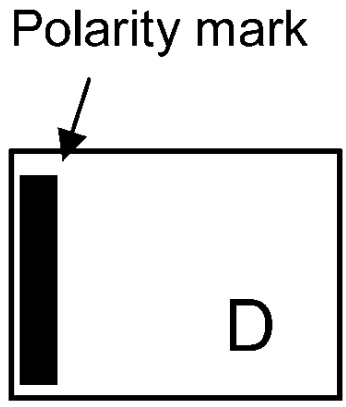
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} = 30 V, V_{GS} = 4.5 V, I_D = 200 mA	—	0.27	0.35	nC
Gate-source charge	Q_{gs}		—	0.08	—	
Gate-drain charge	Q_{gd}		—	0.08	—	

5.5. Source-Drain Characteristics (Unless otherwise specified, T_a = 25 °C)

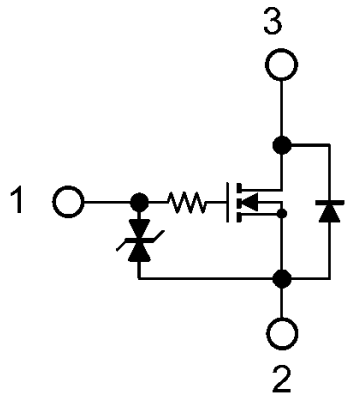
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	(Note 1)	V_{DSF}	I_D = -115 mA, V_{GS} = 0 V	—	0.87	-1.2	V

Note 1: Pulse measurement.

6. Marking



7. Equivalent Circuit



8. Characteristics Curves (Note)

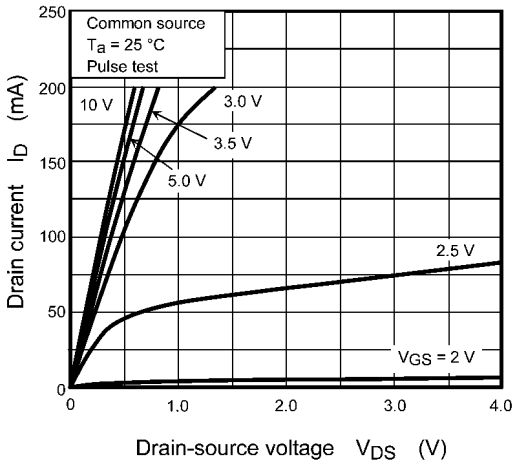


Fig. 8.1 I_D - V_{DS}

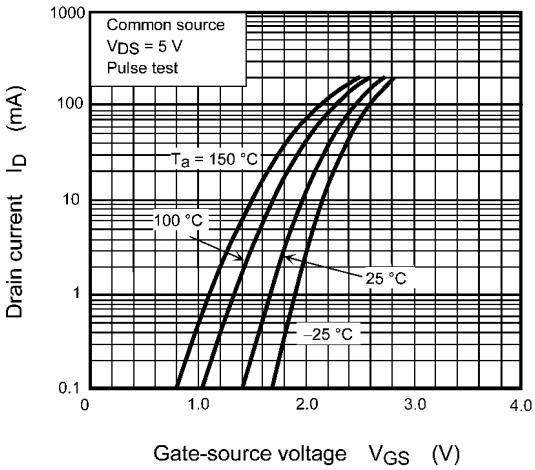


Fig. 8.2 I_D - V_{GS}

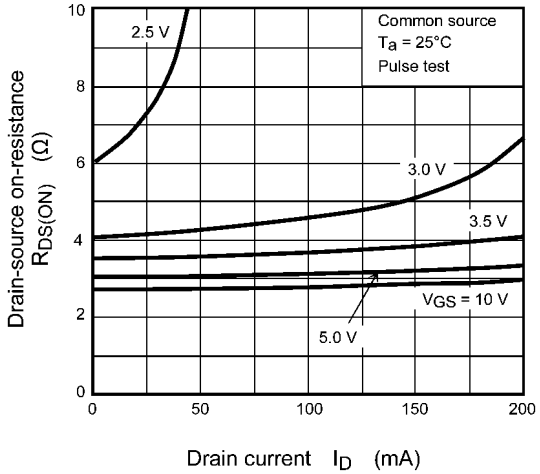


Fig. 8.3 $R_{DS(ON)}$ - I_D

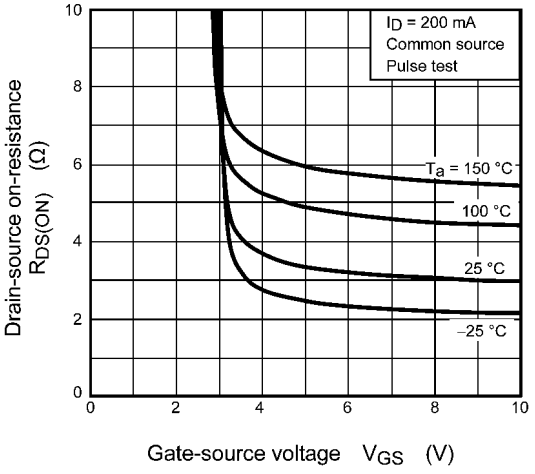


Fig. 8.4 $R_{DS(ON)}$ - V_{GS}

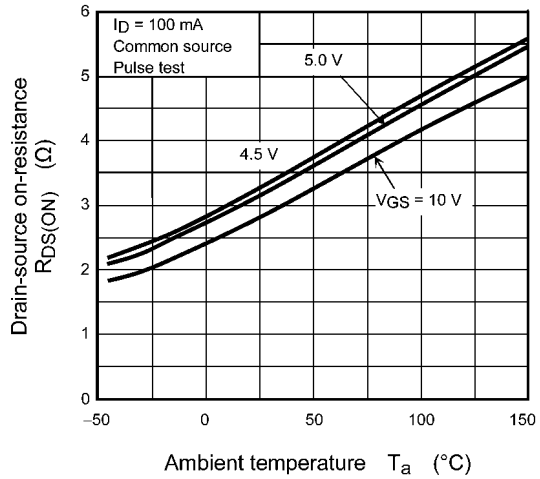


Fig. 8.5 $R_{DS(ON)}$ - T_a

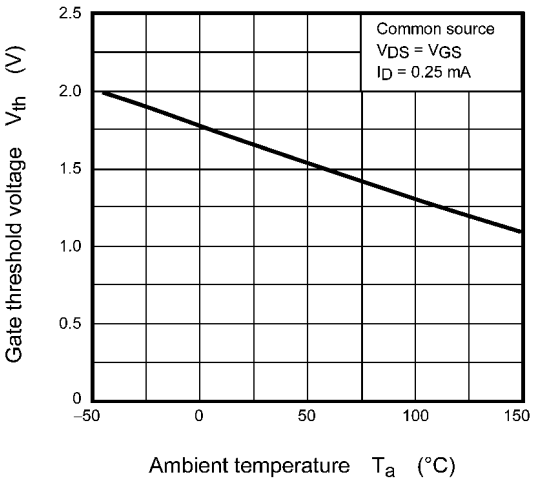


Fig. 8.6 V_{th} - T_a

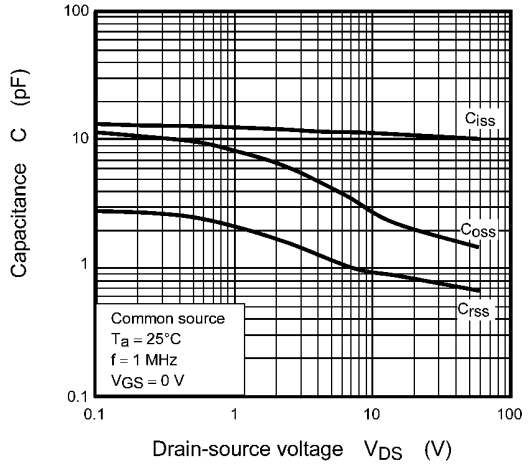


Fig. 8.7 C - V_{DS}

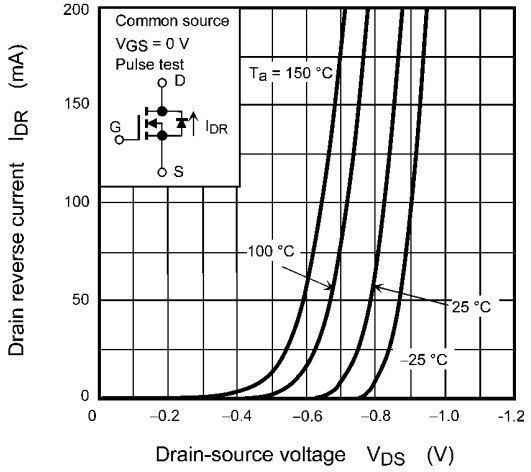


Fig. 8.8 I_{DR} - V_{DS}

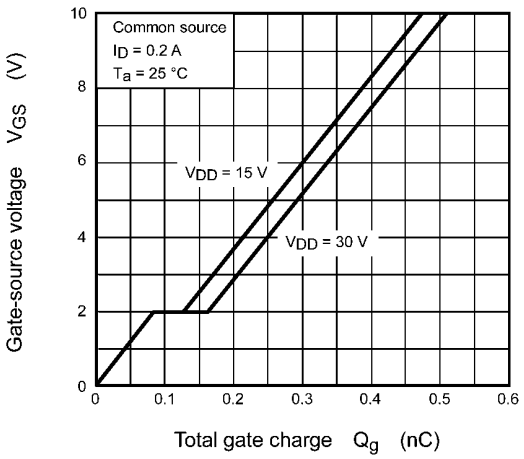


Fig. 8.9 Dynamic Input Characteristics

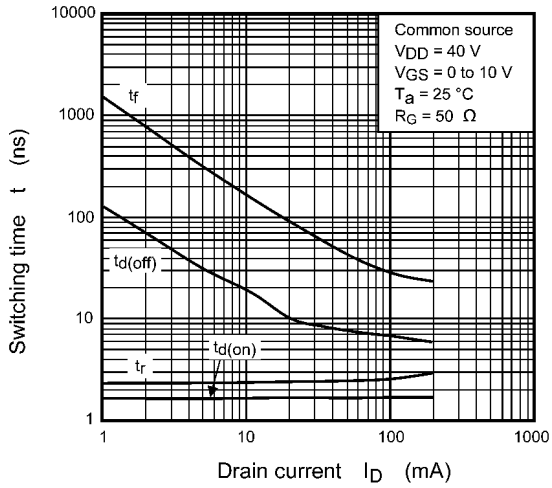


Fig. 8.10 t - I_D

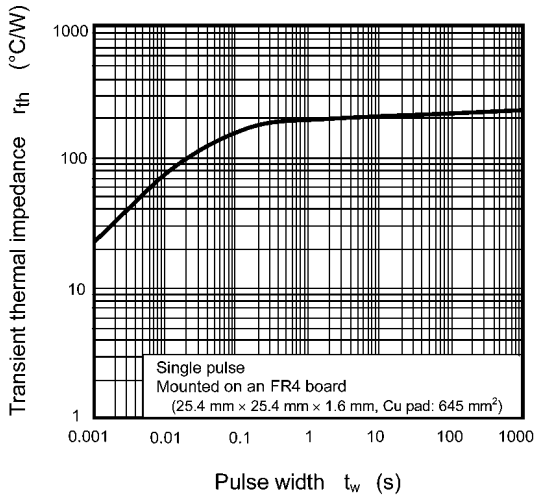


Fig. 8.11 r_{th} - t_w

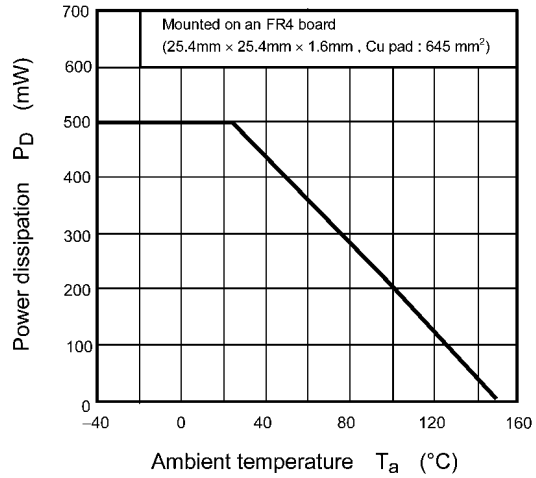
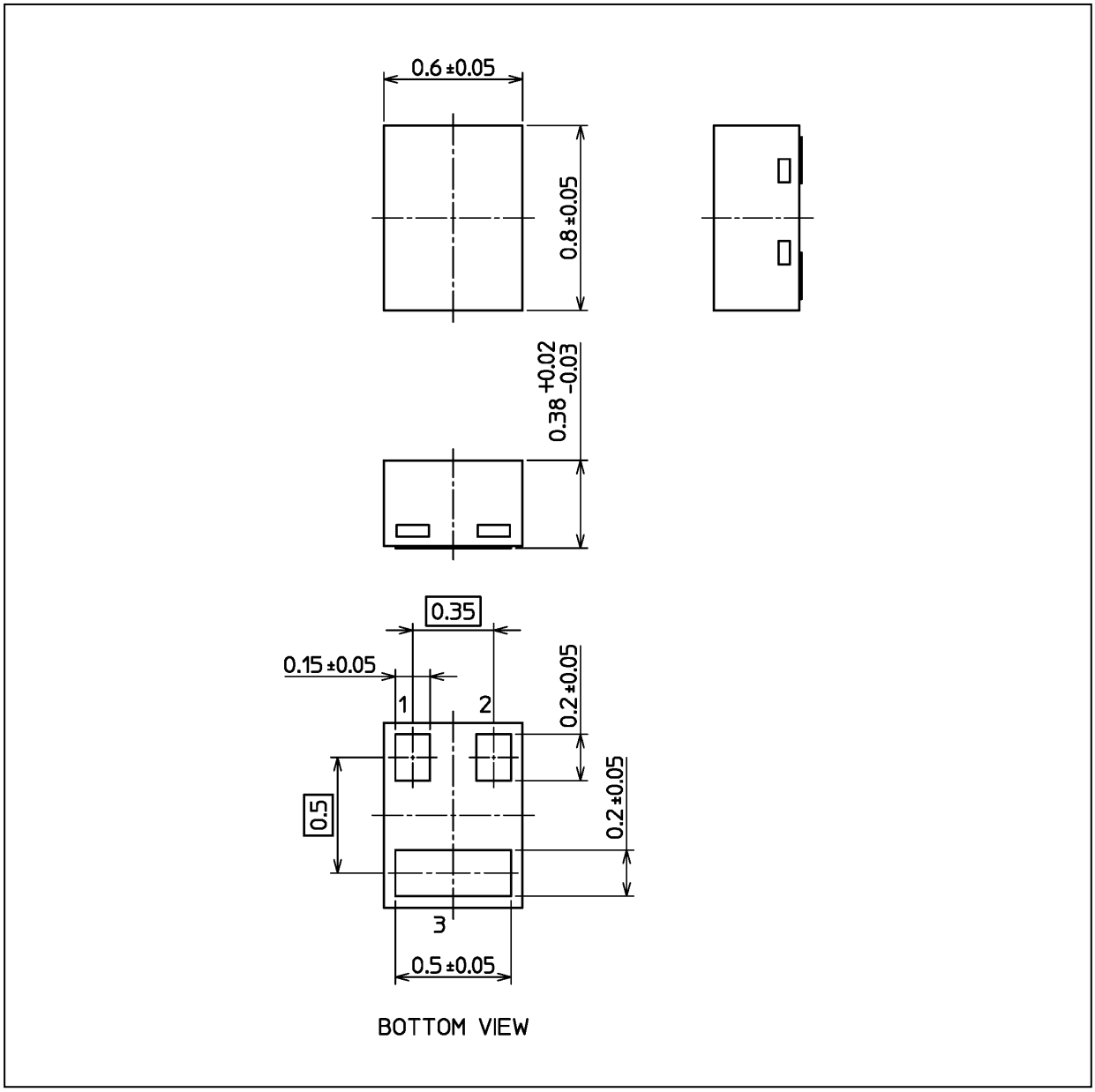


Fig. 8.12 P_D - T_a

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.55 mg (typ.)

Package Name(s)
Nickname: CST3C

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