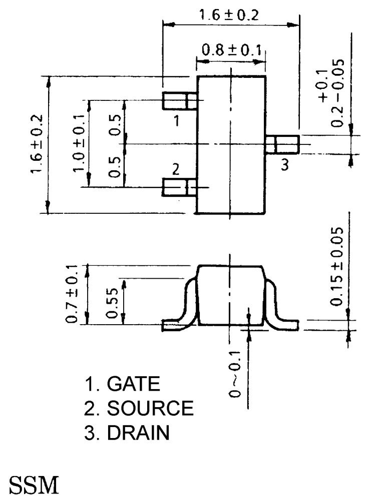
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K44FS

High Speed Switching Applications

Analog Switching Applications

Unit: mm



JEDEC	―
JEITA	―
TOSHIBA	2-2H1B

Weight: 2.4 mg (typ.)

- Compact package suitable for high-density mounting
- Low ON-resistance : $R_{DS(ON)}$ = 4.0 Ω (max) (@V_{GS} = 4 V)
  : $R_{DS(ON)}$ = 7.0 Ω (max) (@V_{GS} = 2.5 V)

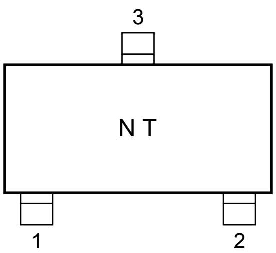
Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	30	V
Gate-Source voltage		V_{GSS}	±20	V
Drain current	DC	I_D	100	mA
	Pulse	I_{DP}	200	
Drain power dissipation (Ta = 25°C)		P_D (Note 1)	150	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

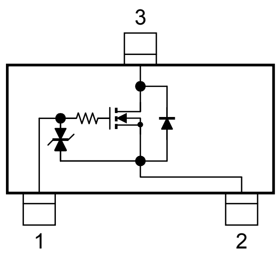
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: mounted on an FR4 board (25.4 mm × 25.4 mm × 1.6 mm, Cu Pad : 0.36mm^2 ×3)

Marking



Equivalent Circuit



Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

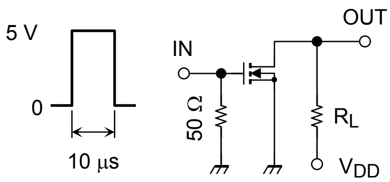
Start of commercial production
2009-12

Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±14 V, V_{DS} = 0 V	—	—	±1	μA
Drain-Source breakdown voltage		$V_{(BR) DSS}$	I_D = 0.1 mA, V_{GS} = 0 V	30	—	—	V
Drain Cut-off current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.8	—	1.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 10 mA	25	—	—	mS
Drain-Source ON resistance		$R_{DS (ON)}$	I_D = 10 mA, V_{GS} = 4 V	—	2.2	4.0	Ω
			I_D = 10 mA, V_{GS} = 2.5 V	—	4.0	7.0	
Input capacitance		C_{iss}	V_{DS} = 3 V, V_{GS} = 0 V, f = 1 MHz	—	8.5	—	pF
Reverse transfer capacitance		C_{rss}		—	5.3	—	
Output capacitance		C_{oss}		—	9.4	—	
Switching time	Turn-on time	t_{on}	V_{DD} = 5 V, I_D = 10 mA, V_{GS} = 0 to 5 V	—	50	—	ns
	Turn-off time	t_{off}		—	200	—	

Switching Time Test Circuit

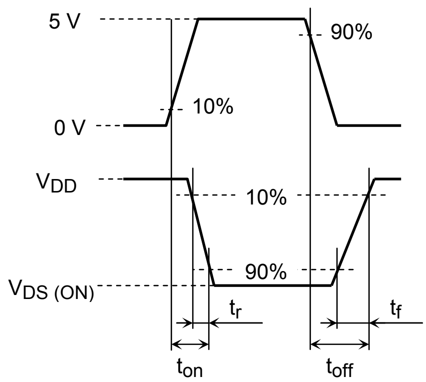
(a) Test circuit



V_{DD} = 5 V
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
(Z_{out} = 50 Ω)
Common source
Ta = 25°C

(b) V_{IN}

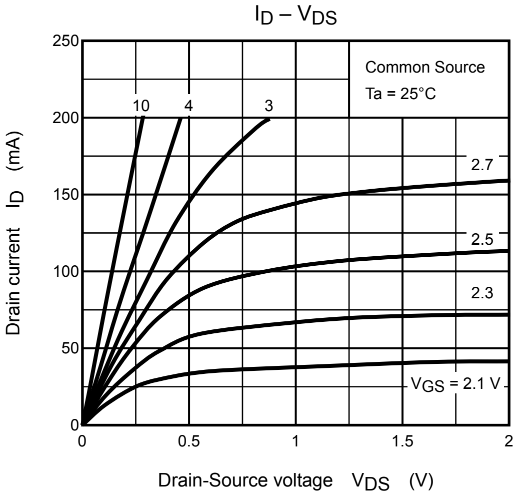
(c) V_{OUT}

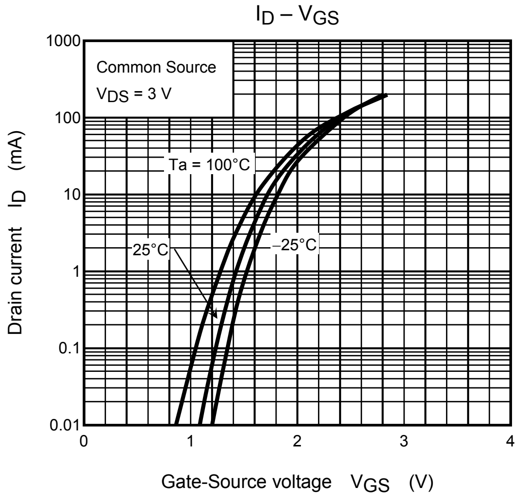


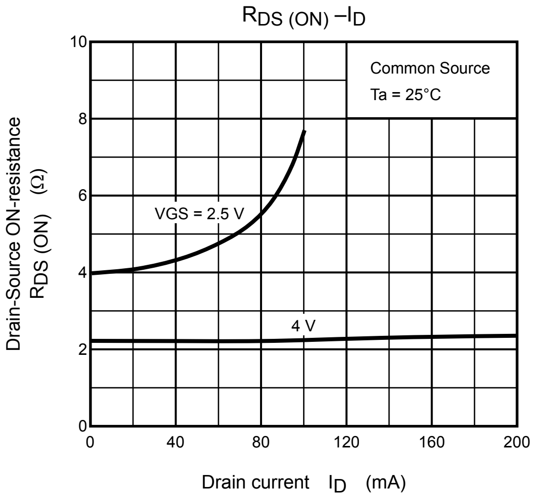
Precaution

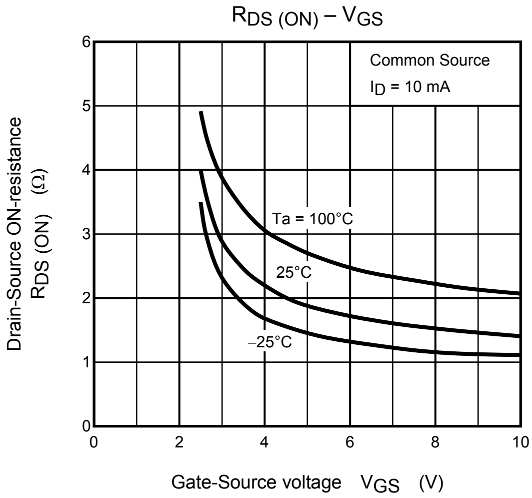
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (0.1mA for the SSM3K44FS). Then, for normal switching operation, $V_{GS(on)}$ must be higher than $V_{th,}$ and $V_{GS(off)}$ must be lower than $V_{th.}$ This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

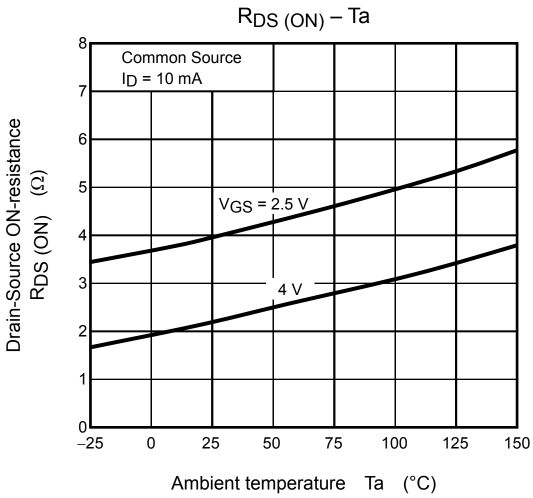
Take this into consideration when using the device

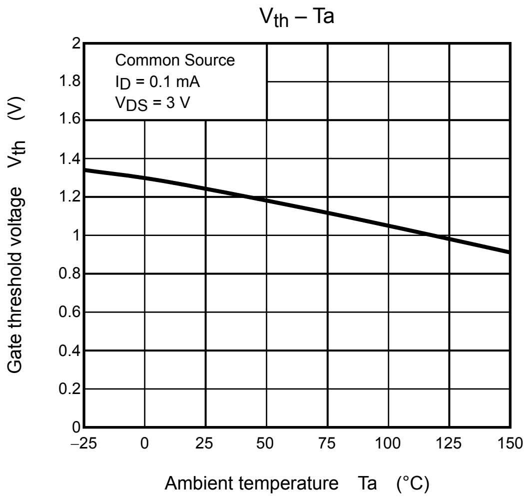

I_D – V_{DS}
Common Source
Ta = 25°C
10
4
3
2.7
2.5
2.3
V_{GS} = 2.1 V
Drain current I_D (mA)
Drain-Source voltage V_{DS} (V)
0
50
100
150
200
250
0.5
1
1.5
2

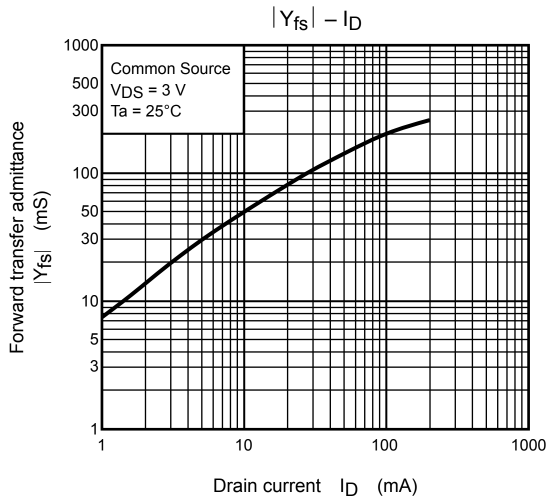

I_D – V_{GS}
Common Source
V_{DS} = 3 V
Ta = 100°C
25°C
−25°C
Drain current I_D (mA)
Gate-Source voltage V_{GS} (V)
0.01
0.1
1
10
100
1000
0
1
2
3
4

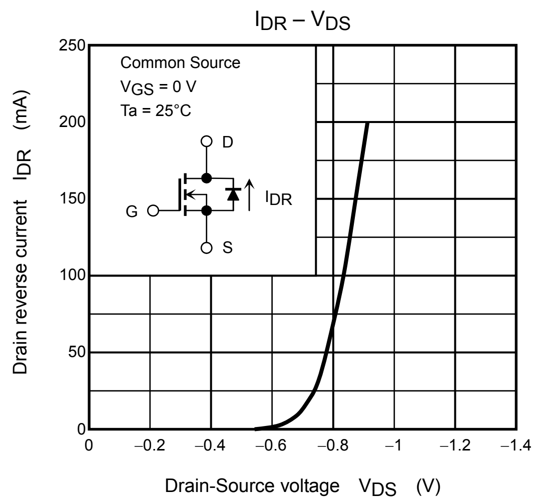

$R_{DS\ (ON)}$ – I_D
Common Source
Ta = 25°C
VGS = 2.5 V
4 V
Drain-Source ON-resistance $R_{DS\ (ON)}$ (Ω)
Drain current I_D (mA)
0
2
4
6
8
10
40
80
120
160
200

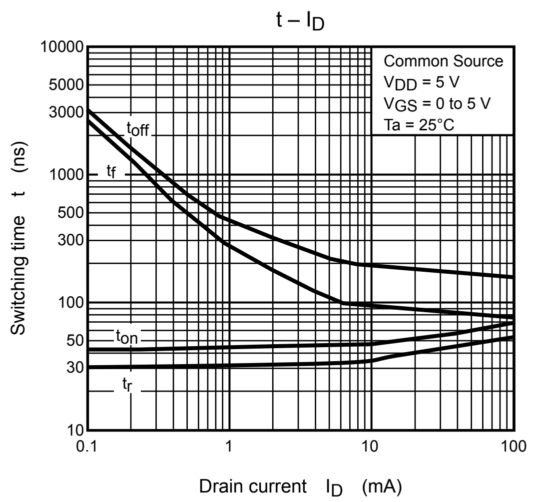

$R_{DS\ (ON)}$ – V_{GS}
Common Source
I_D = 10 mA
Ta = 100°C
25°C
−25°C
Drain-Source ON-resistance $R_{DS\ (ON)}$ (Ω)
Gate-Source voltage V_{GS} (V)
0
1
2
3
4
5
6
8
10

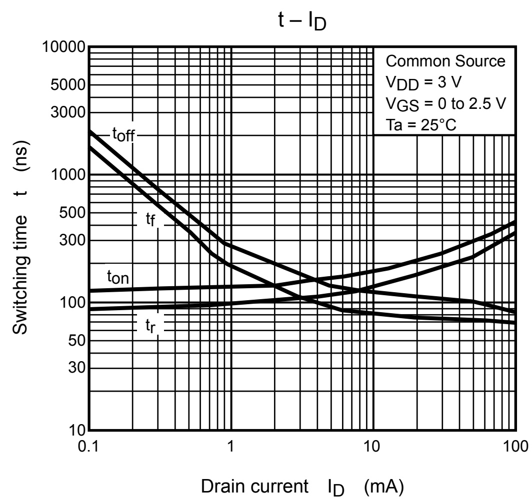

$R_{DS\ (ON)}$ – Ta
Common Source
I_D = 10 mA
V_{GS} = 2.5 V
4 V
Drain-Source ON-resistance $R_{DS\ (ON)}$ (Ω)
Ambient temperature Ta (°C)
0
1
2
3
4
5
6
7
8
−25
25
50
75
100
125
150

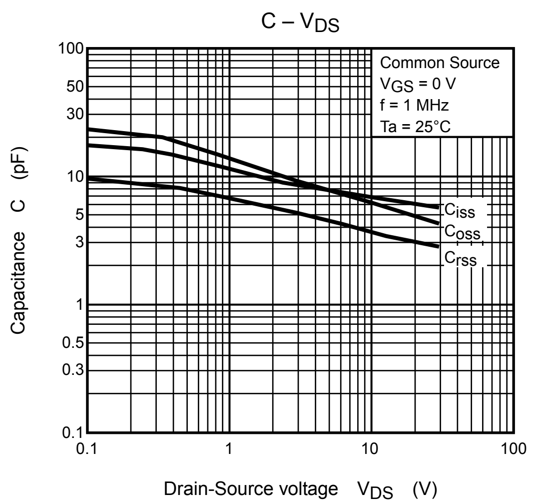

V_{th} – Ta
Common Source
I_D = 0.1 mA
V_{DS} = 3 V
Gate threshold voltage V_{th} (V)
Ambient temperature Ta (°C)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
−25
25
50
75
100
125
150

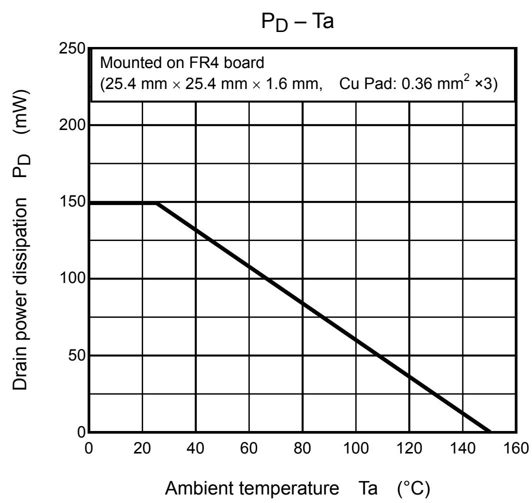

|Yfs| – ID
Common Source
VDS = 3 V
Ta = 25°C
Forward transfer admittance |Yfs| (mS)
Drain current ID (mA)


IDR – VDS
Common Source
VGS = 0 V
Ta = 25°C
D
G
S
IDR
Drain reverse current IDR (mA)
Drain-Source voltage VDS (V)


t – ID
Common Source
VDD = 5 V
VGS = 0 to 5 V
Ta = 25°C
toff
tf
ton
tr
Switching time t (ns)
Drain current ID (mA)


t – ID
Common Source
VDD = 3 V
VGS = 0 to 2.5 V
Ta = 25°C
toff
tf
ton
tr
Switching time t (ns)
Drain current ID (mA)


C – VDS
Common Source
VGS = 0 V
f = 1 MHz
Ta = 25°C
Ciss
Coss
Crss
Capacitance C (pF)
Drain-Source voltage VDS (V)


PD – Ta
Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.36 mm2 ×3)
Drain power dissipation PD (mW)
Ambient temperature Ta (°C)

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