CMOS Digital Integrated Circuits Silicon Monolithic

74VHCV245FT

1. Functional Description

- Octal Schmitt Bus Transceiver

2. General

The 74VHCV245FT is an advanced high speed CMOS OCTAL BUS TRANSCEIVER fabricated with silicon gate CMOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

Input pin and bus terminal have hysteresis between the positive-going and negative-going thresholds. Thus the 74VHCV245FT is capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, etc.

Note: Output in off-state.

3. Features (Note)

(1) AEC-Q100 (Rev. H) (Note 1)

(2) Wide operating temperature range: T_{opr} = -40 to 125 °C

(3) High speed: t_{pd} = 3.8 ns (typ.) at V_{CC} = 5.0 V

(4) Low power dissipation: I_{CC} = 2.0 μA (max) at T_a = 25°C

(5) Wide operating voltage range: $V_{CC(opr)}$ = 1.8 V to 5.5 V

(6) Output current: $|I_{OH}|/I_{OL}$ = 16 mA (min)(V_{CC} = 4.5 V)

(7) Power-down protection is provided on all inputs and outputs.

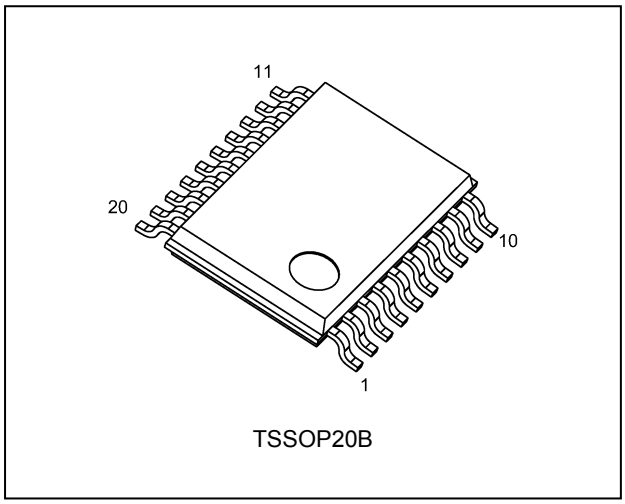
(8) Pin and function compatible with the 74 series (74AC/HC/AHC/LV etc.) 245 type.

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
All floating (high impedance) bus pins must have their input levels fixed by means of pull-up or pull-down resistors.

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

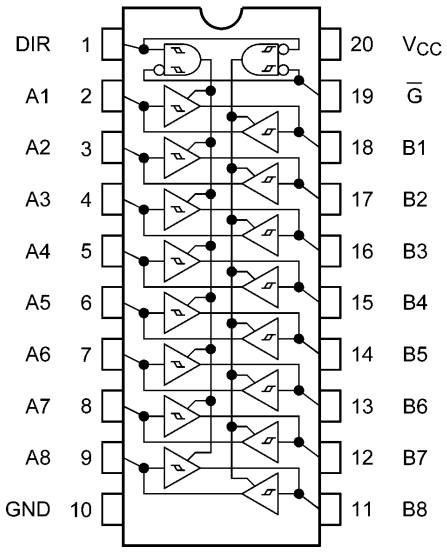
Start of commercial production
2014-10

4. Packaging



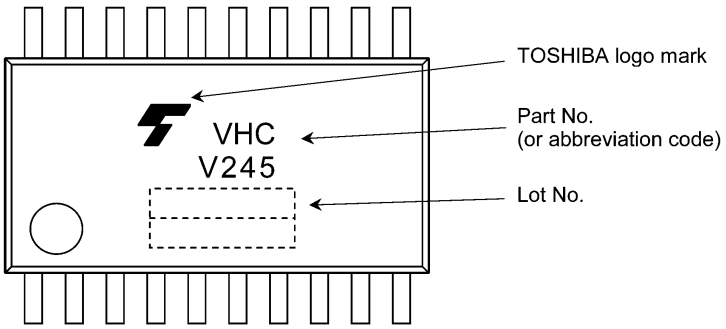
TSSOP20B

5. Pin Assignment



(top view)

6. Marking



7. Truth Table

Inputs $\overline{G}$	Inputs DIR	Function A Bus	Function B Bus	Output
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z	Z	Z

X: Don't care
Z: High Impedance

8. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage(DIR,$\overline{G}$)	V_{IN}		-0.5 to 7.0	V
Bus I/O voltage	$V_{I/O}$	(Note 1)	-0.5 to 7.0	V
		(Note 2)	-0.5 to V_{CC} + 0.5	
Input diode current	I_{IK}		-50	mA
Output diode current	I_{OK}	(Note 3)	±50	mA
Output current	I_{OUT}		±50	mA
Power dissipation	P_D	(Note 4)	180	mW
V_{CC}/ground current	I_{CC}/I_{GND}		±100	mA
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: OFF state.
Note 2: High (H) or Low (L) state. I_{OUT} absolute maximum rating must be observed.
Note 3: V_{OUT} < GND, V_{OUT} > V_{CC}
Note 4: 180 mW in the range of T_a = -40 to 85 °C. From T_a = 85 to 125 °C a derating factor of -3.25 mW/°C shall be applied until 50 mW.

9. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Note	Rating	Unit
Supply voltage	V_{CC}	—		1.8 to 5.5	V
Input voltage(DIR,$\overline{G}$)	V_{IN}	—		0 to 5.5	V
Bus I/O voltage	$V_{I/O}$	—	(Note 1)	0 to 5.5	V
			(Note 2)	0 to V_{CC}	
Operating temperature	T_{opr}	—		-40 to 125	°C
Input rise and fall times	dt/dv	V_{CC} = 3.3 ± 0.3 V		0 to 20	ms/V
		V_{CC} = 5.0 ± 0.5 V		0 to 1	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either V_{CC} or GND. Please connect both bus inputs and the bus outputs with V_{CC} or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note 1: OFF state.
Note 2: High (H) or Low (L) state.

10. Electrical Characteristics

10.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
Positive threshold voltage	V_P	—		1.8	—	—	1.65	V
				2.3	—	—	1.85	
				3.0	—	—	2.20	
				4.5	—	—	3.15	
				5.5	—	—	3.85	
Negative threshold voltage	V_N	—		1.8	0.15	—	—	V
				2.3	0.45	—	—	
				3.0	0.90	—	—	
				4.5	1.35	—	—	
				5.5	1.65	—	—	
Hysteresis voltage	V_H	—		1.8	0.15	—	1.05	V
				2.3	0.20	—	1.10	
				3.0	0.30	—	1.20	
				4.5	0.40	—	1.40	
				5.5	0.50	—	1.60	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	1.8	1.7	1.8	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			I_{OH} = -8 mA	3.0	2.58	—	—	
			I_{OH} = -16 mA	4.5	3.94	—	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	1.8	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			I_{OL} = 8 mA	3.0	—	—	0.36	
			I_{OL} = 16 mA	4.5	—	—	0.44	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 5.5 V		1.8 to 5.5	—	—	±0.5	μA
Power-OFF leakage current	I_{OFF}	V_{IN}/V_{OUT} = 5.5 V		0	—	—	0.5	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	2.0	μA

10.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Positive threshold voltage	V_P	—		1.8	—	1.65	V
				2.3	—	1.85	
				3.0	—	2.20	
				4.5	—	3.15	
				5.5	—	3.85	
Negative threshold voltage	V_N	—		1.8	0.15	—	V
				2.3	0.45	—	
				3.0	0.90	—	
				4.5	1.35	—	
				5.5	1.65	—	
Hysteresis voltage	V_H	—		1.8	0.15	1.05	V
				2.3	0.20	1.10	
				3.0	0.30	1.20	
				4.5	0.40	1.40	
				5.5	0.50	1.60	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	1.8	1.7	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			I_{OH} = -8 mA	3.0	2.48	—	
			I_{OH} = -16 mA	4.5	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	1.8	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			I_{OL} = 8 mA	3.0	—	0.44	
			I_{OL} = 16 mA	4.5	—	0.55	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 5.5 V		1.8 to 5.5	—	±5.0	μA
Power-OFF leakage current	I_{OFF}	V_{IN}/V_{OUT} = 5.5 V		0	—	5.0	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	20.0	μA

10.3. DC Characteristics (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Positive threshold voltage	V_P	—		1.8	—	1.65	V
				2.3	—	1.85	
				3.0	—	2.20	
				4.5	—	3.15	
				5.5	—	3.85	
Negative threshold voltage	V_N	—		1.8	0.15	—	V
				2.3	0.45	—	
				3.0	0.90	—	
				4.5	1.35	—	
				5.5	1.65	—	
Hysteresis voltage	V_H	—		1.8	0.15	1.05	V
				2.3	0.20	1.10	
				3.0	0.30	1.20	
				4.5	0.40	1.40	
				5.5	0.50	1.60	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	1.8	1.7	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			I_{OH} = -8 mA	3.0	2.40	—	
			I_{OH} = -16 mA	4.5	3.70	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	1.8	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			I_{OL} = 8 mA	3.0	—	0.55	
			I_{OL} = 16 mA	4.5	—	0.65	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 5.5 V		1.8 to 5.5	—	±20.0	μA
Power-OFF leakage current	I_{OFF}	V_{IN}/V_{OUT} = 5.5 V		0	—	20.0	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	±2.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	40.0	μA

10.4. AC Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time	t_{PLH},t_{PHL}		—	2.5 ± 0.2	15	—	5.9	13.0	ns
					50	—	8.7	15.9	
				3.3 ± 0.3	15	—	4.6	8.4	
					50	—	6.9	11.9	
				5.0 ± 0.5	15	—	3.8	5.5	
					50	—	5.4	7.5	
3-state output enable time	t_{PZL},t_{PZH}		R_L = 1 kΩ	2.5 ± 0.2	15	—	7.0	19.9	ns
					50	—	9.6	22.7	
				3.3 ± 0.3	15	—	5.3	13.2	
					50	—	7.4	16.7	
				5.0 ± 0.5	15	—	4.1	8.5	
					50	—	5.7	10.6	
3-state output disable time	t_{PLZ},t_{PHZ}		R_L = 1 kΩ	2.5 ± 0.2	50	—	15.0	23.1	ns
				3.3 ± 0.3	50	—	11.6	15.8	
				5.0 ± 0.5	50	—	9.3	9.7	
Output skew	t_{osLH},t_{osHL}	(Note 1)	—	2.5 ± 0.2	50	—	—	2.0	ns
				3.3 ± 0.3	50	—	—	1.5	
				5.0 ± 0.5	50	—	—	1.0	
Input capacitance	C_{IN}		DIR, $\overline{G}$			—	4	10	pF
Bus I/O capacitance	$C_{I/O}$		An, Bn			—	6	—	pF
Power dissipation capacitance	C_{PD}	(Note 2)	—			—	26	—	pF

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per bit)

10.5. AC Characteristics
(Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	t_{PLH},t_{PHL}		—	2.5 ± 0.2	15	1.0	15.0	ns
					50	1.0	18.0	
				3.3 ± 0.3	15	1.0	10.0	
					50	1.0	13.5	
				5.0 ± 0.5	15	1.0	6.5	
					50	1.0	8.5	
3-state output enable time	t_{PZL},t_{PZH}		R_L = 1 kΩ	2.5 ± 0.2	15	1.0	22.0	ns
					50	1.0	26.0	
				3.3 ± 0.3	15	1.0	15.5	
					50	1.0	19.0	
				5.0 ± 0.5	15	1.0	10.0	
					50	1.0	12.0	
3-state output disable time	t_{PLZ},t_{PHZ}		R_L = 1 kΩ	2.5 ± 0.2	50	1.0	25.0	ns
				3.3 ± 0.3	50	1.0	18.0	
				5.0 ± 0.5	50	1.0	11.0	
Output skew	t_{osLH},t_{osHL}	(Note 1)	—	2.5 ± 0.2	50	—	2.0	ns
				3.3 ± 0.3	50	—	1.5	
				5.0 ± 0.5	50	—	1.0	
Input capacitance	C_{IN}		DIR, $\overline{G}$			—	10	pF

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

10.6. AC Characteristics
(Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	t_{PLH},t_{PHL}		—	2.5 ± 0.2	15	1.0	16.5	ns
					50	1.0	19.5	
				3.3 ± 0.3	15	1.0	11.5	
					50	1.0	15.0	
				5.0 ± 0.5	15	1.0	7.5	
					50	1.0	9.5	
3-state output enable time	t_{PZL},t_{PZH}		R_L = 1 kΩ	2.5 ± 0.2	15	1.0	23.5	ns
					50	1.0	28.5	
				3.3 ± 0.3	15	1.0	17.5	
					50	1.0	21.0	
				5.0 ± 0.5	15	1.0	11.5	
					50	1.0	13.5	
3-state output disable time	t_{PLZ},t_{PHZ}		R_L = 1 kΩ	2.5 ± 0.2	50	1.0	26.5	ns
				3.3 ± 0.3	50	1.0	20.0	
				5.0 ± 0.5	50	1.0	12.5	
Output skew	t_{osLH},t_{osHL}	(Note 1)	—	2.5 ± 0.2	50	—	2.0	ns
				3.3 ± 0.3	50	—	1.5	
				5.0 ± 0.5	50	—	1.0	
Input capacitance	C_{IN}		DIR, $\overline{G}$			—	10	pF

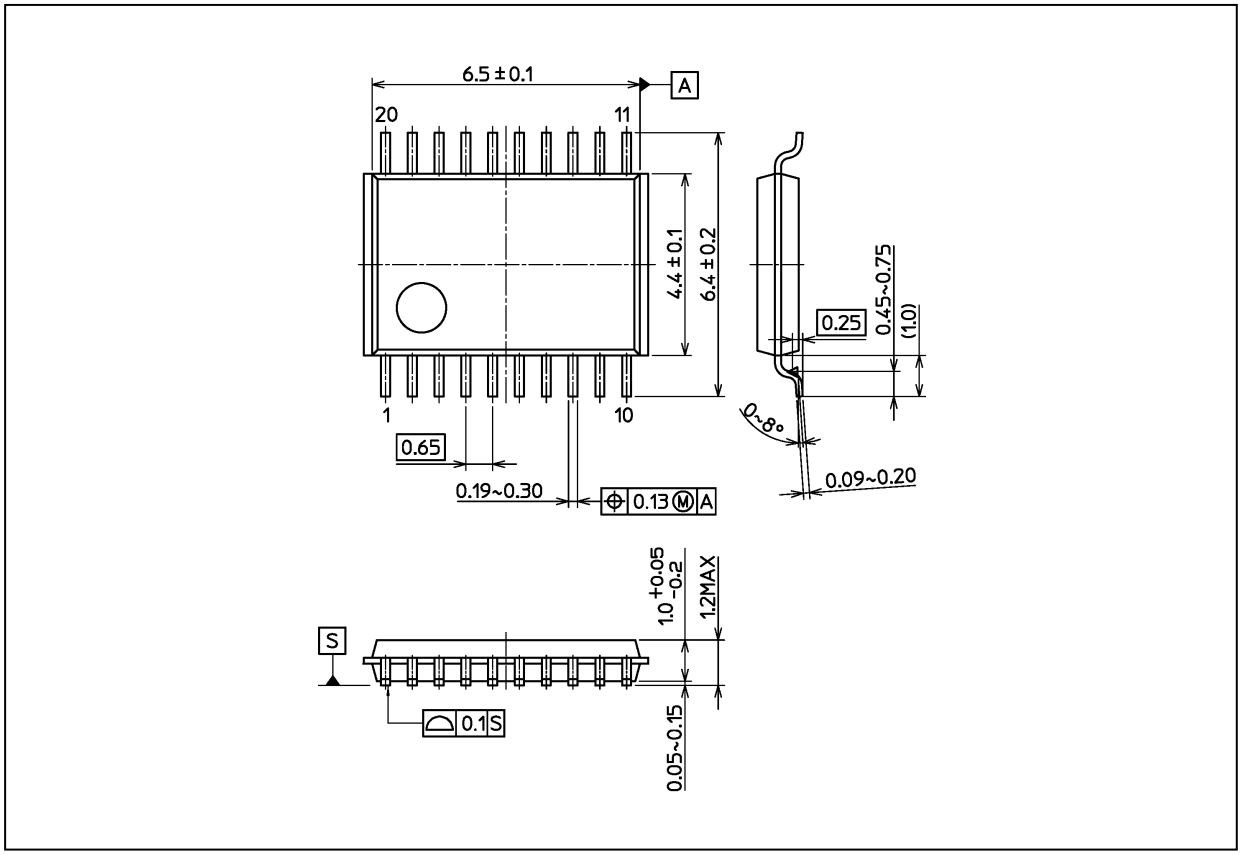
Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

10.7. Noise Characteristics (Unless otherwise specified, T_a = 25°C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Max	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	3.3	0.5	—	V
			5.0	1.0	—	
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	3.3	-0.1	—	V
			5.0	-0.3	—	
Minimum high-level dynamic input voltage	V_{IHD}	C_L = 50 pF	5.0	—	3.5	V
Maximum low-level dynamic input voltage	V_{ILD}	C_L = 50 pF	5.0	—	1.5	V

Package Dimensions

Unit: mm



Weight: 0.071 g (typ.)

Package Name(s)
Nickname: TSSOP20B

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