

74VHCV07FT

1. Functional Description

- Hex Schmitt Buffer (Open Drain)

2. General

The 74VHCV07FT is an advanced high speed CMOS BUFFER fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Output have high performance MOS N-channel transistor. (OPEN-DRAIN outputs)

Input pin have hysteresis between the positive-going and negative-going thresholds. Thus the 74VHCV07FT is capable of squaring up transitions of slowly changing input signals such as line receivers.

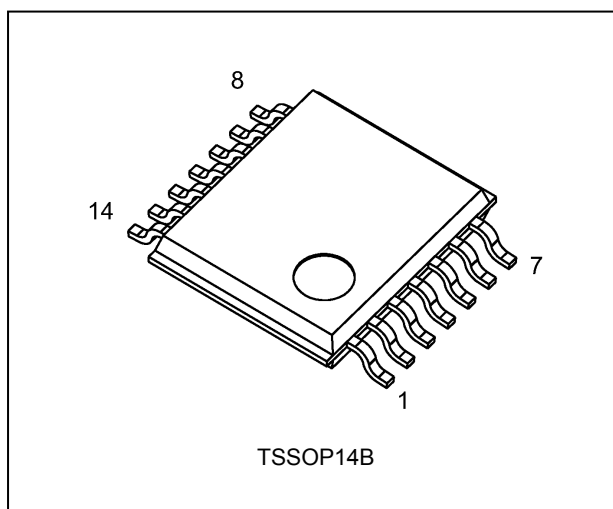
Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, etc.

3. Features

- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature range: $T_{opr} = -40$ to 125°C
- (3) High speed: $t_{pd} = 3.8$ ns (typ.) at $V_{CC} = 5.0$ V
- (4) Low power dissipation: $I_{CC} = 2.0$ μA (max) at $T_a = 25^{\circ}\text{C}$
- (5) Wide operating voltage range: $V_{CC(opr)} = 1.8$ V to 5.5 V
- (6) Output current: $I_{OL} = 16$ mA (min)($V_{CC} = 4.5$ V)
- (7) Power-down protection is provided on all inputs and outputs.
- (8) Pin and function compatible with the 74 series (74AC/HC/AHC/LV etc.) 07 type.

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

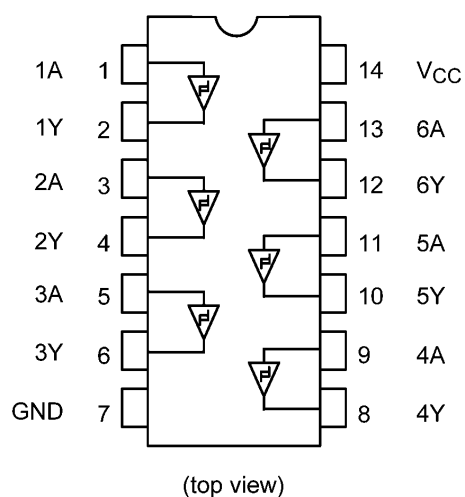
4. Packaging



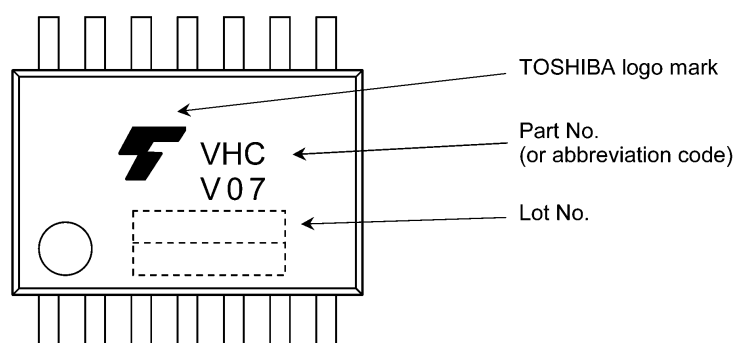
Start of commercial production

2014-11

5. Pin Assignment



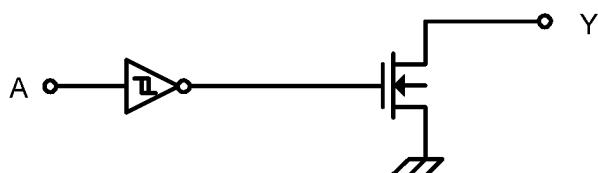
6. Marking



7. Truth Table

A	Y
L	L
H	Z

8. System Diagram (per gate)



9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to 7.0	V
Output voltage	V_{OUT}	(Note 1)	-0.5 to 7.0	V
Input diode current	I_{IK}		-50	mA
Output diode current	I_{OK}	(Note 2)	-50	mA
Output current	I_{OUT}		50	mA
Power dissipation	P_D	(Note 3)	180	mW
V_{CC} /ground current	I_{CC}/I_{GND}		± 100	mA
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Output in off state. I_{OUT} absolute maximum rating must be observed.(Output in low state)

Note 2: $V_{OUT} < GND$

Note 3: 180 mW in the range of $T_a = -40$ to 85 °C. From $T_a = 85$ to 125 °C a derating factor of -3.25 mW/°C shall be applied until 50 mW.

10. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}	—	1.8 to 5.5	V
Input voltage	V_{IN}	—	0 to 5.5	V
Output voltage	V_{OUT}	—	0 to 5.5	V
Operating temperature	T_{opr}	—	-40 to 125	°C
Input rise and fall times	dt/dv	$V_{CC} = 3.3 \pm 0.3$ V	0 to 20	ms/V
		$V_{CC} = 5.0 \pm 0.5$ V	0 to 1	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^{\circ}\text{C}$)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
Positive threshold voltage	V_P	—		1.8	—	—	1.65	V
				2.3	—	—	1.85	
				3.0	—	—	2.20	
				4.5	—	—	3.15	
				5.5	—	—	3.85	
Negative threshold voltage	V_N	—		1.8	0.15	—	—	V
				2.3	0.45	—	—	
				3.0	0.90	—	—	
				4.5	1.35	—	—	
				5.5	1.65	—	—	
Hysteresis voltage	V_H	—		1.8	0.15	—	1.05	V
				2.3	0.20	—	1.10	
				3.0	0.30	—	1.20	
				4.5	0.40	—	1.40	
				5.5	0.50	—	1.60	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	1.8	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			$I_{OL} = 8\text{ mA}$	3.0	—	—	0.36	
			$I_{OL} = 16\text{ mA}$	4.5	—	—	0.44	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH}$ $V_{OUT} = 0\text{ to }5.5\text{ V}$		1.8 to 5.5	—	—	± 0.25	μA
Power-OFF leakage current	I_{OFF}	$V_{IN}/V_{OUT} = 5.5\text{ V}$		0	—	—	0.5	μA
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V or GND}$		0 to 5.5	—	—	± 0.1	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}\text{ or GND}$		5.5	—	—	2.0	μA

11.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $85\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Positive threshold voltage	V_P	—		1.8	—	1.65	V
				2.3	—	1.85	
				3.0	—	2.20	
				4.5	—	3.15	
				5.5	—	3.85	
Negative threshold voltage	V_N	—		1.8	0.15	—	V
				2.3	0.45	—	
				3.0	0.90	—	
				4.5	1.35	—	
				5.5	1.65	—	
Hysteresis voltage	V_H	—		1.8	0.15	1.05	V
				2.3	0.20	1.10	
				3.0	0.30	1.20	
				4.5	0.40	1.40	
				5.5	0.50	1.60	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	1.8	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 8\text{ mA}$	3.0	—	0.44	
			$I_{OL} = 16\text{ mA}$	4.5	—	0.55	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH}$ $V_{OUT} = 0$ to 5.5 V		1.8 to 5.5	—	± 2.5	μA
Power-OFF leakage current	I_{OFF}	$V_{IN}/V_{OUT} = 5.5\text{ V}$		0	—	5.0	μA
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND		0 to 5.5	—	± 1.0	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	20.0	μA

11.3. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $125\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Positive threshold voltage	V_P	—		1.8	—	1.65	V
				2.3	—	1.85	
				3.0	—	2.20	
				4.5	—	3.15	
				5.5	—	3.85	
Negative threshold voltage	V_N	—		1.8	0.15	—	V
				2.3	0.45	—	
				3.0	0.90	—	
				4.5	1.35	—	
				5.5	1.65	—	
Hysteresis voltage	V_H	—		1.8	0.15	1.05	V
				2.3	0.20	1.10	
				3.0	0.30	1.20	
				4.5	0.40	1.40	
				5.5	0.50	1.60	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	1.8	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 8\text{ mA}$	3.0	—	0.55	
			$I_{OL} = 16\text{ mA}$	4.5	—	0.65	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH}$ $V_{OUT} = 0$ to 5.5 V		1.8 to 5.5	—	± 10.0	μA
Power-OFF leakage current	I_{OFF}	$V_{IN}/V_{OUT} = 5.5\text{ V}$		0	—	20.0	μA
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND		0 to 5.5	—	± 2.0	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	40.0	μA

11.4. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time	t_{pZL}		$R_L = 1\text{ k}\Omega$	2.5 ± 0.2	15	—	6.7	10.4	ns
					50	—	9.4	15.2	
				3.3 ± 0.3	15	—	5.2	7.1	
					50	—	7.1	10.6	
				5.0 ± 0.5	15	—	3.8	5.5	
					50	—	5.3	7.5	
Propagation delay time	t_{PLZ}		$R_L = 1\text{ k}\Omega$	2.5 ± 0.2	50	—	12.2	15.2	ns
				3.3 ± 0.3	50	—	9.5	10.6	
				5.0 ± 0.5	50	—	7.0	7.5	
Input capacitance	C_{IN}		—			—	4	10	pF
Output capacitance	C_{OUT}		—			—	5	—	pF
Power dissipation capacitance	C_{PD}	(Note 1)	—			—	4	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/6 \text{ (per gate)}$$

11.5. AC Characteristics

(Unless otherwise specified, $T_a = -40$ to $85\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	t_{PZL}	$R_L = 1\text{ k}\Omega$	2.5 ± 0.2	15	1.0	13.0	ns
				50	1.0	18.0	
			3.3 ± 0.3	15	1.0	8.5	
				50	1.0	12.0	
			5.0 ± 0.5	15	1.0	6.5	
				50	1.0	8.5	
Propagation delay time	t_{PLZ}	$R_L = 1\text{ k}\Omega$	2.5 ± 0.2	50	1.0	18.0	ns
			3.3 ± 0.3	50	1.0	12.0	
			5.0 ± 0.5	50	1.0	8.5	
Input capacitance	C_{IN}	—			—	10	pF

11.6. AC Characteristics

(Unless otherwise specified, $T_a = -40$ to $125\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

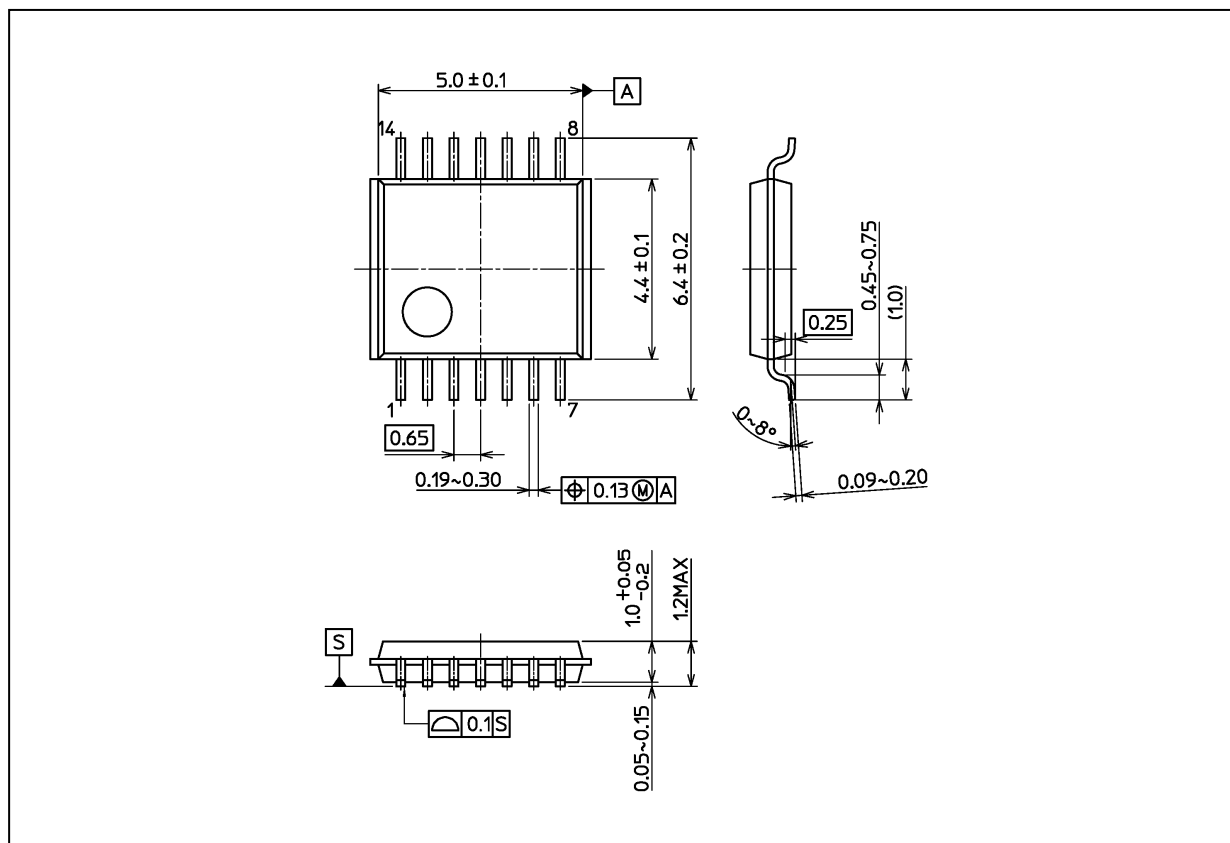
Characteristics	Symbol	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	t_{PZL}	$R_L = 1\text{ k}\Omega$	2.5 ± 0.2	15	1.0	15.0	ns
				50	1.0	20.0	
			3.3 ± 0.3	15	1.0	10.0	
				50	1.0	13.5	
			5.0 ± 0.5	15	1.0	7.5	
				50	1.0	9.5	
Propagation delay time	t_{PLZ}	$R_L = 1\text{ k}\Omega$	2.5 ± 0.2	50	1.0	20.0	ns
			3.3 ± 0.3	50	1.0	13.5	
			5.0 ± 0.5	50	1.0	9.5	
Input capacitance	C_{IN}	—			—	10	pF

11.7. Noise Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Max	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	$C_L = 50\text{ pF}$	3.3	0.3	—	V
			5.0	0.6	—	
Quiet output minimum dynamic V_{OL}	V_{OLV}	$C_L = 50\text{ pF}$	3.3	-0.1	—	V
			5.0	-0.2	—	
Minimum high-level dynamic input voltage	V_{IHD}	$C_L = 50\text{ pF}$	5.0	—	3.5	V
Maximum low-level dynamic input voltage	V_{ILD}	$C_L = 50\text{ pF}$	5.0	—	1.5	V

Package Dimensions

Unit: mm



Weight: 0.054 g (typ.)

Package Name(s)
Nickname: TSSOP14B

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