CMOS Digital Integrated Circuits Silicon Monolithic

74HC374D

1. Functional Description

- Octal D-Type Flip Flop with 3-State Outputs

2. General

The 74HC374D is a high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

When the input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features

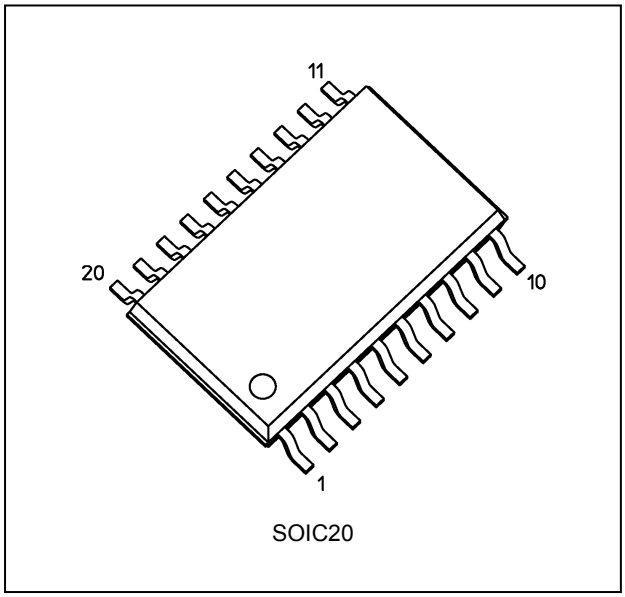
(1) High speed: f_{MAX} = 90 MHz (typ.) at V_{CC} = 6.0 V

(2) Low power dissipation: I_{CC} = 4.0 μA (max) at T_a = 25 °C

(3) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$

(4) Wide operating voltage range: $V_{CC(opr)}$ = 2.0 V to 6.0 V

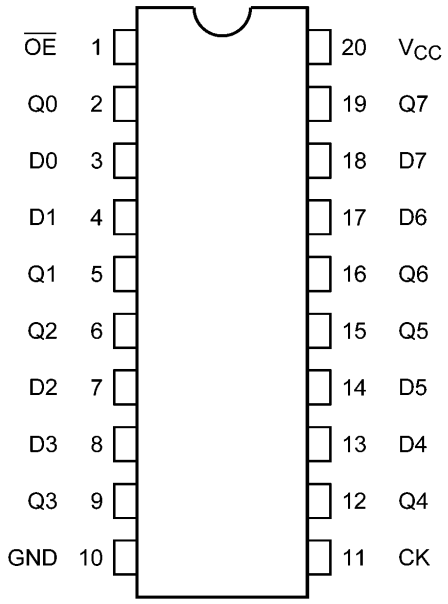
4. Packaging



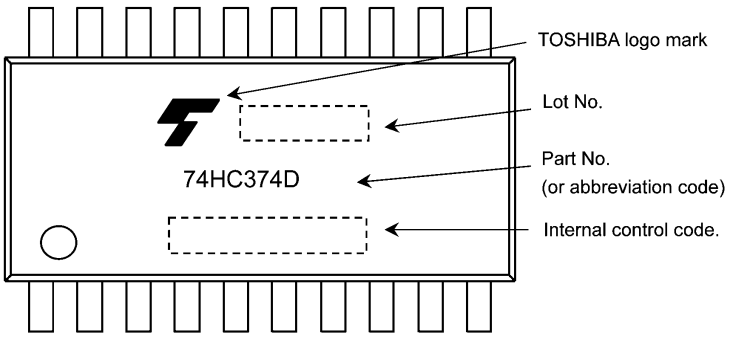
SOIC20

Start of commercial production
2016-03

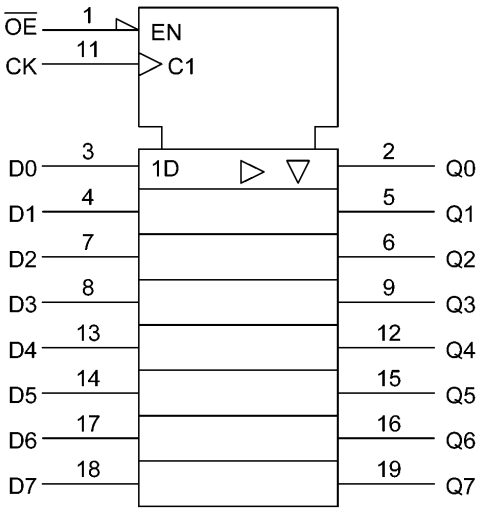
5. Pin Assignment



6. Marking



7. IEC Logic Symbol

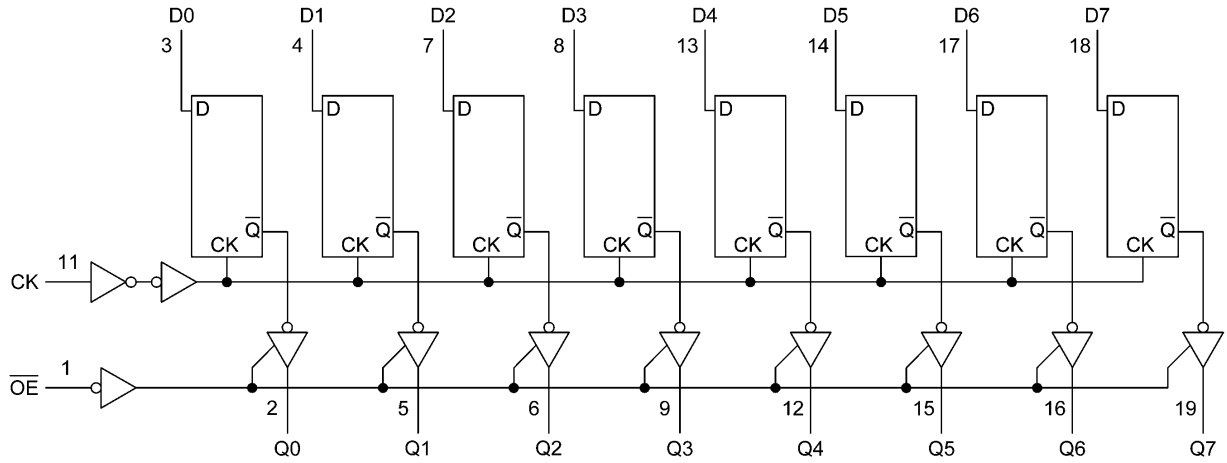


8. Truth Table

Inputs			Output
$\overline{OE}$	CK	D	
H	X	X	Z
L	↓	X	Qn
L	↑	L	L
L	↑	H	H

X: Don't care
Z: High impedance
Qn: No change

9. System Diagram



10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}		-0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}		±20	mA
Output diode current	I_{OK}		±20	mA
Output current	I_{OUT}		±35	mA
V_{CC}/ground current	I_{CC}		±75	mA
Power dissipation	P_D	(Note 1)	500	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: PD derates linearly with -8 mW/°C above 85 °C

11. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}	—	2.0 to 6.0	V
Input voltage	V_{IN}	—	0 to V_{CC}	V
Output voltage	V_{OUT}	—	0 to V_{CC}	V
Operating temperature	T_{opr}	—	-40 to 125	°C
Input rise and fall times	t_r,t_f	—	0 to 50	μs

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

12. Electrical Characteristics

12.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				4.5	3.15	—	—	
				6.0	4.20	—	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	V
				4.5	—	—	1.35	
				6.0	—	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	2.0	—	V
				4.5	4.4	4.5	—	
				6.0	5.9	6.0	—	
			I_{OH} = -6 mA	4.5	4.18	4.31	—	
			I_{OH} = -7.8 mA	6.0	5.68	5.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	V
				4.5	—	0.0	0.1	
				6.0	—	0.0	0.1	
			I_{OL} = 6 mA	4.5	—	0.17	0.26	
			I_{OL} = 7.8 mA	6.0	—	0.18	0.26	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	—	±0.5	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND I_O = 0 A		6.0	—	—	4.0	μA

12.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	—	V
				4.5	4.4	—	
				6.0	5.9	—	
			I_{OH} = -6 mA	4.5	4.13	—	
			I_{OH} = -7.8 mA	6.0	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
			I_{OL} = 6 mA	4.5	—	0.33	
			I_{OL} = 7.8 mA	6.0	—	0.33	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	±5.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND I_O = 0 A		6.0	—	40.0	μA

12.3. DC Characteristics (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	—	V
				4.5	4.4	—	
				6.0	5.9	—	
			I_{OH} = -6 mA	4.5	3.7	—	
			I_{OH} = -7.8 mA	6.0	5.2	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
			I_{OL} = 6 mA	4.5	—	0.4	
			I_{OL} = 7.8 mA	6.0	—	0.4	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	±10.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND I_O = 0 A		6.0	—	160.0	μA

12.4. Timing Requirements (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}$,$t_{w(H)}$	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum setup time (Dn)	t_s	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum hold time (Dn)	t_h	—	2.0	—	0	ns
			4.5	—	0	
			6.0	—	0	
Clock frequency	f	—	2.0	—	6	MHz
			4.5	—	31	
			6.0	—	36	

12.5. Timing Requirements (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}$,$t_{w(H)}$	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum setup time (Dn)	t_s	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum hold time (Dn)	t_h	—	2.0	0	ns
			4.5	0	
			6.0	0	
Clock frequency	f	—	2.0	5	MHz
			4.5	25	
			6.0	29	

12.6. Timing Requirements (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}$,$t_{w(H)}$	—	2.0	120	ns
			4.5	24	
			6.0	20	
Minimum setup time (Dn)	t_s	—	2.0	120	ns
			4.5	24	
			6.0	20	
Minimum hold time (Dn)	t_h	—	2.0	0	ns
			4.5	0	
			6.0	0	
Clock frequency	f	—	2.0	4	MHz
			4.5	20	
			6.0	24	

12.7. AC Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Note	Test Condition	C_L (pF)	V_{CC} (V)	Min	Typ.	Max	Unit
Output transition time	t_{TLH},t_{THL}		—	50	2.0	—	20	60	ns
					4.5	—	6	12	
					6.0	—	5	10	
Propagation delay time (CK-Q)	t_{PLH},t_{PHL}		—	50	2.0	—	45	140	ns
					4.5	—	15	28	
					6.0	—	13	24	
				150	2.0	—	60	190	
					4.5	—	20	38	
					6.0	—	17	32	
Output enable time	t_{PZL},t_{PZH}		R_L = 1 kΩ	50	2.0	—	39	135	ns
					4.5	—	13	27	
					6.0	—	11	23	
				150	2.0	—	54	185	
					4.5	—	18	37	
					6.0	—	15	31	
Output disable time	t_{PLZ},t_{PHZ}		R_L = 1 kΩ	50	2.0	—	30	135	ns
					4.5	—	13	27	
					6.0	—	12	23	
Maximum clock frequency	f_{MAX}		—	50	2.0	6	18	—	MHz
					4.5	31	75	—	
					6.0	36	90	—	
Input capacitance	C_{IN}		—			—	3	—	pF
Output capacitance	C_{OUT}		—			—	4	—	pF
Power dissipation capacitance	C_{PD}	(Note 1)	—			—	11	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per latch)

And the total C_{PD} when n pcs of latch operate can be gained by the following equation.

C_{PD} (total) = 22 + 16 × n

12.8. AC Characteristics
(Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

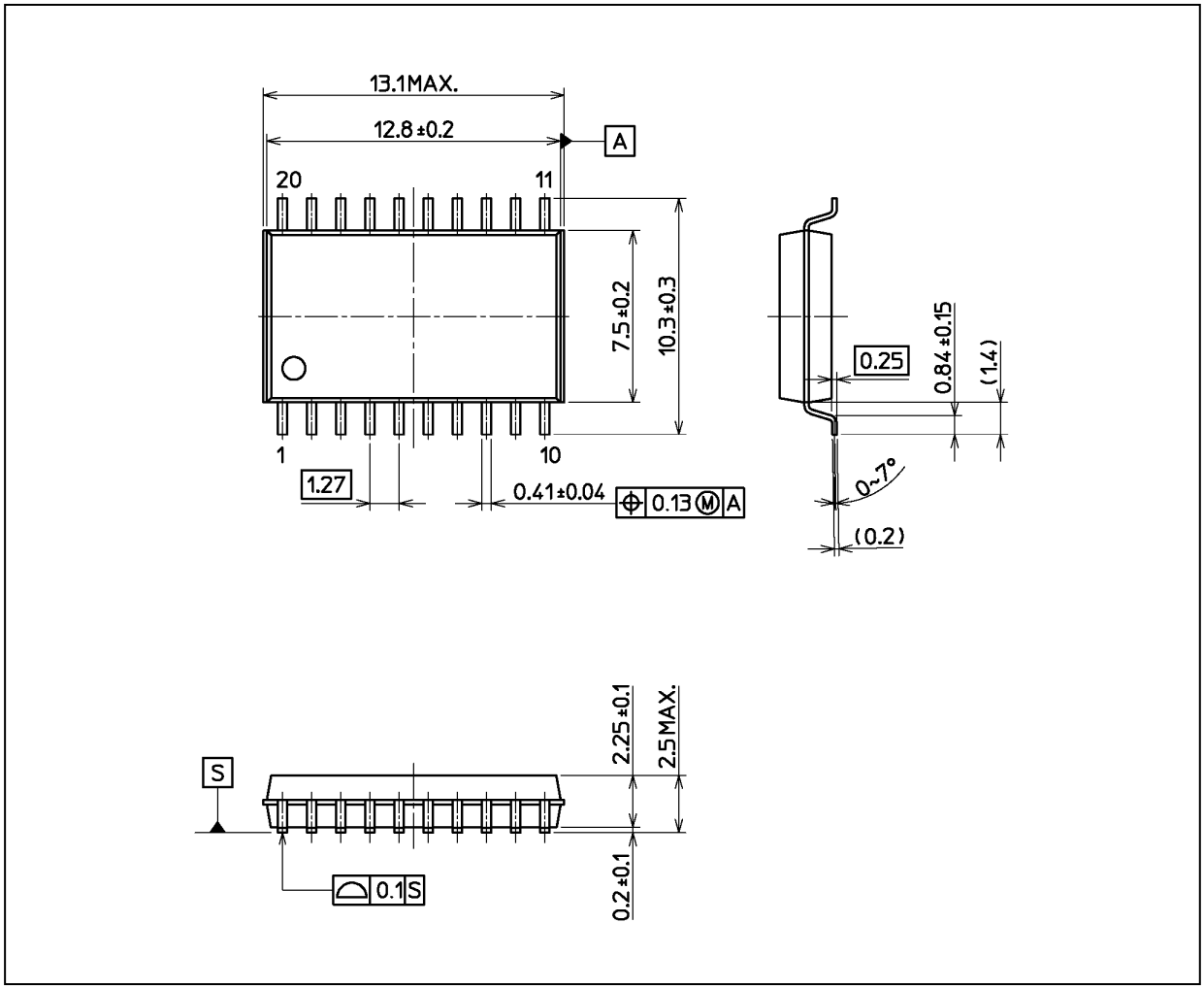
Characteristics	Symbol	Test Condition	C_L (pF)	V_{CC} (V)	Min	Max	Unit
Output transition time	t_{TLH},t_{THL}	—	50	2.0	—	75	ns
				4.5	—	15	
				6.0	—	13	
Propagation delay time (CK-Q)	t_{PLH},t_{PHL}	—	50	2.0	—	175	ns
				4.5	—	35	
				6.0	—	30	
			150	2.0	—	240	
				4.5	—	48	
				6.0	—	41	
Output enable time	t_{PZL},t_{PZH}	R_L = 1 kΩ	50	2.0	—	170	ns
				4.5	—	34	
				6.0	—	29	
			150	2.0	—	230	
				4.5	—	46	
				6.0	—	39	
Output disable time	t_{PLZ},t_{PHZ}	R_L = 1 kΩ	50	2.0	—	170	ns
				4.5	—	34	
				6.0	—	29	
Maximum clock frequency	f_{MAX}	—	50	2.0	5	—	MHz
				4.5	25	—	
				6.0	29	—	

12.9. AC Characteristics
(Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	C_L (pF)	V_{CC} (V)	Min	Max	Unit
Output transition time	t_{TLH},t_{THL}	—	50	2.0	—	90	ns
				4.5	—	18	
				6.0	—	15	
Propagation delay time (CK-Q)	t_{PLH},t_{PHL}	—	50	2.0	—	250	ns
				4.5	—	50	
				6.0	—	43	
			150	2.0	—	285	
				4.5	—	57	
				6.0	—	48	
Output enable time	t_{PZL},t_{PZH}	R_L = 1 kΩ	50	2.0	—	205	ns
				4.5	—	41	
				6.0	—	35	
			150	2.0	—	280	
				4.5	—	56	
				6.0	—	48	
Output disable time	t_{PLZ},t_{PHZ}	R_L = 1 kΩ	50	2.0	—	205	ns
				4.5	—	41	
				6.0	—	35	
Maximum clock frequency	f_{MAX}	—	50	2.0	4	—	MHz
				4.5	20	—	
				6.0	24	—	

Package Dimensions

Unit: mm



Weight: 0.51 g (typ.)

Package Name(s)
Nickname: SOIC20

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